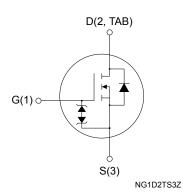




# Automotive-grade N-channel 500 V, 320 m $\Omega$ typ., 11 A MDmesh DM2 Power MOSFET in a DPAK package

# Features





Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD13N50DM2AG	500 V	360 mΩ	11 A

- AEC-Q101 qualified
- · Fast-recovery body diode
- · Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- · Extremely high dv/dt ruggedness
- · Zener-protected

#### **Applications**

· Switching applications

#### **Description**

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.



# Product status STD13N50DM2AG

Product summary		
Order code	STD13N50DM2AG	
Marking	13N50DM2	
Package	DPAK	
Packing	Tape and reel	



# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate-source voltage	±25	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	11	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	8	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	28	Α
P <sub>TOT</sub>	Total power dissipation at T <sub>C</sub> = 25 °C	110	W
dv/dt (2)	Peak diode recovery voltage slope	50	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T <sub>stg</sub>	Storage temperature range	-55 to 150	°C
T <sub>j</sub>	Operating junction temperature range	-55 to 150	C

- 1. Pulse width limited by safe operating area.
- 2.  $I_{SD} \le 11~A,~di/dt \le 800~A/\mu s;~V_{DS~peak} < V_{(BR)DSS},~V_{DD} = 400~V$
- $3. \quad V_{DS} \leq 400 \ V$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	1.14	°C/W
R <sub>thj-pcb</sub> (1)	R <sub>thj-pcb</sub> <sup>(1)</sup> Thermal resistance junction-pcb		C/VV

1. When mounted on a 1-inch² FR-4, 2 oz Cu board

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetetive or not repetetive (pulse width limited by $T_{jmax}$ )	2	А
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 50$ V)	230	mJ

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### 2 Electrical characteristics

( $T_C$  = 25 °C unless otherwise specified).

**Table 4. Static** 

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	500			V
	Zana mata walta na daala	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 500 V			1	μA
I <sub>DSS</sub>	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 500 \text{ V},$ $T_C = 125 \text{ °C}^{(1)}$			100	μА
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±5	μA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.5 A		320	360	mΩ

<sup>1.</sup> Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	597	-	pF
C <sub>oss</sub>	Output capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	38	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	3.5	-	pF
Coss eq. (1)	Equivalent output capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	69	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz open drain	-	7	-	Ω
Qg	Total gate charge	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 11 A,	-	11.7	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 0 to 10 V (see Figure 14. Test circuit for gate	-	3.8	-	nC
Q <sub>gd</sub>	Gate-drain charge	charge behavior)	-	4.2	-	nC

<sup>1.</sup>  $C_{\rm oss~eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\rm oss}$  when  $V_{\rm DS}$  increases from 0 to 80%  $V_{\rm DSS}$ 

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 5.5 A	-	13	-	ns
t <sub>r</sub>	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$ (see Figure 13. Test circuit for	-	9	-	ns
t <sub>d(off)</sub>	Turn-off delay time	resistive load switching times and Figure 18. Switching time	-	26	-	ns
t <sub>f</sub>	Fall time	waveform)	-	8	-	ns

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Table 7. Source-drain diode

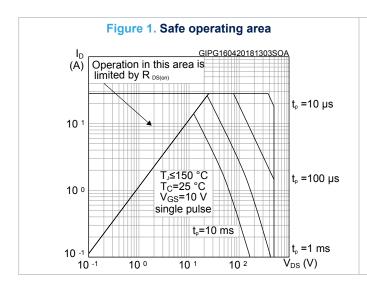
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		-		11	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		28	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 11 A	-		1.6	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 11 A, di/dt = 100 A/μs,	-	68		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 60 V (see Figure 15. Test circuit for	-	200		nC
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times)	-	5.9		Α
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 11 \text{ A, di/dt} = 100 \text{ A/µs,}$	-	107		ns
Q <sub>rr</sub>	Reverse recovery charge	$V_{DD}$ = 60 V, $T_j$ = 150 °C (see Figure 15. Test circuit for	-	450		nC
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times)	-	8.5		А

<sup>1.</sup> Pulse width is limited by safe operating area

<sup>2.</sup> Pulse test: pulse duration = 300  $\mu$ s, duty cycle 1.5%



### 2.1 Electrical characteristics (curves)



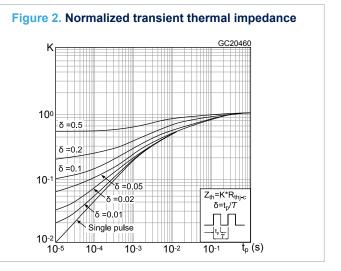
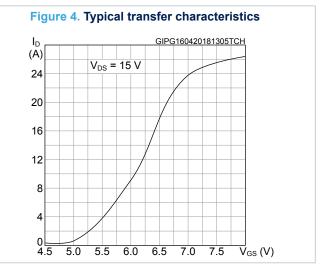
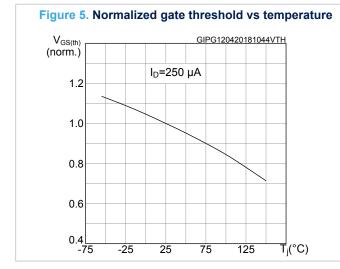
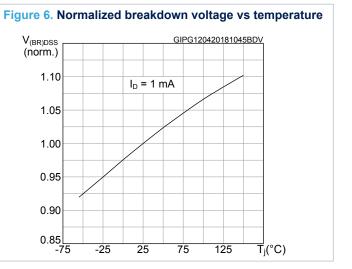


Figure 3. Typical output characteristics GIPG160420181305OCH  $I_{\mathsf{D}}$ (A) V<sub>GS</sub> = 8, 9, 10 V 24  $V_{GS}$  =7 V 20 16 12 V<sub>GS</sub> =6 V  $V_{GS} = \overline{5} V$ 0 12 16  $\overline{V}_{DS}(V)$ 







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Figure 7. Typical drain-source on-resistance

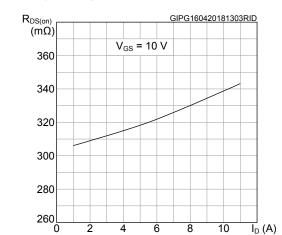


Figure 8. Normalized on-resistance vs. temperature

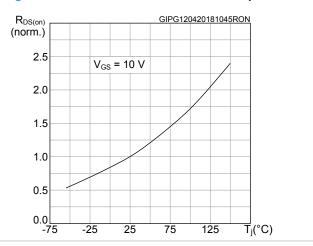


Figure 9. Typical gate charge characteristics

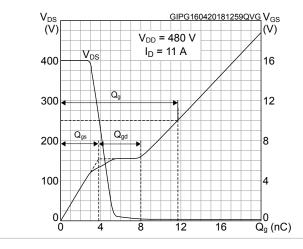


Figure 10. Typical capacitance characteristics

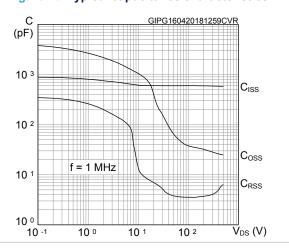


Figure 11. Typical output capacitance stored energy

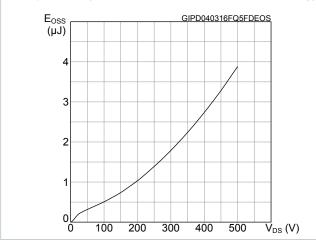
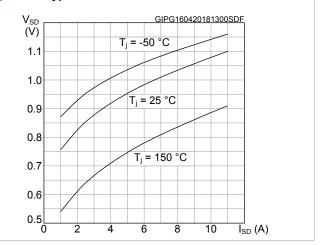


Figure 12. Typical reverse diode forward characteristics



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### 3 Test circuits

Figure 13. Test circuit for resistive load switching times

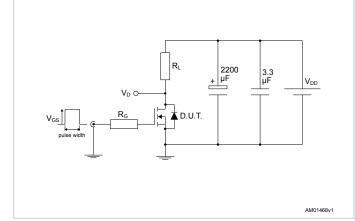


Figure 14. Test circuit for gate charge behavior

VGS

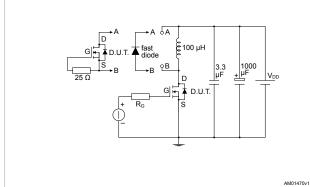
PUSE WICH 100 \( \Omega \)

VGS

PUSE WICH 100 \( \Omega \)

AND 14869/10

Figure 15. Test circuit for inductive load switching and diode recovery times



V<sub>0</sub>

Figure 16. Unclamped inductive load test circuit

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Figure 17. Unclamped inductive waveform

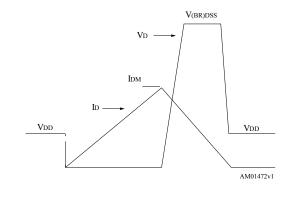
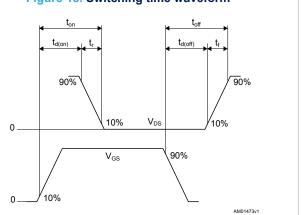


Figure 18. Switching time waveform



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# 4 Package information

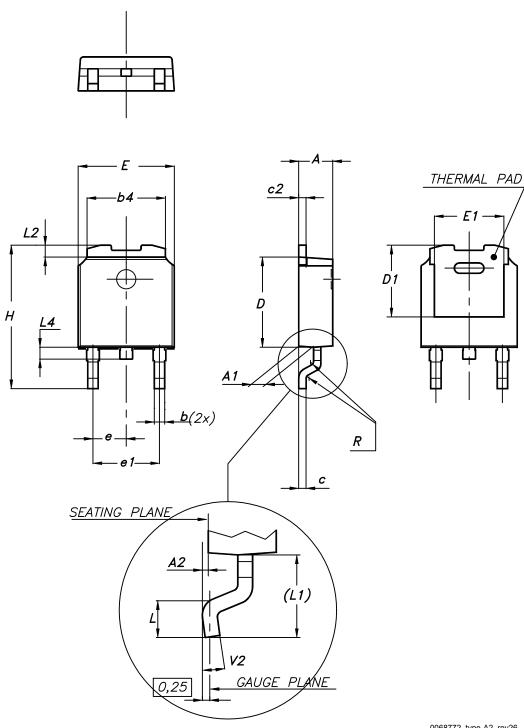
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: <a href="https://www.st.com">www.st.com</a>. ECOPACK is an ST trademark.

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#### DPAK (TO-252) type A2 package information 4.1

Figure 19. DPAK (TO-252) type A2 package outline



0068772\_type-A2\_rev26

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Table 8. DPAK (TO-252) type A2 mechanical data

Dim.		mm	
Dim.	Min.	Тур.	Max.
Α	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

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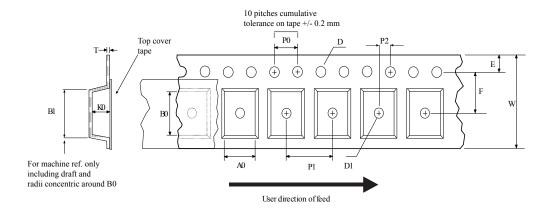
Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)

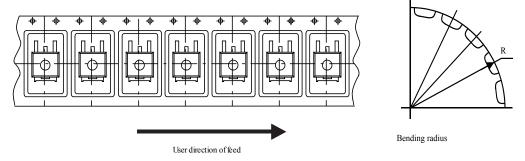
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# 4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



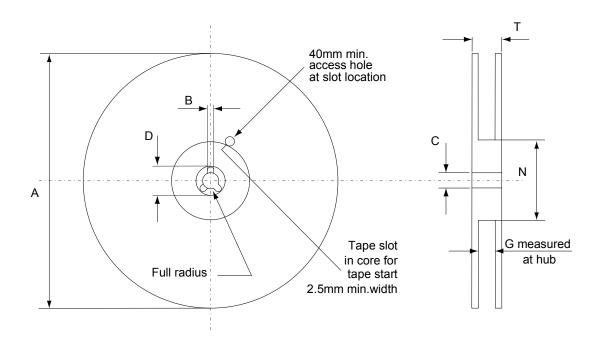


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Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Таре			Reel		
Dim.	n	nm	Dim.		mm
Dilli.	Min.	Max.		Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
Е	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Bas	se qty.	2500
P1	7.9	8.1	Bul	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

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# **Revision history**

Table 10. Document revision history

Date	Revision	Changes
23-Jun-2017	1	First release.
16-Apr-2018	2	Removed maturity status indication from cover page. The document status is production data.  Modified title, Table 1. Absolute maximum ratings, Table 3. Avalanche characteristics, Table 4. Static, Table 5. Dynamic, Table 6. Switching times, Table 7. Source drain diode.  Modified Section 2.1 Electrical characteristics (curves).  Minor text changes.
27-Jun-2018	3	Updated Section 4 Package information.
31-Oct-2019	4	Modified Features table on cover page and Table 4. Static.  Updated Section 4.1 DPAK (TO-252) type A2 package information.  Minor text changes.

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Revision history			14	



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