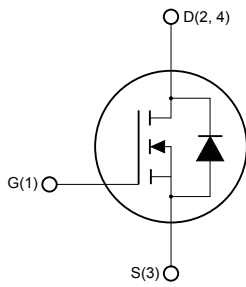
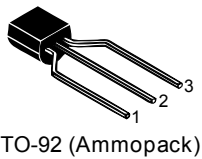


N-channel 600 V, 7.3 Ω typ., 0.4 A SuperMESH™ Power MOSFETs in a SOT-223 and TO-92 packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STN1HNK60	600 V	8.5 Ω	0.4 A	SOT-223
STQ1HNK60R-AP				TO-92

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status

STN1HNK60

STQ1HNK60R-AP

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		SOT-223	TO-92	
V_{DS}	Drain-source voltage	600		V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	600		V
V_{GS}	Gate- source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25 \text{ }^\circ\text{C}$	0.4		A
I_D	Drain current (continuous) at $T_C = 100 \text{ }^\circ\text{C}$	0.25		A
$I_{DM}^{(1)}$	Drain current (pulsed)	1.6		A
P_{TOT}	Total dissipation at $T_C = 25 \text{ }^\circ\text{C}$	3.3	3	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	3		V/ns
T_j	Operating junction temperature range	-55 to 150		$^\circ\text{C}$
T_{stg}	Storage temperature range			

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 0.4 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		SOT-223	TO-92	
$R_{thj-amb}$	Thermal resistance junction-ambient		120	$^\circ\text{C}/\text{W}$
$R_{thj-lead}$	Thermal resistance junction-lead		40	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	37.87		$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 in^2 , 2 oz Cu, $t < 10 \text{ s}$.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j \text{ Max}$)	0.4	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25 \text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50 \text{ V}$)	25	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.25	3	3.7	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$		7.3	8.5	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	156		μF
C_{oss}	Output capacitance			23.5		
C_{rss}	Reverse transfer capacitance			3.8		
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 1\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	7	10	nC
Q_{gs}	Gate-source charge			1.1		
Q_{gd}	Gate-drain charge			3.7		

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 0.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	6.5	-	ns
t_r	Rise time			5		
$t_{d(off)}$	Turn-off delay time			19		
t_f	Fall time			25		

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				0.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		1.6	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.4 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.0 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		140		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 25 \text{ V}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	240		nC
I_{RRM}	Reverse recovery current			3.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 1.0 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		229		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 25 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	377		nC
I_{RRM}	Reverse recovery current			3.3		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

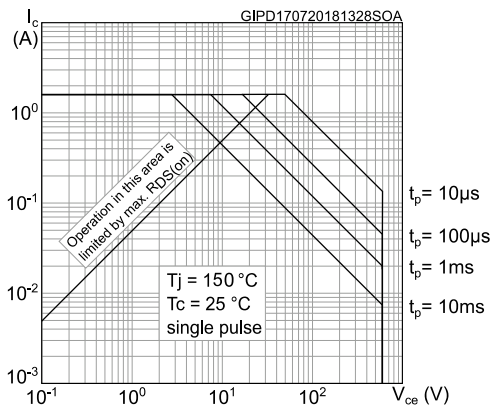
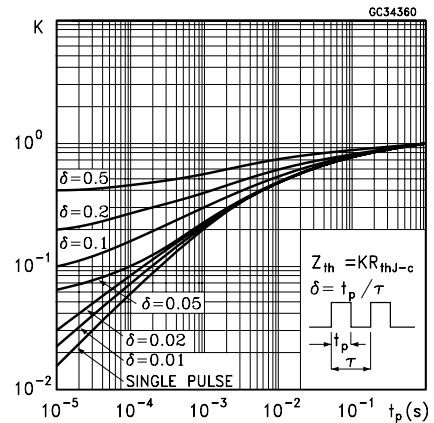
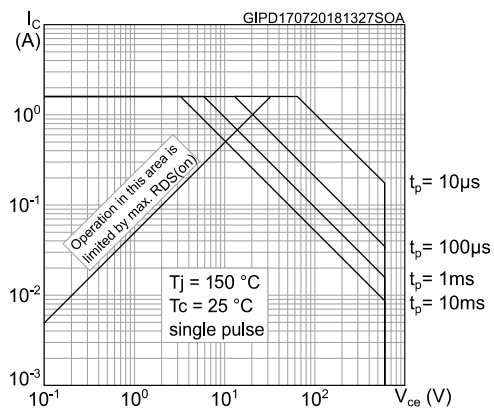
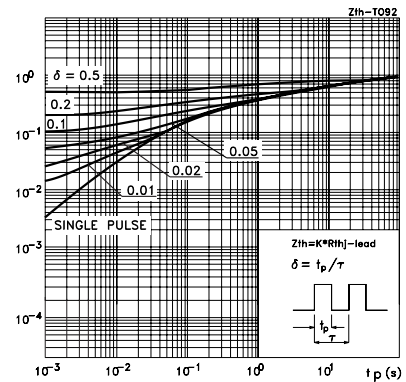
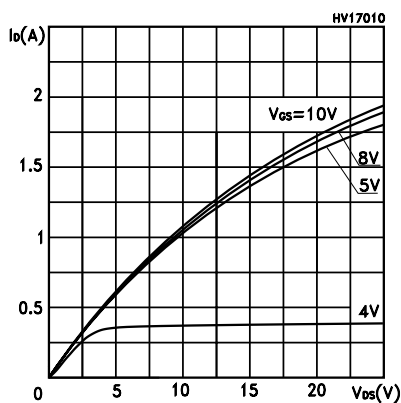
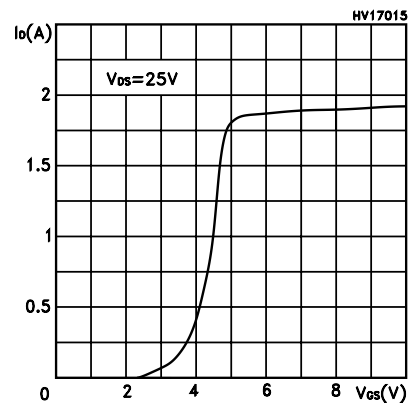
Figure 1. Safe operating area for SOT-223

Figure 2. Thermal impedance for SOT-223

Figure 3. Safe operating area for TO-92

Figure 4. Thermal impedance for TO-92

Figure 5. Output characteristics

Figure 6. Transfer characteristics


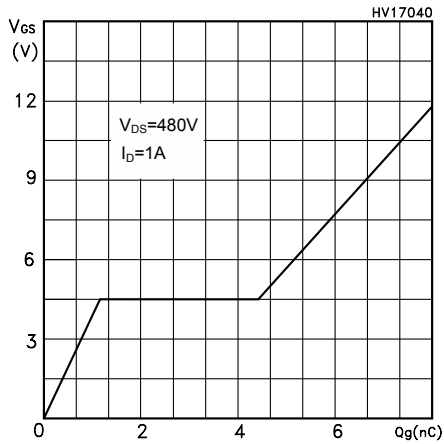
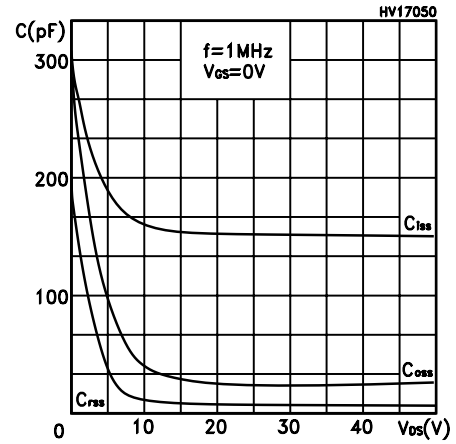
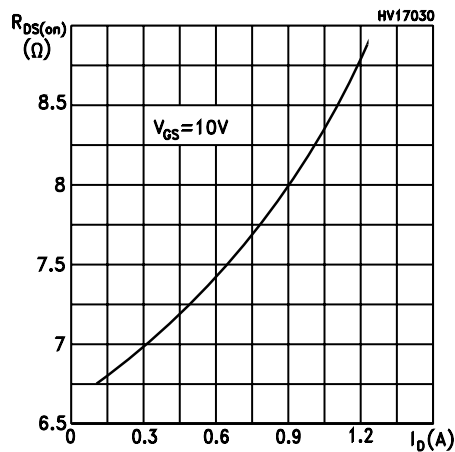
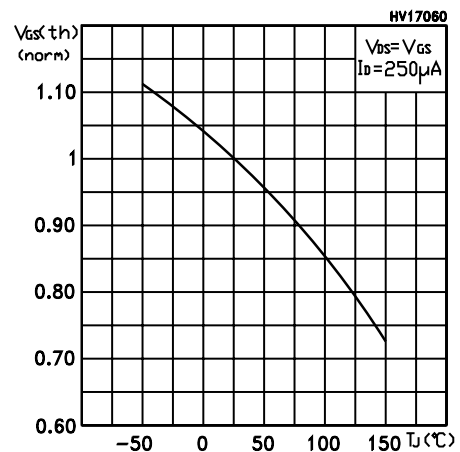
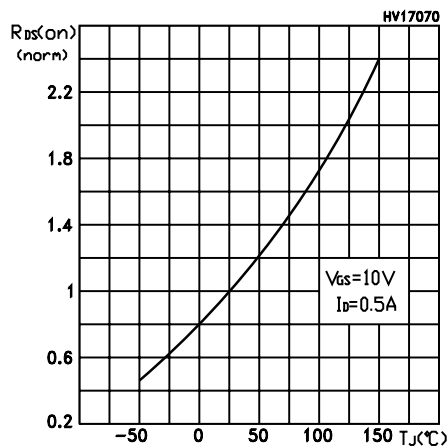
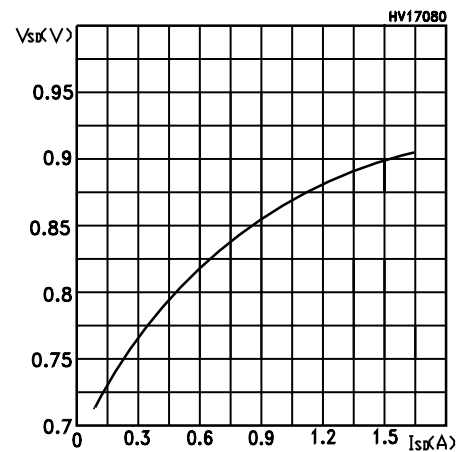
Figure 7. Gate charge vs gate-source voltage

Figure 8. Capacitance variations

Figure 9. Static drain-source on-resistance

Figure 10. Normalized gate threshold voltage vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Source-drain forward characteristics


Figure 13. Normalized $V_{(BR)DSS}$ vs Temperature

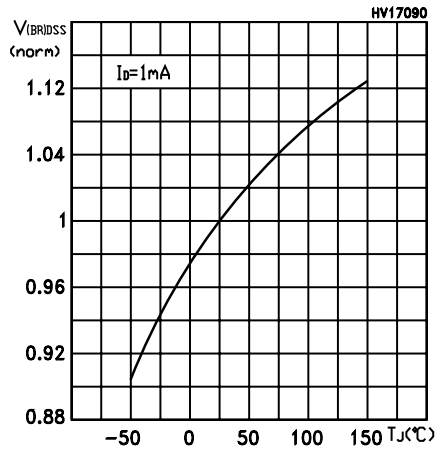
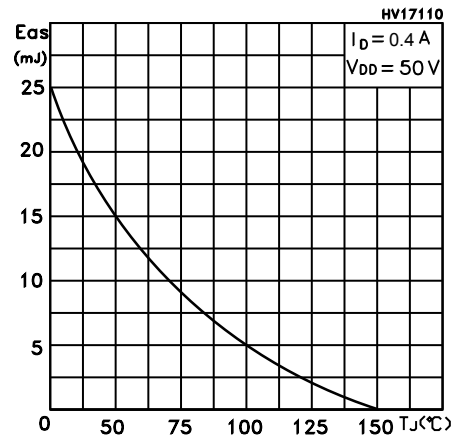
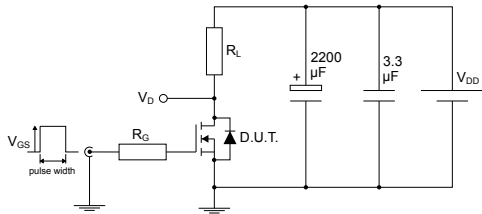


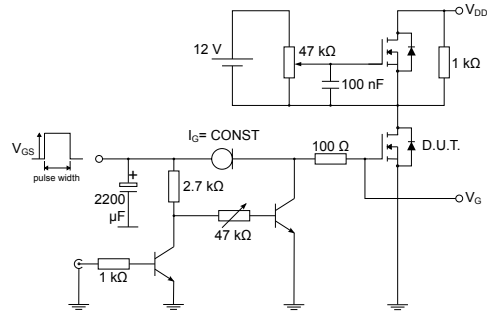
Figure 14. Maximum avalanche energy vs temperature



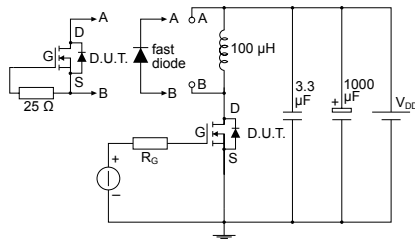
3 Test circuits

Figure 15. Test circuit for resistive load switching times


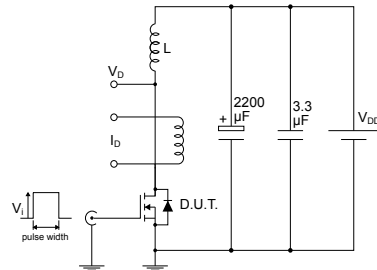
AM01468v1

Figure 16. Test circuit for gate charge behavior


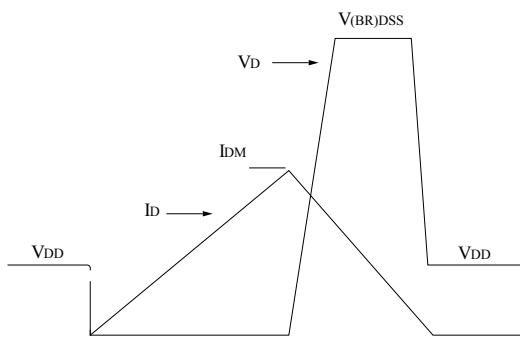
AM01469v1

Figure 17. Test circuit for inductive load switching and diode recovery times


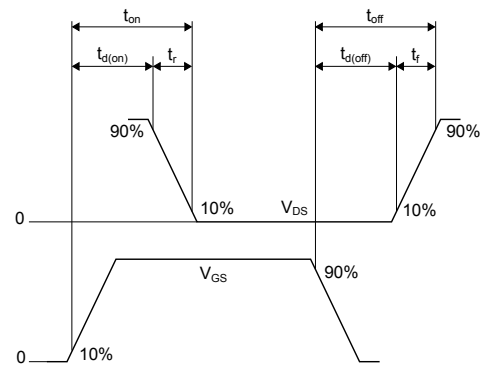
AM01470v1

Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


AM01472v1

Figure 20. Switching time waveform


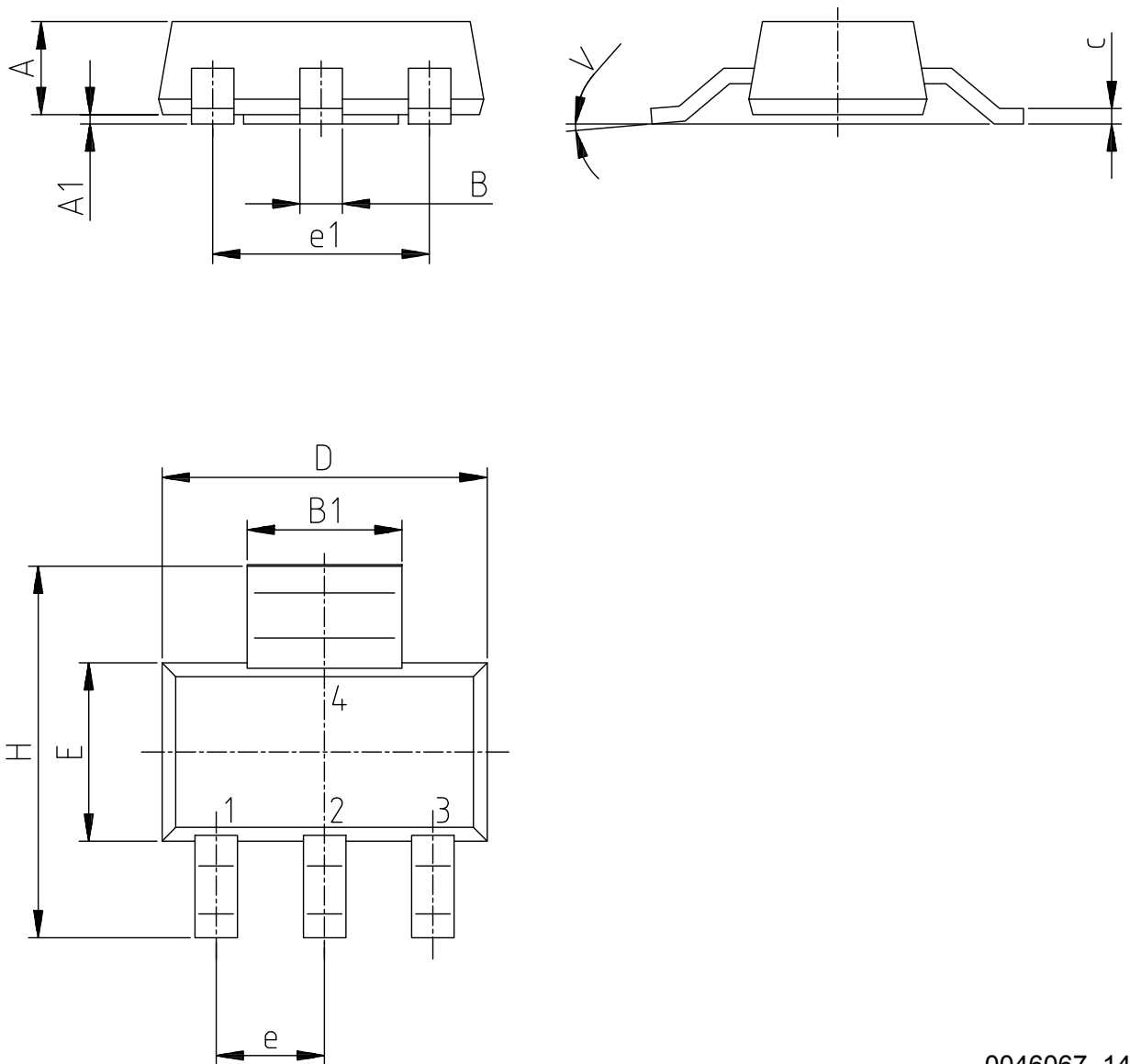
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 SOT-223 package information

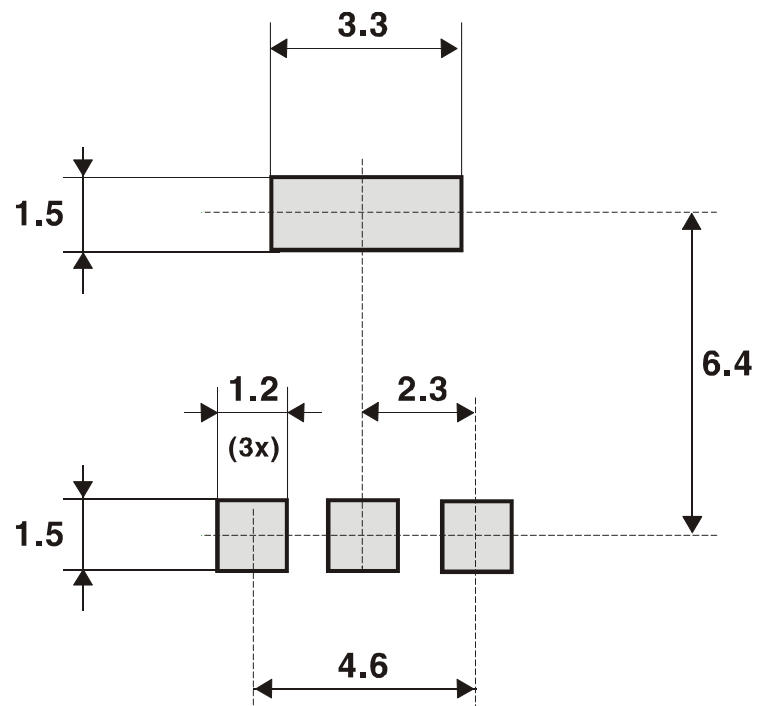
Figure 21. SOT-223 package outline



0046067_14

Table 8. SOT-223 package mechanical data

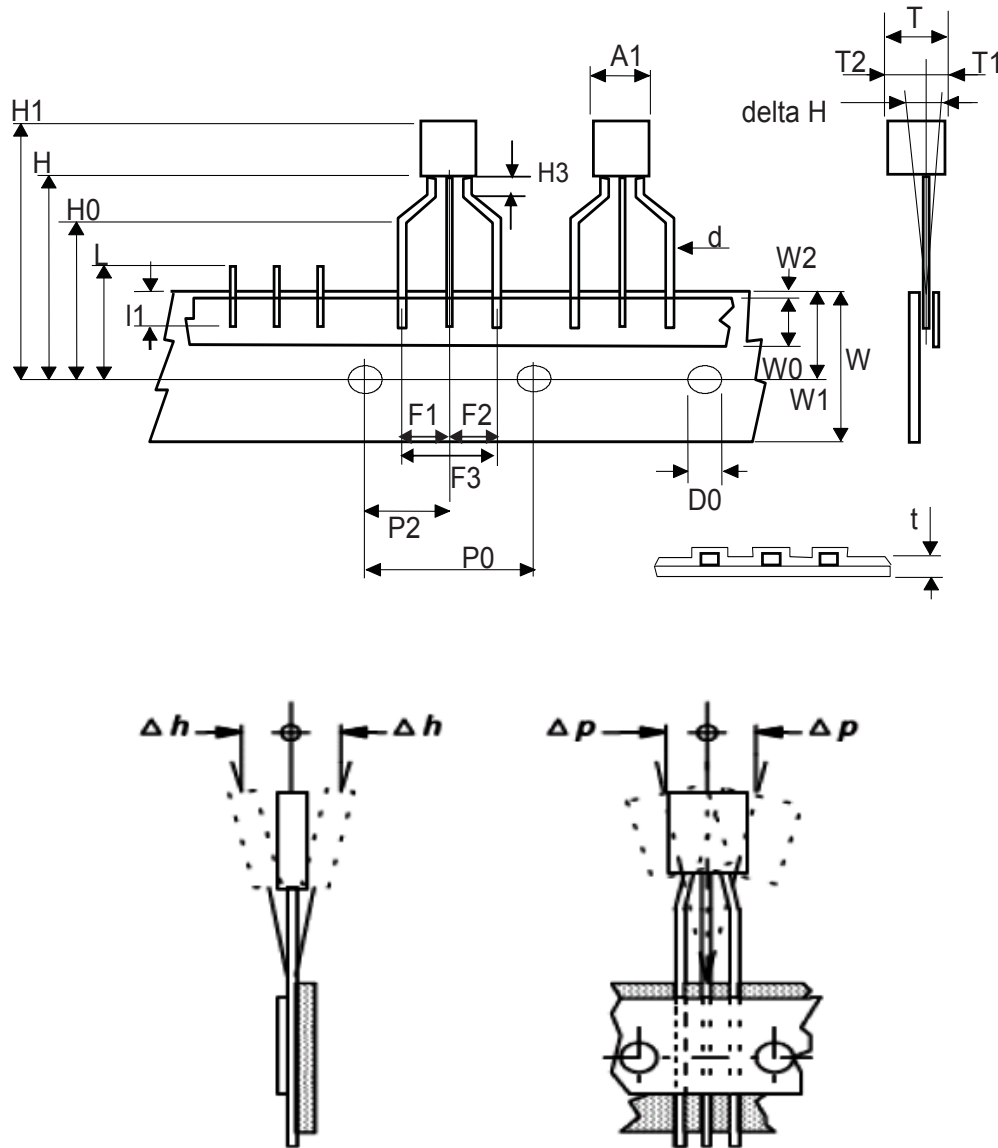
Dim.	mm		
	Min.	Typ.	Max.
A			1.8
A1	0.02		0.1
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7.0	7.3
V			10°

Figure 22. SOT-223 recommended footprint (dimensions are in mm)


0046067

4.2 TO-92 Ammopack package information

Figure 23. TO-92 Ammopack package outline



0050910_Rev_22

Table 9. TO-92 Ammopack mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			4.80
T			3.80
T1			1.60
T2			2.30
d	0.45	0.47	0.48
P0	12.50	12.70	12.90
P2	5.65	6.35	7.05
F1, F2	2.40	2.50	2.94
F3	4.98	5.08	5.48
delta H	-2.00		2.00
W	17.50	18.00	19.00
W0	5.50	6.00	6.50
W1	8.50	9.00	9.25
W2			0.50
H		18.50	21.00
H0	15.50	16.00	18.20
H1		25.00	27.00
H3	0.50	1.00	2.00
D0	3.80	4.00	4.20
t			0.90
L			11.00
l1	3.00		
delta P	-1.00		1.00

5 Ordering information

Table 10. Order codes

Order code	Marking	Package	Packing
STN1HNK60	N1HNK60	SOT-223	Tape and reel
STQ1HNK60R-AP	1HNK60R	TO-92	Ammopak

Revision history

Table 11. Document revision history

Date	Version	Changes
20-Aug-2018	1	Initial release.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics curves	5
3	Test circuits	8
4	Package information	9
4.1	SOT-223 package information	9
4.2	TO-92 Ammopack package information	10
5	Ordering information	13
	Revision history	14

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved