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FDS6975

Dual P-Channel, Logic Level, PowerTrench™ MOSFET

General Description

These P-Channel Logic Level MOSFETs are produced using ON Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for notebook computer applications: load switching and power management, battery charging circuits, and DC/DC conversion.

Features

- -6 A, -30 V. $R_{DS(ON)}$ = 0.032 Ω @ V_{GS} = -10 V, $R_{DS(ON)}$ = 0.045 Ω @ V_{GS} = -4.5 V.

- Low gate charge (14.5nC typical).

- High performance trench technology for extremely low $R_{DS(ON)}$.

- High power and current handling capability.

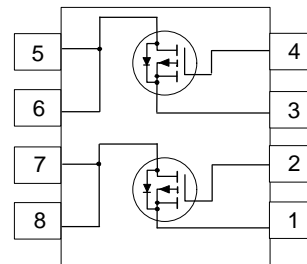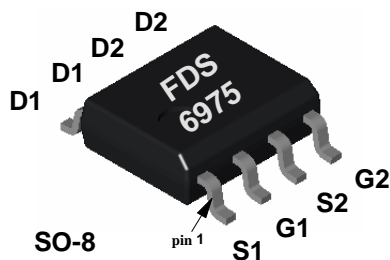| SOT-23	SuperSOT™-6	SuperSOT™-8	SO-8	SOT-223	SOIC-16

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	-6	A
	- Pulsed		-20	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)		78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)		40	°C/W

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Electrical Characteristics (T$_A$ = 25 ^{O}C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	V$_{GS}$ = 0 V, I$_D$ = -250 µA		-30			V
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	I$_D$ = -250 µA, Referenced to 25 ^{O}C			-21		mV/^{O}C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{DS}$ = -24 V, V$_{GS}$ = 0 V				-1	µA
			T$_J$ = 55°C			-10	µA
I$_{GSSF}$	Gate - Body Leakage, Forward	V$_{GS}$ = 20 V, V$_{DS}$ = 0 V				100	nA
I$_{GSSR}$	Gate - Body Leakage, Reverse	V$_{GS}$ = -20 V, V$_{DS}$ = 0 V				-100	nA
ON CHARACTERISTICS (Note 2)							
V$_{GS(th)}$	Gate Threshold Voltage	V$_{DS}$ = V$_{GS}$, I$_D$ = -250 µA		-1	-1.7	-3	V
ΔV$_{GS(th)}$/ΔT$_J$	Gate Threshold Voltage Temp. Coefficient	I$_D$ = 250 µA, Referenced to 25 ^{O}C			4		mV/^{O}C
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V$_{GS}$ = -10 V, I$_D$ = -6 A			0.025	0.032	Ω
			T$_J$ =125°C		0.033	0.051	
		V$_{GS}$ = -4.5 V, I$_D$ = -5 A			0.034	0.045	
I$_{D(ON)}$	On-State Drain Current	V$_{GS}$ = -10 V, V$_{DS}$ = -5 V		-20			A
g$_{FS}$	Forward Transconductance	V$_{DS}$ = -10 V, I$_D$ = -6 A			16		S
DYNAMIC CHARACTERISTICS							
C$_{iss}$	Input Capacitance	V$_{DS}$ = -15 V, V$_{GS}$ = 0 V, f = 1.0 MHz			1540		pF
C$_{oss}$	Output Capacitance				400		pF
C$_{rss}$	Reverse Transfer Capacitance				170		pF
SWITCHING CHARACTERISTICS (Note 2)							
t$_{D(on)}$	Turn - On Delay Time	V$_{DS}$ = -15 V, I$_D$ = -1 A			13	24	ns
t$_r$	Turn - On Rise Time	V$_{GEN}$ = -10 V, R$_{GEN}$ = 6 Ω			22	35	ns
t$_{D(off)}$	Turn - Off Delay Time				47	75	ns
t$_f$	Turn - Off Fall Time				18	30	ns
Q$_g$	Total Gate Charge	V$_{DS}$ = -10 V, I$_D$ = -6 A,			14.5	20	nC
Q$_{gs}$	Gate-Source Charge	V$_{GS}$ = -5 V			4		nC
Q$_{gd}$	Gate-Drain Charge				5		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I$_S$	Maximum Continuous Drain-Source Diode Forward Current					-1.3	A
V$_{SD}$	Drain-Source Diode Forward Voltage	V$_{GS}$ = 0 V, I$_S$ = -1.3 A (Note 2)			-0.73	-1.2	V

Notes:

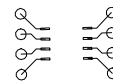1. R$_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R$_{\theta JC}$ is guaranteed by design while R$_{\theta CA}$ is determined by the user's board design.
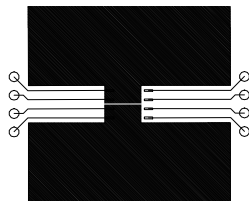
a. 78°C/W on a 0.5 in^2 pad of 2oz copper.
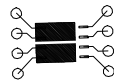
b. 125°C/W on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W on a 0.003 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.
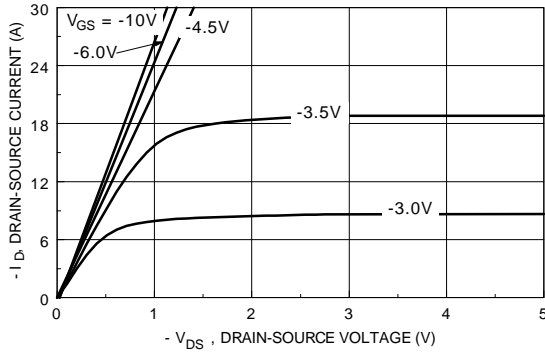
Typical Electrical Characteristics

Figure 1. On-Region Characteristics.
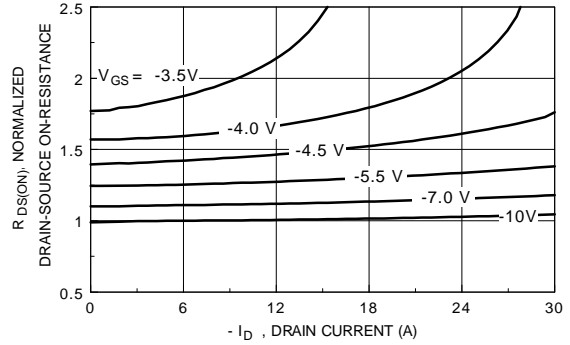

Figure 2. On-Resistance Variation with
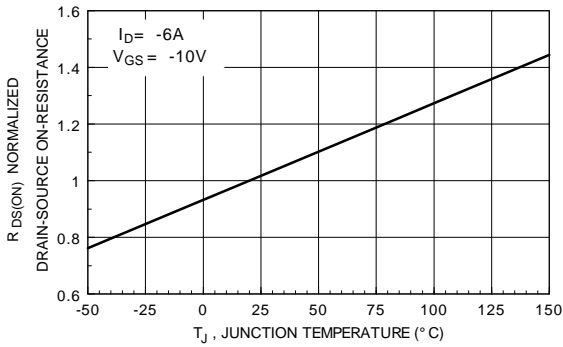Dain Current and Gate Voltage.

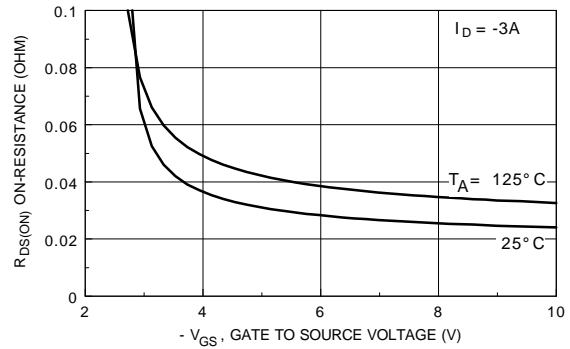Figure 3. On-Resistance Variation   with
Temperature.

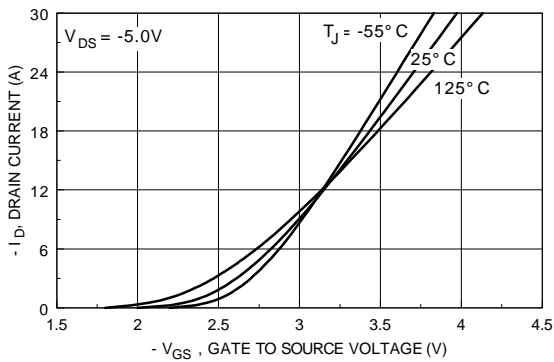Figure 4. On-Resistance Variation with
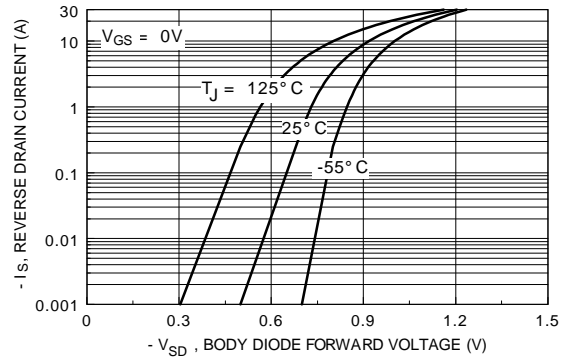Gate-to-Source Voltage.

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage
Variation with Source Current
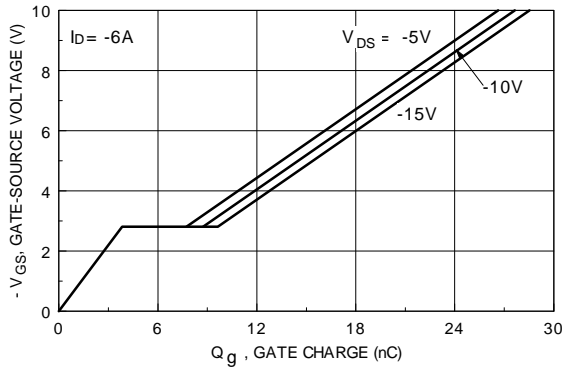and Temperature.

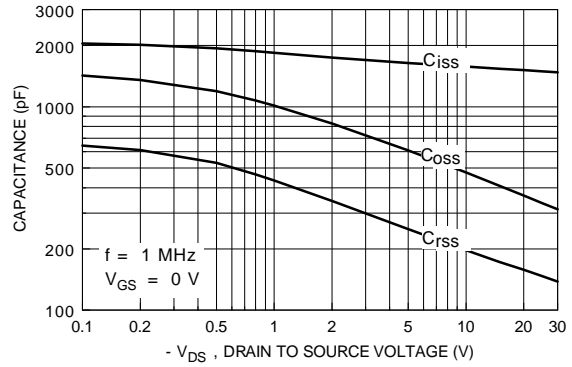# Typical Electrical Characteristics (continued)

Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.
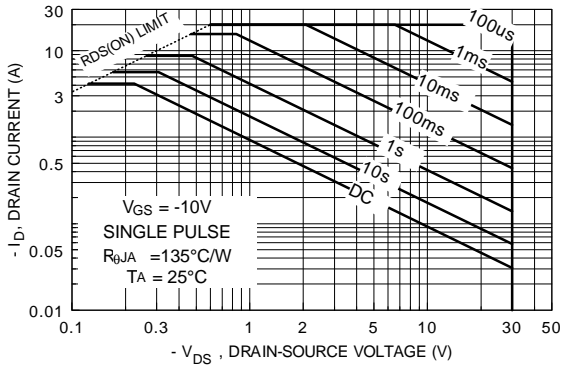
Figure 9. Maximum Safe Operating Area.
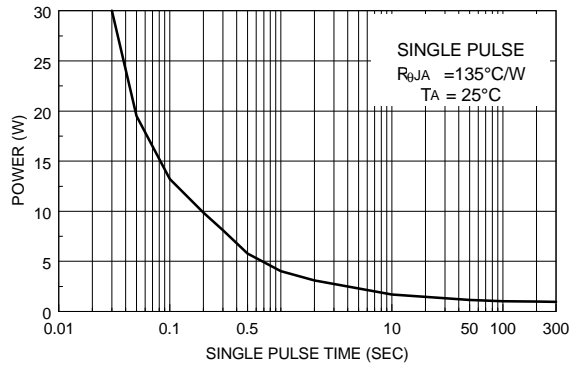
Figure 10. Single Pulse Maximum Power Dissipation.

$$R_{\theta JA}(t) = r(t) * R_{\theta JA}$$
$$R_{\theta JA} = 135°C/W$$
$$T_J - T_A = P * R_{\theta JA}(t)$$
$$\text{Duty Cycle, } D = t_1 / t_2$$
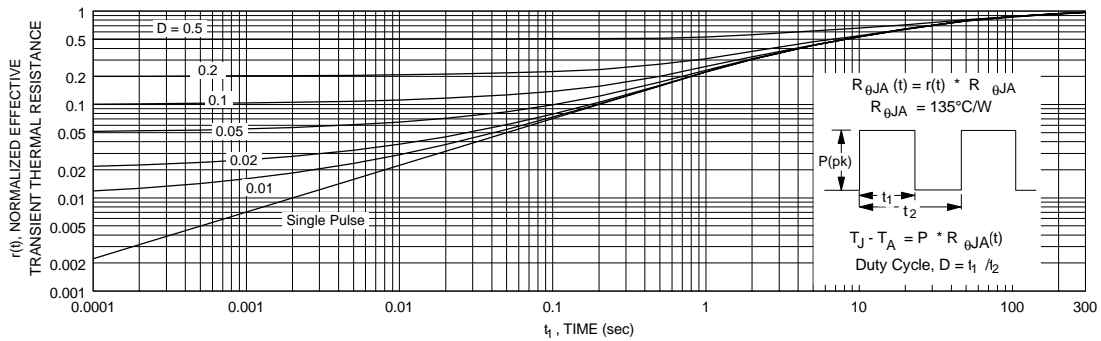
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

PUBLICATION ORDERING INFORMATION

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