

STO362N8F7AG

Automotive N-channel 80 V, 1.6 mΩ max., 300 A STripFET[™] F7 Power MOSFET in a TO-LL package

Figure 1: Internal schematic diagram



Datasheet - preliminary data

Features

Order code	VDS	RDS(on) max.	ID
STO362N8F7AG	80 V	1.8 mΩ	300 A

Designed for automotive applications

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

• Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low onstate resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STO362N8F7AG	362N8F7	TO-LL	Tape and reel

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
I _D ⁽¹⁾	Drain current (continuous) at Tc = 25 °C	300	А
lD	Drain current (continuous) at Tc = 100 °C	257	А
IDM ⁽²⁾	Drain current (pulsed)	1200	А
Ртот	Total dissipation at $T_C = 25 \ ^{\circ}C$	441	W
TJ	T _J Operating junction temperature range		°C
T _{stg}	Storage temperature range		C

Notes:

⁽¹⁾Limited by package.

 $^{(2)}\mbox{Pulse}$ width limited by safe operating area

Table 3: Thermal data				
Symbol	Parameter	Value	Unit	
R _{thj-case}	Thermal resistance junction-case	0.34	°C/W	



2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	80			V
Zara sata valtara dasis		V_{GS} = 0 V, V_{DS} = 80 V			1	μA
loss current	$V_{GS} = 0 V, V_{DS} = 80 V,$ Tj = 125 °C ⁽¹⁾			100	μA	
I _{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 μ A	2.5		4.5	V
R _{DS(on)}	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 150 \text{ A}$			1.6	mΩ

Notes:

⁽¹⁾Defined by design, not subject to production test.

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	16500	I	pF
Coss	Output capacitance	V_{DS} = 25 V, f = 1 MHz,	-	4200	I	pF
Crss	Reverse transfer capacitance	V _{GS} = 0 V	-	290	-	pF
Qg	Total gate charge	$V_{DD} = 40 V, I_D = 300 A,$	-	240	-	nC
Q _{gs}	Gate-source charge	$V_{GS} = 0$ to 10 V	-	TBD	I	nC
Q _{gd}	Gate-drain charge	for gate charge behavior")	-	TBD	-	nC

Table 5: Dynamic



3 Test circuits







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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.







Figure 8: TO-LL package outline

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Package information

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Table 6: TO-LL package mechanical data						
Dim	mm			mm		
Dim.	Min.	Тур.	Max.			
А	2.20	2.30	2.40			
A1	0.40	0.48	0.60			
b		0.80				
С		0.46				
c1		0.15				
С	10.28	10.38	10.48			
C2	2.35	2.45	2.55			
C3		0.71				
D	9.80	9.90	10.00			
D2	3.30	3.50	3.70			
D3	9.30	9.40	9.50			
D4	8.20	8.40	8.6			
D5	9.50	9.70	9.90			
D6		7.40				
D7		2.20				
е		1.20				
E	11.48	11.68	11.88			
E1		4.96				
E2		5.54				
E3		5.14				
E4		0.90				
E5		0.72				
E6	6.41	6.61	6.81			
E7	0.50	0.70	0.90			
К	1.70	1.90	2.10			
L	1.05	1.20	1.35			
L1	0.25	0.35	0.45			
L2	0.40	0.60	0.80			
θ		11°				

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Package information





5 Revision history

Table 7: Document revision history

Date	Revision	Changes
01-Dec-2018	1	First release

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