# NTHD4401P

# Power MOSFET

## −20 V, −3.0 A, Dual P−Channel, ChipFET™

### Features

- Low $R_{DS(on)}$ and Fast Switching Speed in a ChipFET Package
- Leadless ChipFET Package 40% Smaller Footprint than TSOP−6
- ChipFET Package with Excellent Thermal Capabilities where Heat Transfer is Required
- Pb−Free Package is Available

### Applications

- Charge Control in Battery Chargers
- Optimized for Battery and Load Management Applications in Portable Equipment
- MP3 Players, Cell Phones, Digital Cameras, PDAs
- Buck and Boost DC−DC Converters

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | −20 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | −2.1 | A |
| | | $T_A$ = 85°C | | −1.5 | |
| | t ≤ 5 s | $T_A$ = 25°C | | −3.0 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 1.1 | W |
| | | $T_A$ = 85°C | | 0.6 | |
| | t ≤ 5 s | $T_A$ = 25°C | | 2.1 | |
| Pulsed Drain Current | tp = 10 μs | | $I_{DM}$ | −9.0 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | −2.5 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

**THERMAL RESISTANCE RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 110 | °C/W |
| Junction−to−Ambient − t ≤ 5 s | | 60 | |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

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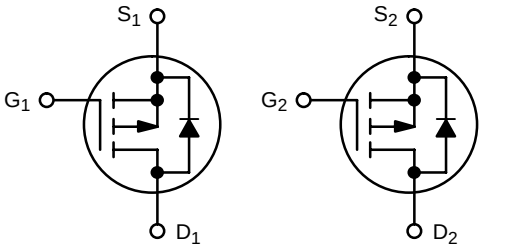
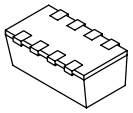
| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| −20 V | 130 mΩ @ −4.5 V | −3.0 A |
| | 200 mΩ @ −2.5 V | |

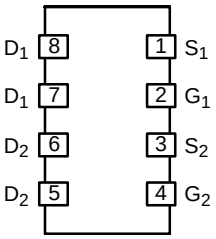



**P−Channel MOSFET** **P−Channel MOSFET**

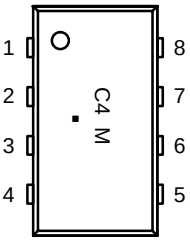


**ChipFET**
**CASE 1206A**
**STYLE 2**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




C4 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTHD4401PT1 | ChipFET | 3000/Tape & Reel |
| NTHD4401PT1G | ChipFET (Pb−Free) | 3000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(Br)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = −250 μA | | −20 | −23 | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(Br)DSS}/T_J$ | | | | −8.0 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V | $T_J$ = 25°C | | | −1.0 | μA |
| | | $V_{DS}$ = −16 V | $T_J$ = 85°C | | | −5.0 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = −250 μA | | −0.6 | −0.75 | −1.2 | V |
| Gate Threshold Temperature Coefficient | $V_{GS(th)}/T_J$ | | | | 2.65 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = −4.5 V, $I_D$ = −2.1 A<br>$V_{GS}$ = −2.5 V, $I_D$ = −1.7 A<br>$V_{GS}$ = −1.8 V, $I_D$ = −1.0 A | | | 0.130<br>0.200<br>0.34 | 0.155<br>0.240 | Ω |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = −10 V, $I_D$ = −2.1 A | | | 5.0 | | S |
| **CHARGES, CAPACITANCES AND GATE RESISTANCE** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = −10 V | | | 185 | 300 | pF |
| Output Capacitance | $C_{oss}$ | | | | 95 | 150 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 30 | 50 | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = −4.5 V, $V_{DS}$ = −10 V, $I_D$ = −2.1 A | | | 3.0 | 6.0 | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 0.2 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 0.5 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 0.9 | | |
| **SWITCHING CHARACTERISTICS** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = −4.5 V, $V_{DD}$ = −16 V, $I_D$ = −2.1 A, $R_G$ = 2.5 Ω | | | 7.0 | 12 | ns |
| Rise Time | $t_r$ | | | | 13 | 25 | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 33 | 50 | |
| Fall Time | $t_f$ | | | | 27 | 40 | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = −2.5 A | | | −0.85 | −1.15 | V |
| Reverse Recovery Time | $t_{rr}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 90 A/μs, $I_S$ = −2.1 A | | | 32 | | ns |
| Charge Time | $t_a$ | | | | 10 | | |
| Discharge Time | $t_b$ | | | | 22 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 15 | | nC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

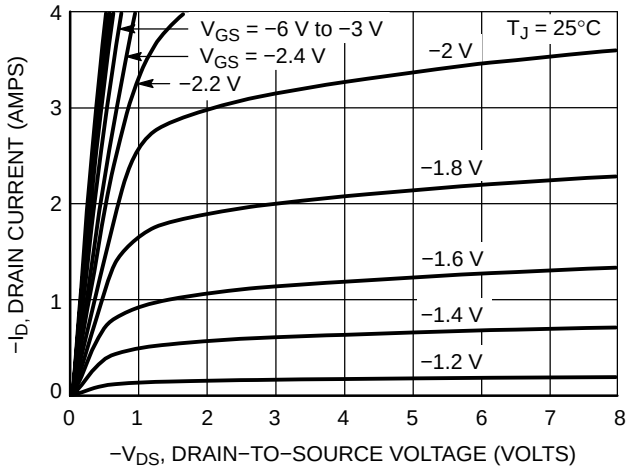



**Figure 1. On−Region Characteristics**

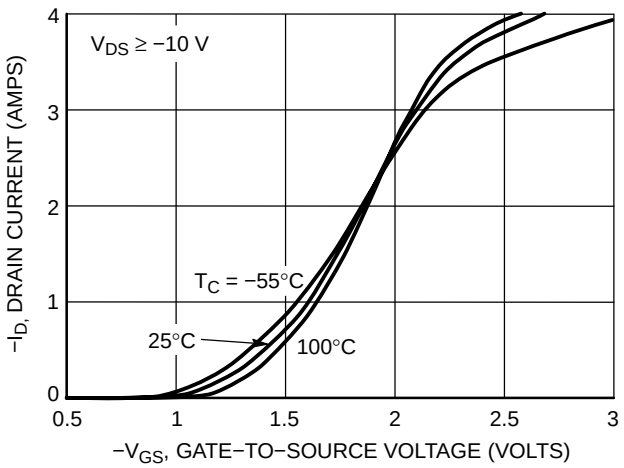



**Figure 2. Transfer Characteristics**

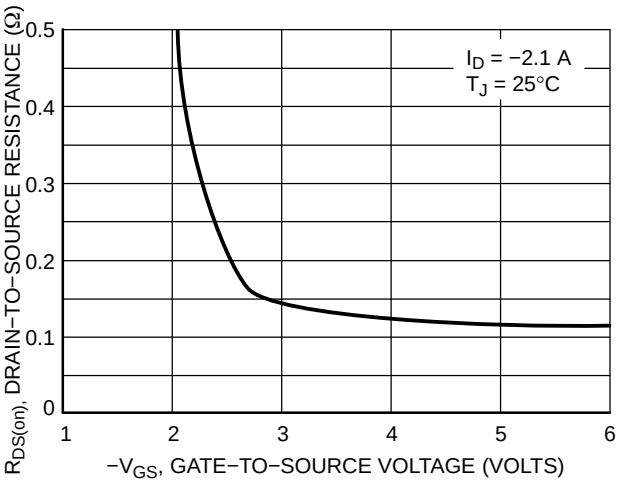



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

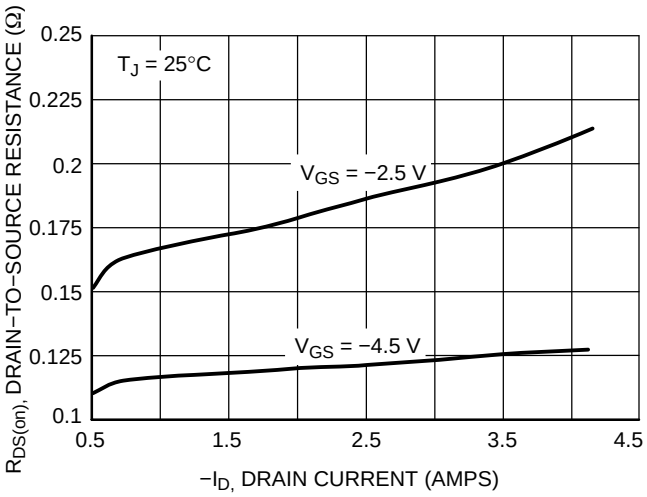



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

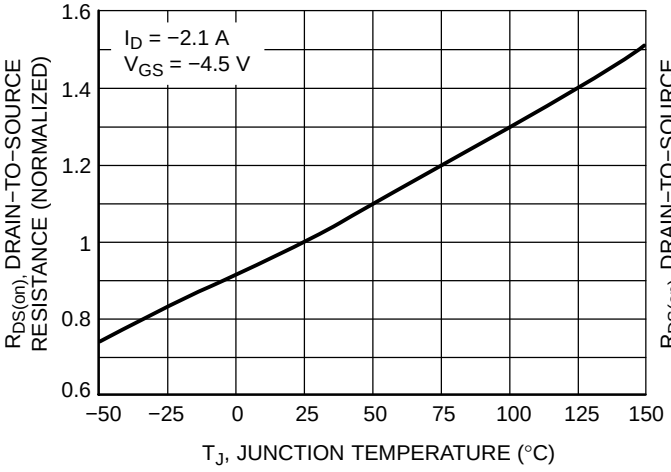



**Figure 5. On−Resistance Variation with Temperature**

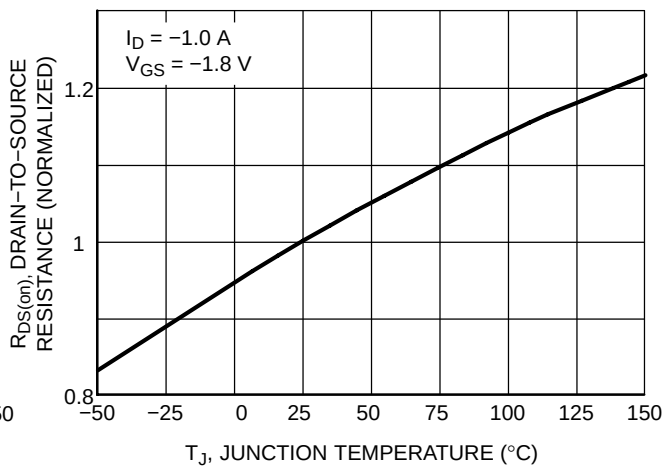



**Figure 6. On−Resistance Variation with Temperature**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

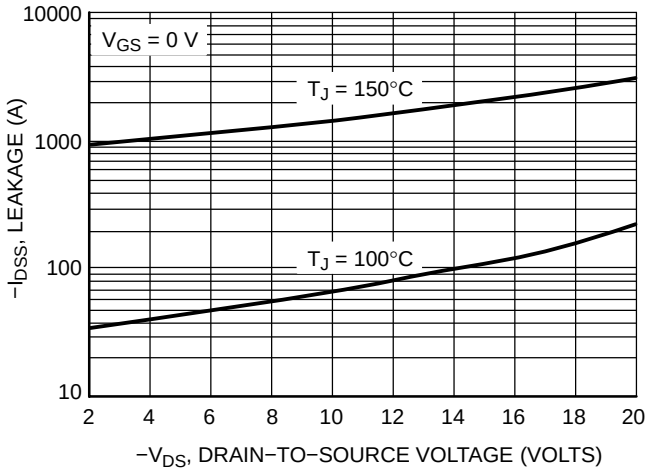



**Figure 7. Drain−to−Source Leakage Current vs. Voltage**

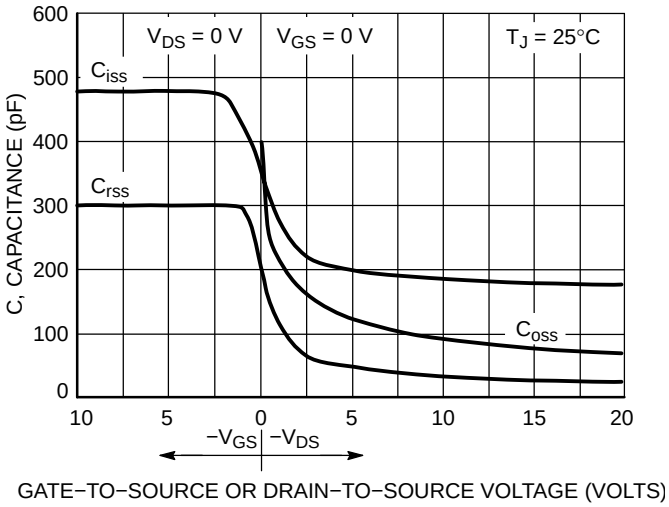



**Figure 8. Capacitance Variation**

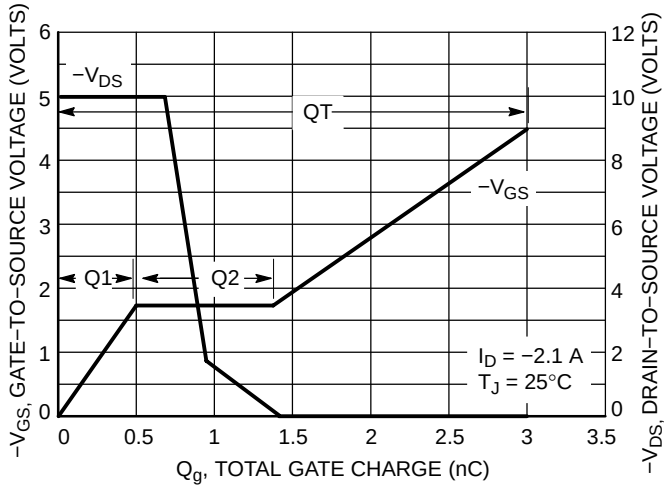



**Figure 9. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

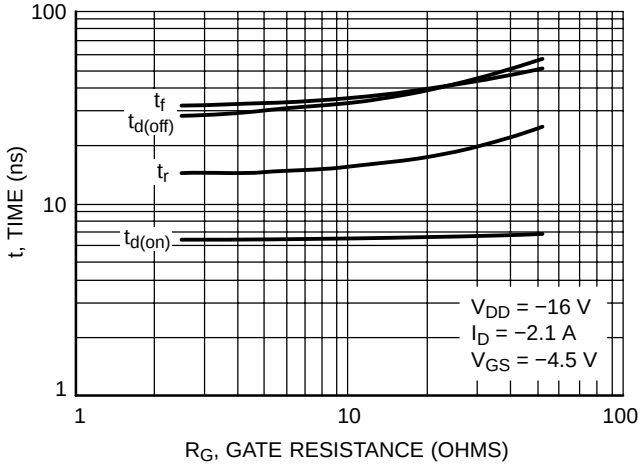



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

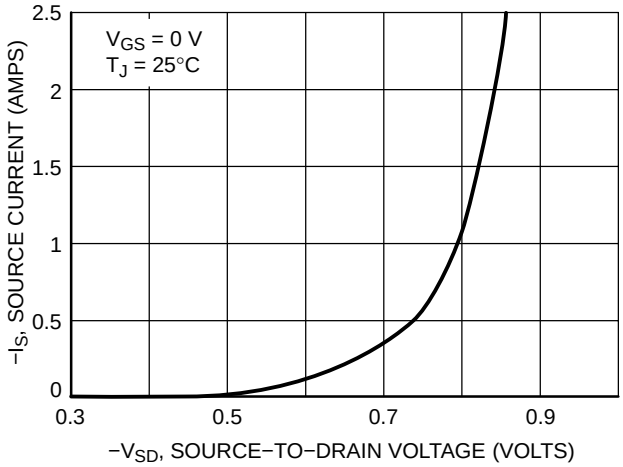



**Figure 11. Diode Forward Voltage vs. Current**

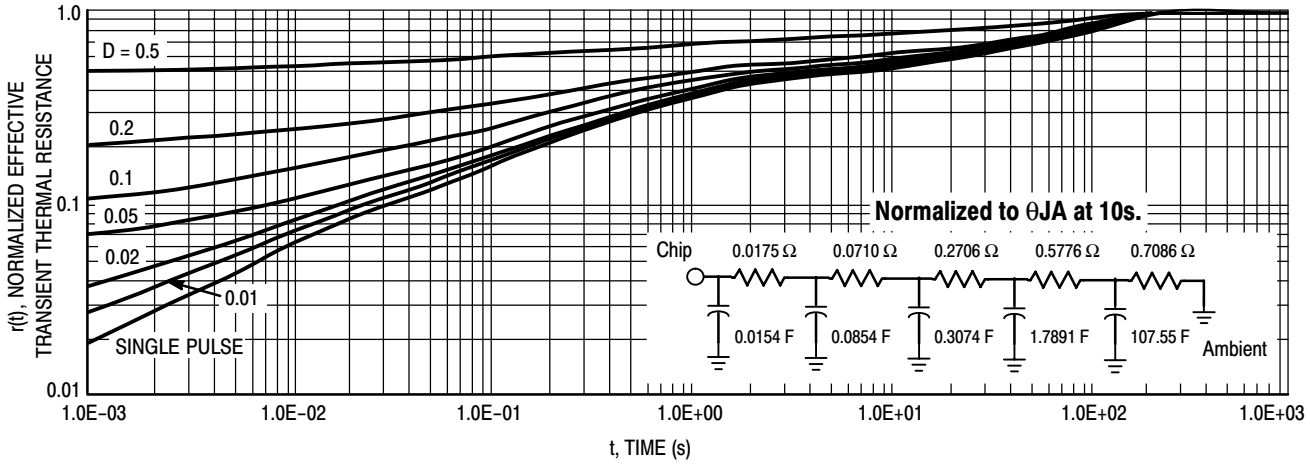



**Figure 12. Thermal Response**

## SOLDERING FOOTPRINT*

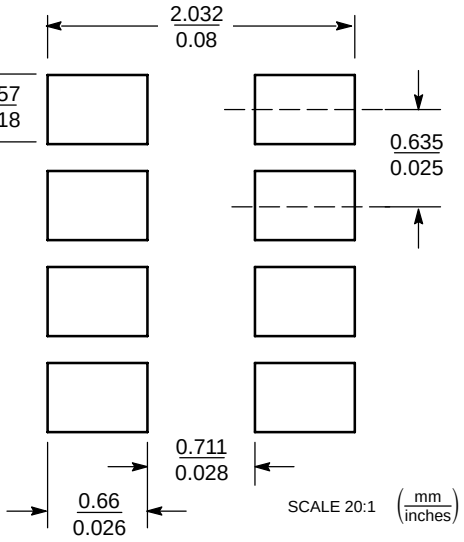



**Figure 13. Basic**

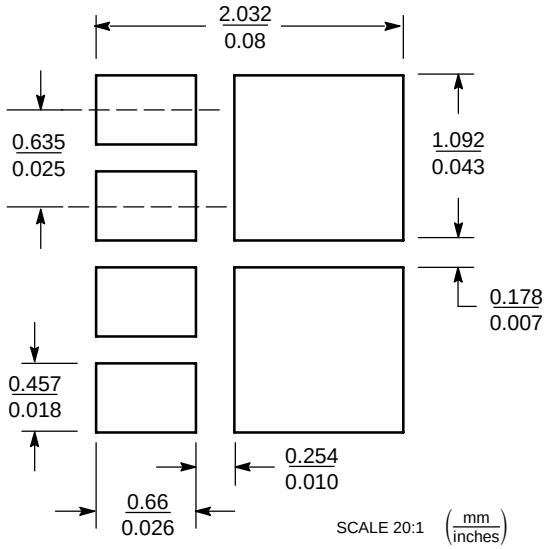



**Figure 14. Style 2**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

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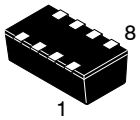
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

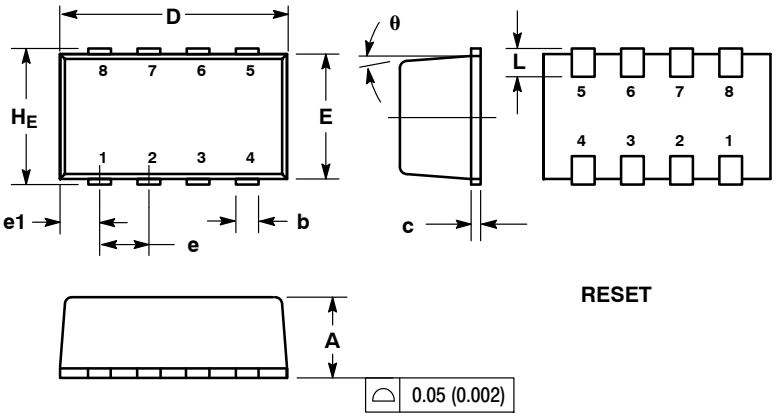
ON Semiconductor®

**ChipFET™**
CASE1206A−03
ISSUE K

DATE 19 MAY 2009




**SCALE 1:1**




**RESET**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.00 | 1.05 | 1.10 | 0.039 | 0.041 | 0.043 |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 |
| c | 0.10 | 0.15 | 0.20 | 0.004 | 0.006 | 0.008 |
| D | 2.95 | 3.05 | 3.10 | 0.116 | 0.120 | 0.122 |
| E | 1.55 | 1.65 | 1.70 | 0.061 | 0.065 | 0.067 |
| e | 0.65 BSC | | | 0.025 BSC | | |
| e1 | 0.55 BSC | | | 0.022 BSC | | |
| L | 0.28 | 0.35 | 0.42 | 0.011 | 0.014 | 0.017 |
| $H_E$ | 1.80 | 1.90 | 2.00 | 0.071 | 0.075 | 0.079 |
| θ | 5° NOM | | | 5° NOM | | |

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

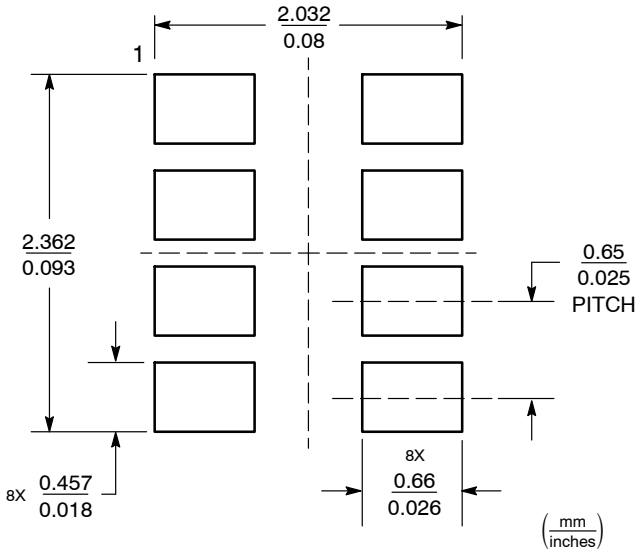
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

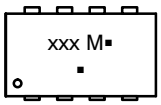
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

### SOLDERING FOOTPRINT




**Basic Style**

### GENERIC MARKING DIAGRAM*




xxx = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

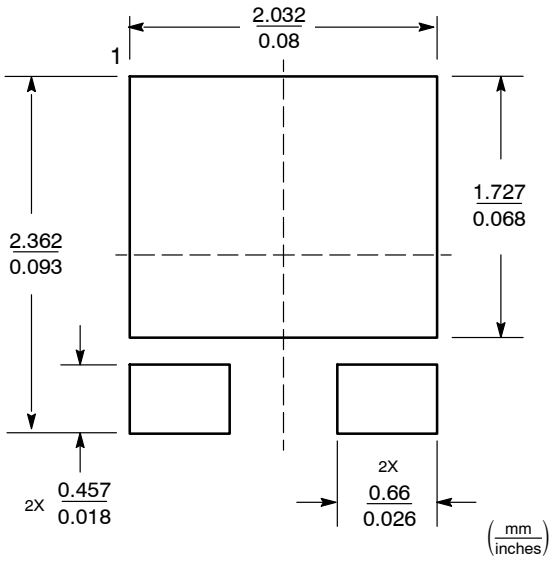
**OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2**

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON03078D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **ChipFET** | **PAGE 1 OF 2** |

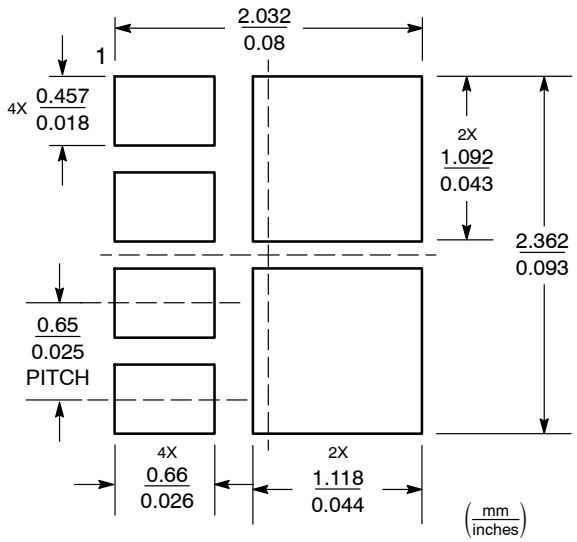
**ChipFET™**
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

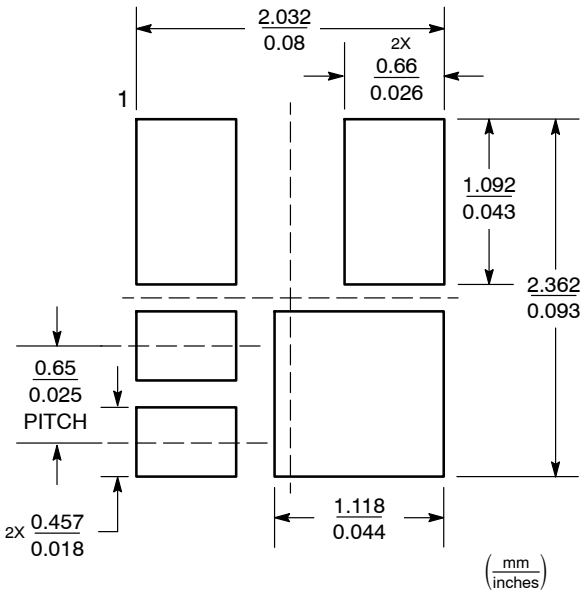
**ADDITIONAL SOLDERING FOOTPRINTS***



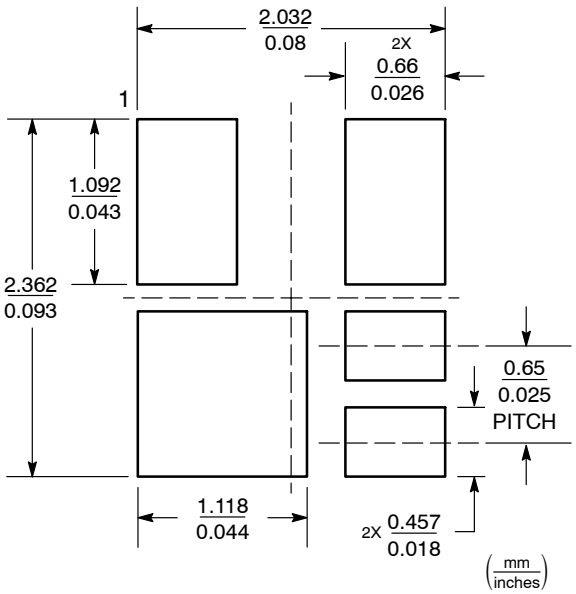

**Styles 1 and 4**




**Style 2**




**Style 3**




**Style 5**

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **ChipFET** | **PAGE 2 OF 2** |

## PUBLICATION ORDERING INFORMATION

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**onsemi Website:** www.onsemi.com

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Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊