

NTHD4401P

Power MOSFET

-20 V, -3.0 A, Dual P-Channel, ChipFET™

Features

- Low $R_{DS(on)}$ and Fast Switching Speed in a ChipFET Package
- Leadless ChipFET Package 40% Smaller Footprint than TSOP-6
- ChipFET Package with Excellent Thermal Capabilities where Heat Transfer is Required
- Pb-Free Package is Available

Applications

- Charge Control in Battery Chargers
- Optimized for Battery and Load Management Applications in Portable Equipment
- MP3 Players, Cell Phones, Digital Cameras, PDAs
- Buck and Boost DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	-20	V
Gate-to-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-2.1	A
		$T_A = 85^\circ\text{C}$	-1.5	
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	-3.0	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.1	W
		$T_A = 85^\circ\text{C}$	0.6	
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	2.1	
Pulsed Drain Current	$tp = 10\ \mu\text{s}$	I_{DM}	-9.0	A
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	-2.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Rating	Symbol	Value	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	110	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 5\text{ s}$		60	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

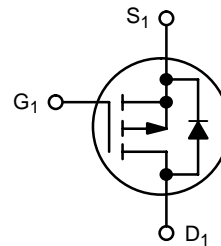
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).



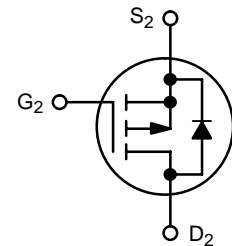
ON Semiconductor®

<http://onsemi.com>

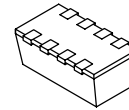
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-20 V	130 m Ω @ -4.5 V	-3.0 A
	200 m Ω @ -2.5 V	



P-Channel MOSFET

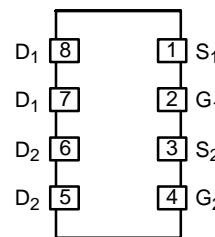


P-Channel MOSFET

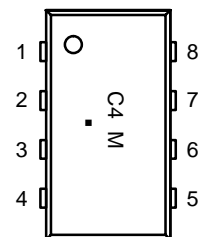


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



- C4 = Specific Device Code
- M = Month Code
- = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4401PT1	ChipFET	3000/Tape & Reel
NTHD4401PT1G	ChipFET (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTHD4401P

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(Br)DSS}	V _{GS} = 0 V, I _D = -250 μA	-20	-23		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(Br)DSS} /T _J			-8.0		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, T _J = 25°C			-1.0	μA
		V _{DS} = -16 V, T _J = 85°C			-5.0	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.6	-0.75	-1.2	V
Gate Threshold Temperature Coefficient	V _{GS(th)} /T _J			2.65		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -2.1 A V _{GS} = -2.5 V, I _D = -1.7 A V _{GS} = -1.8 V, I _D = -1.0 A		0.130 0.200 0.34	0.155 0.240	Ω
Forward Transconductance	g _{FS}	V _{DS} = -10 V, I _D = -2.1 A		5.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -10 V		185	300	pF
Output Capacitance	C _{oss}			95	150	
Reverse Transfer Capacitance	C _{rss}			30	50	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -10 V, I _D = -2.1 A		3.0	6.0	nC
Threshold Gate Charge	Q _{G(TH)}			0.2		
Gate-to-Source Charge	Q _{GS}			0.5		
Gate-to-Drain Charge	Q _{GD}			0.9		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DD} = -16 V, I _D = -2.1 A, R _G = 2.5 Ω		7.0	12	ns
Rise Time	t _r			13	25	
Turn-Off Delay Time	t _{d(off)}			33	50	
Fall Time	t _f			27	40	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V I _S = -2.5 A		-0.85	-1.15	V
Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _S /dt = 90 A/μs, I _S = -2.1 A		32		ns
Charge Time	t _a			10		
Discharge Time	t _b			22		
Reverse Recovery Charge	Q _{RR}			15		

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

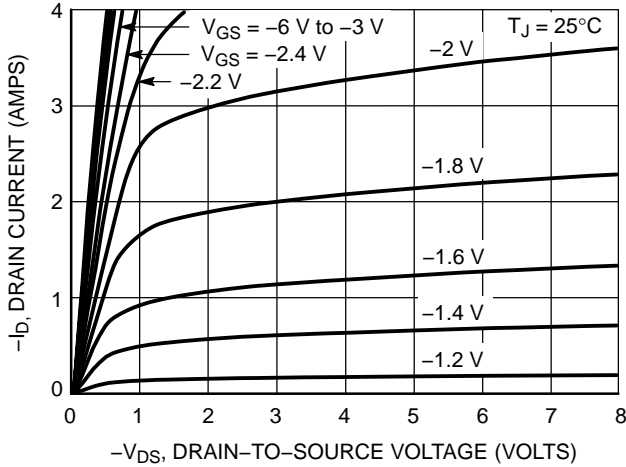


Figure 1. On-Region Characteristics

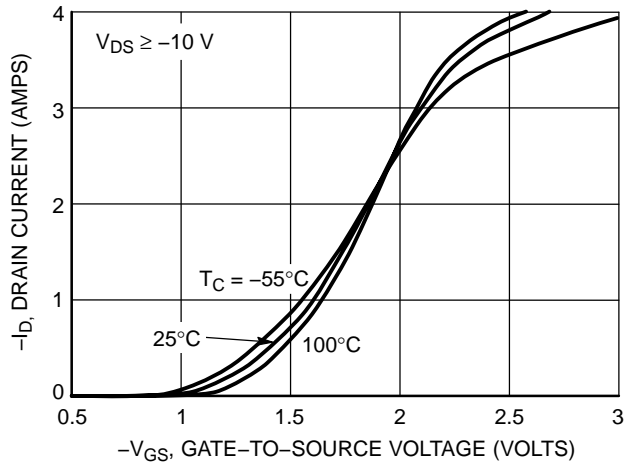


Figure 2. Transfer Characteristics

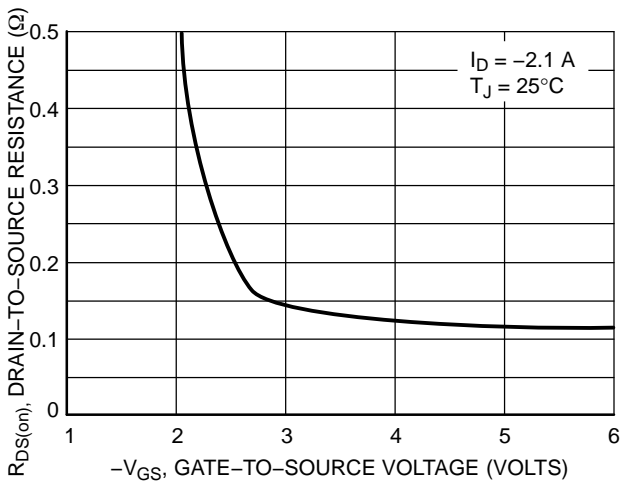


Figure 3. On-Resistance vs. Gate-to-Source Voltage

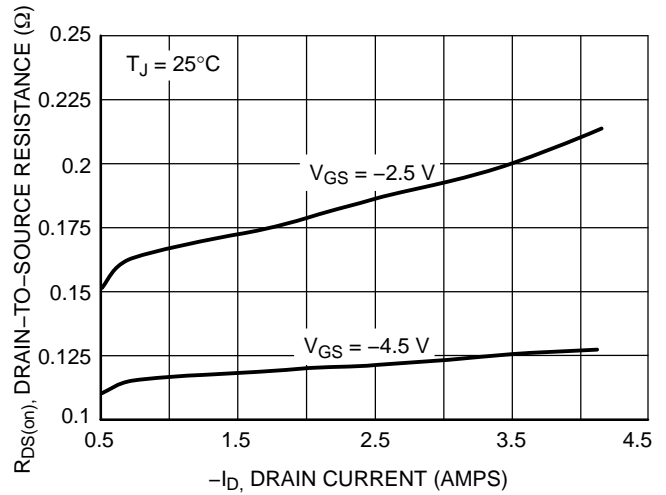


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

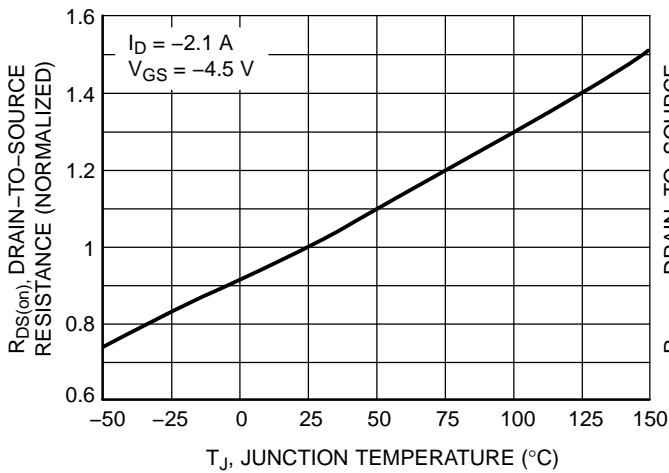


Figure 5. On-Resistance Variation with Temperature

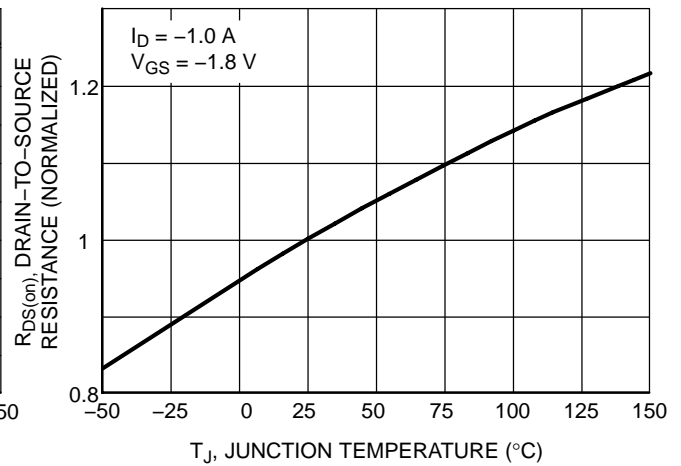


Figure 6. On-Resistance Variation with Temperature

NTHD4401P

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

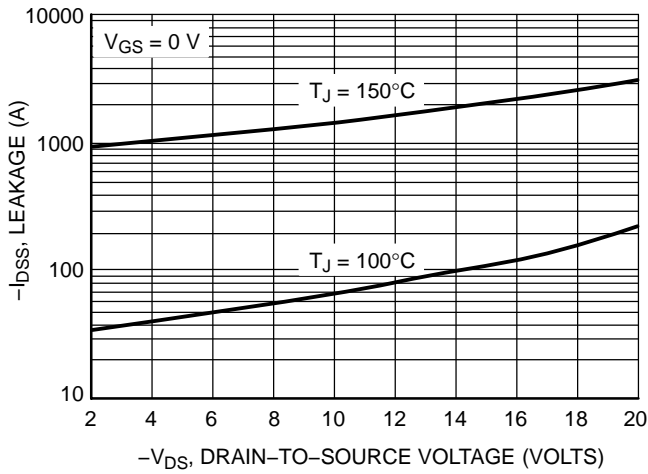


Figure 7. Drain-to-Source Leakage Current vs. Voltage

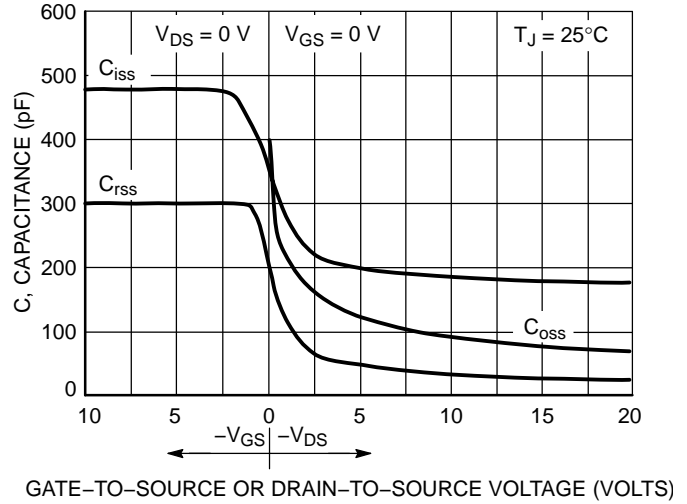


Figure 8. Capacitance Variation

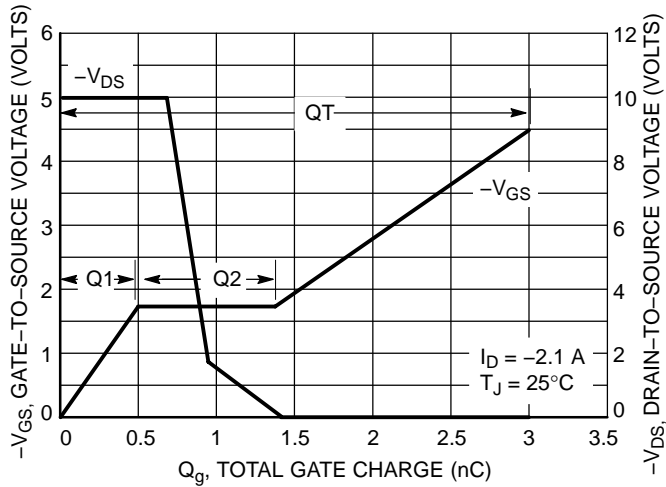


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

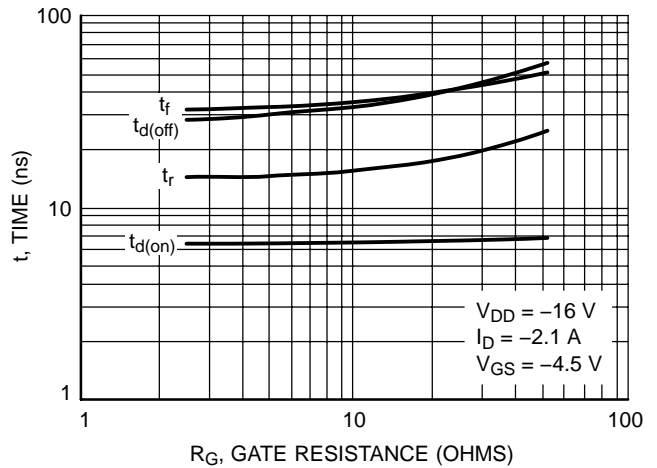


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

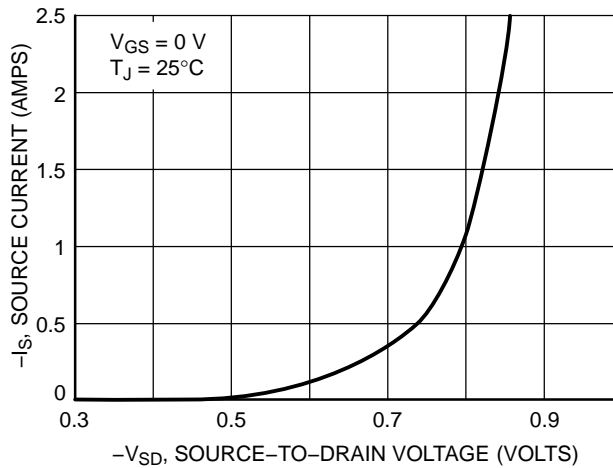


Figure 11. Diode Forward Voltage vs. Current

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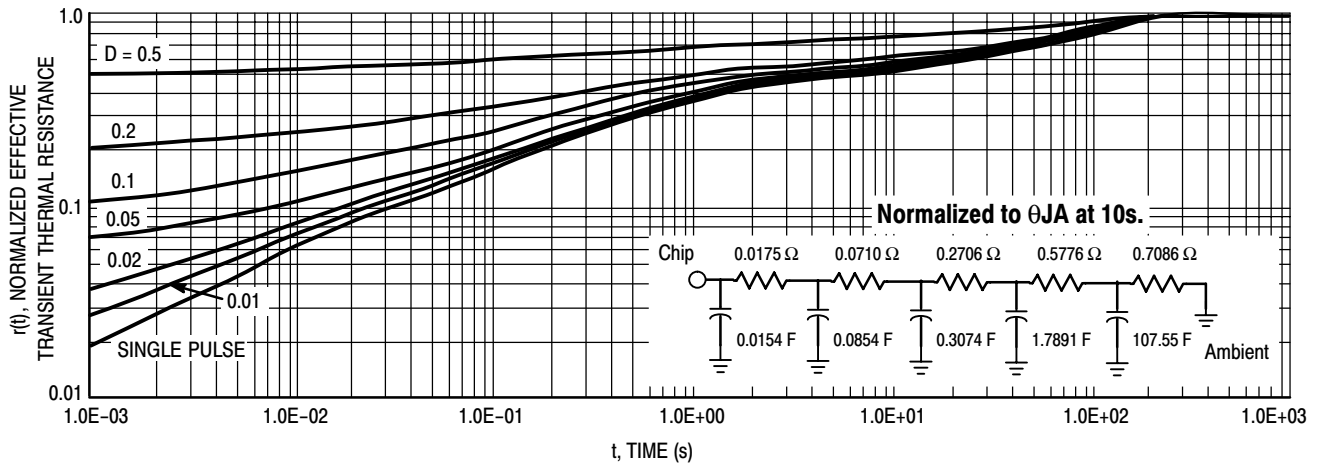


Figure 12. Thermal Response

SOLDERING FOOTPRINT*

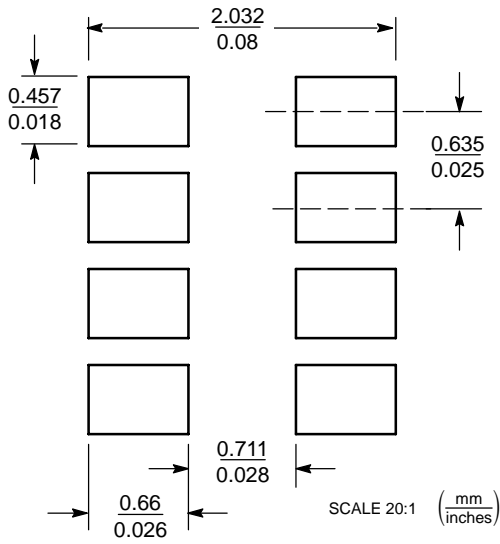


Figure 13. Basic

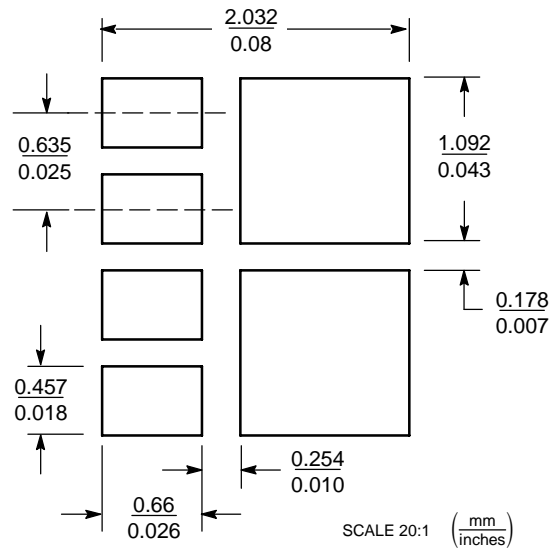


Figure 14. Style 2

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 5, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0019 sq. in. (or 1.22 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



ChipFET™ CASE1206A-03 ISSUE K

DATE 19 MAY 2009

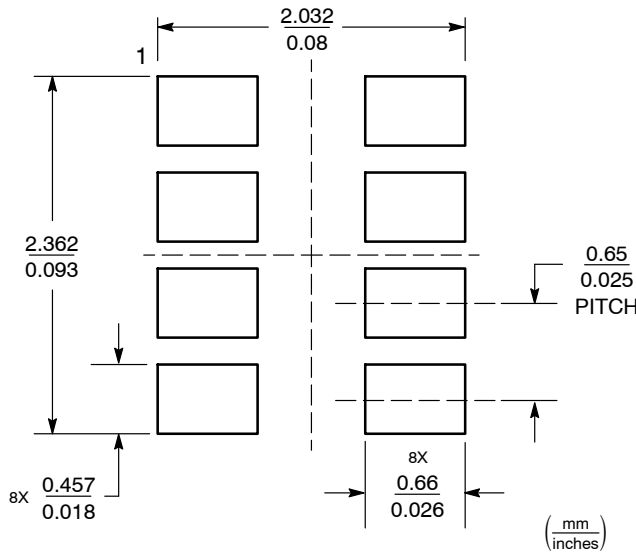


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

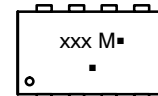
- | | | | | | |
|--------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|
| STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN | STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1 | STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE | STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR | STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE | STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN |
|--------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



- xxx = Specific Device Code
 - M = Month Code
 - = Pb-Free Package
- (Note: Microdot may be in either location)

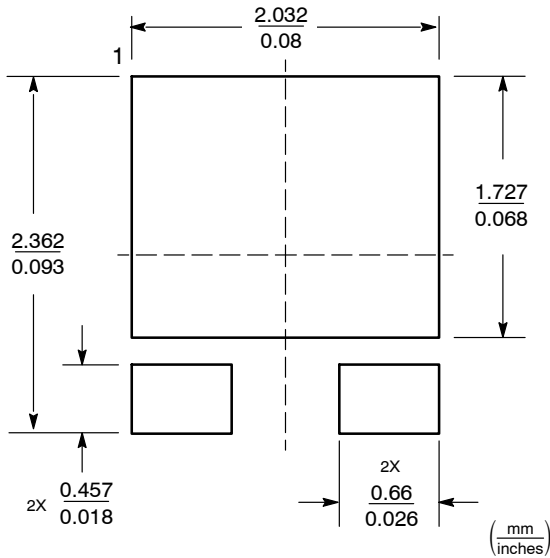
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

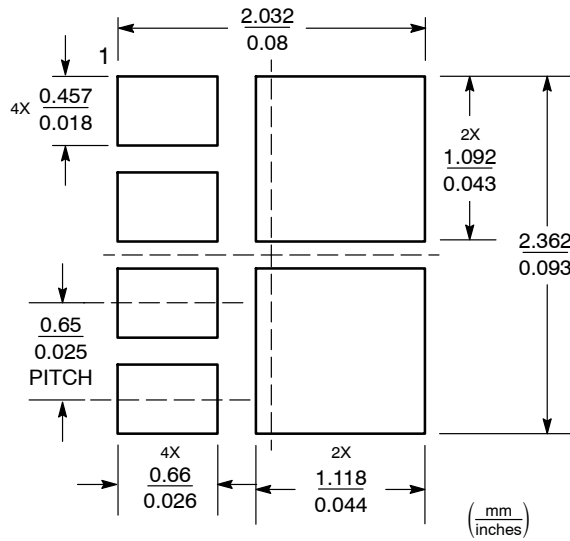
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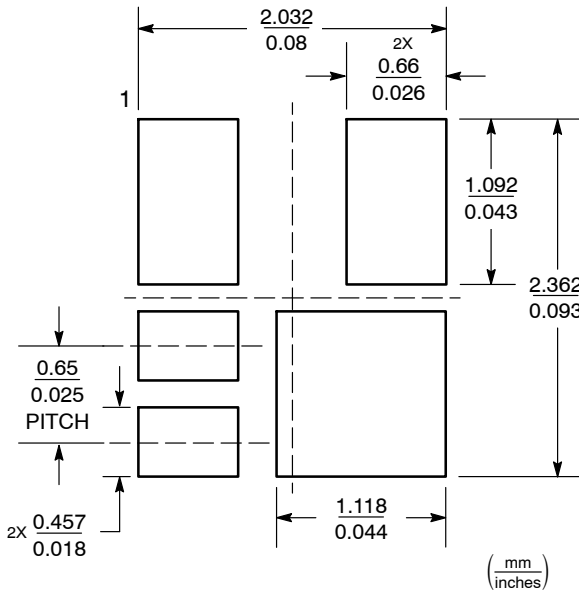
ADDITIONAL SOLDERING FOOTPRINTS*



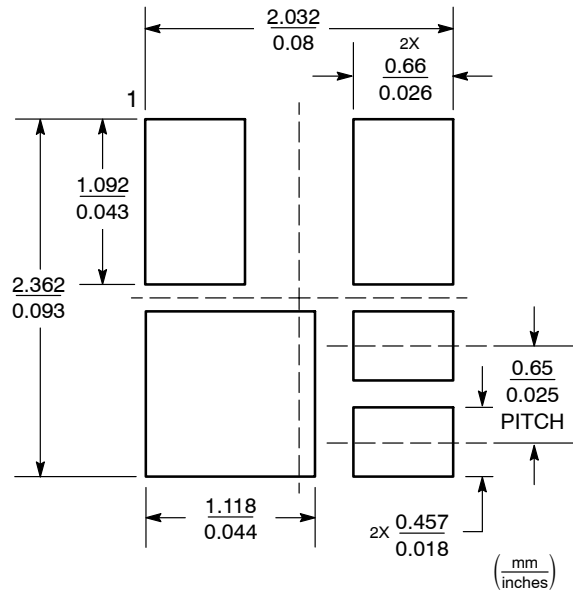
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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