MOSFET - POWERTRENCH®
N-Channel
80 V, 300 A, 1.4 mΩ

FDBL86361-F085

Features

- Typical $R_{DS(on)}$ = 1.1 mΩ at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 172 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain−to−Source Voltage	80	V
V_{GS}	Gate−to−Source Voltage	±20	V
I_D	Drain Current − Continuous (V_{GS} = 10), T_C = 25°C (Note 1)	300	A
	Pulsed Drain Current, T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	820	mJ
P_D	Power Dissipation	429	W
	Derate Above 25°C	2.86	W/°C
T_J, T_{STG}	Operating and Storage Temperature	−55 to +175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.
2. Starting T_J = 25°C, L = 0.4 mH, I_{AS} = 64 A, V_{DD} = 40 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

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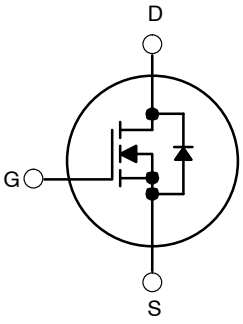
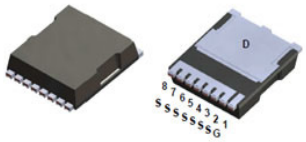


N−Channel



H−PSOF8L
CASE 100CU

MARKING DIAGRAM

$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FDBL86361	= Specific Device Code

ORDERING INFORMATION

Device	Top Mark	Package	Shipping†
FDBL86361−F085	FDBL86361	H−PSOF8L	2000 Units/ Tape&Reel

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		80	–	–	V
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 80 V, V_{GS} = 0 V	T_J = 25°C	–	–	1	μA
			T_J = 175°C (Note 4)	–	–	1	mA
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0	3.0	4.0	V
$R_{DS(on)}$	Drain to Source on Resistance	I_D = 80 A, V_{GS} = 10 V	T_J = 25°C	–	1.1	1.4	mΩ
			T_J = 175°C (Note 4)	–	2.4	3.1	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz		–	12800	–	pF
C_{oss}	Output Capacitance			–	1925	–	pF
C_{rss}	Reverse Transfer Capacitance			–	139	–	pF
R_g	Gate Resistance	f = 1 MHz		–	2.7	–	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V	V_{DD} = 64 V	–	172	188	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2 V	I_D = 80 A	–	23	27	nC
Q_{gs}	Gate−to−Source Gate Charge			–	51	–	nC
Q_{gd}	Gate−to−Drain “Miller” Charge			–	34	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 40 V, I_D = 80 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		–	–	128	ns
$t_{d(on)}$	Turn−On Delay			–	42	–	ns
t_r	Rise Time			–	73	–	ns
$t_{d(off)}$	Turn−Off Delay			–	87	–	ns
t_f	Fall Time			–	48	–	ns
t_{off}	Turn−Off Time			–	–	193	ns
DRAIN−SOURCE DIODE CHARACTERISTIC							
V_{SD}	Source−to−Drain Diode Voltage	I_{SD} = 80 A, V_{GS} = 0 V		–	–	1.25	V
		I_{SD} = 40 A, V_{GS} = 0 V		–	–	1.2	V
t_{rr}	Reverse−Recovery Time	I_F = 80 A, dI_{SD}/dt = 100 A/μs, V_{DD} = 64 V		–	117	136	ns
Q_{rr}	Reverse−Recovery Charge			–	205	269	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

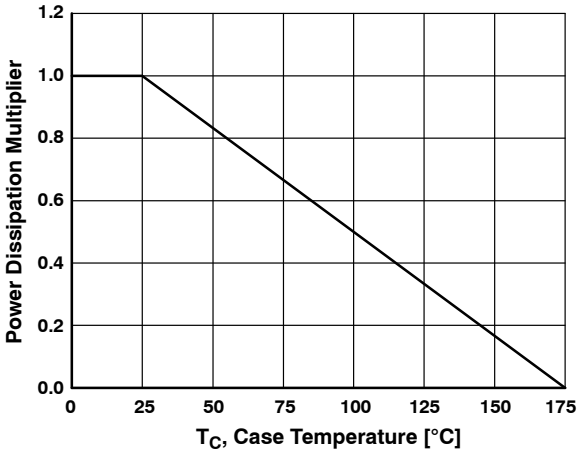


Figure 1. Normalized Power Dissipation vs. Case Temperature

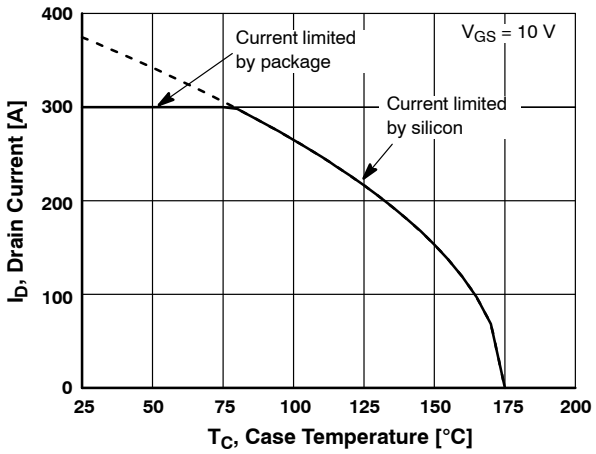


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

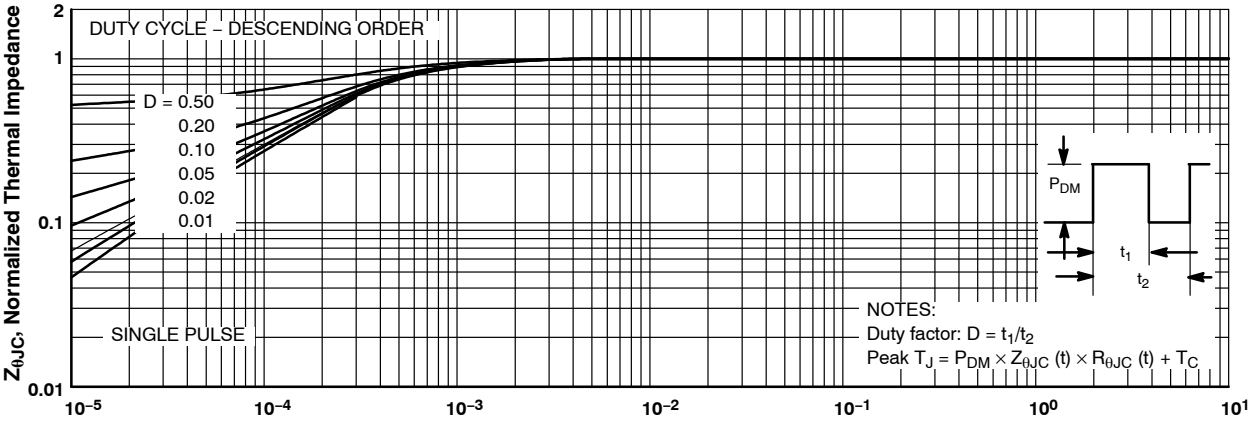


Figure 3. Normalized Maximum Transient Thermal Impedance

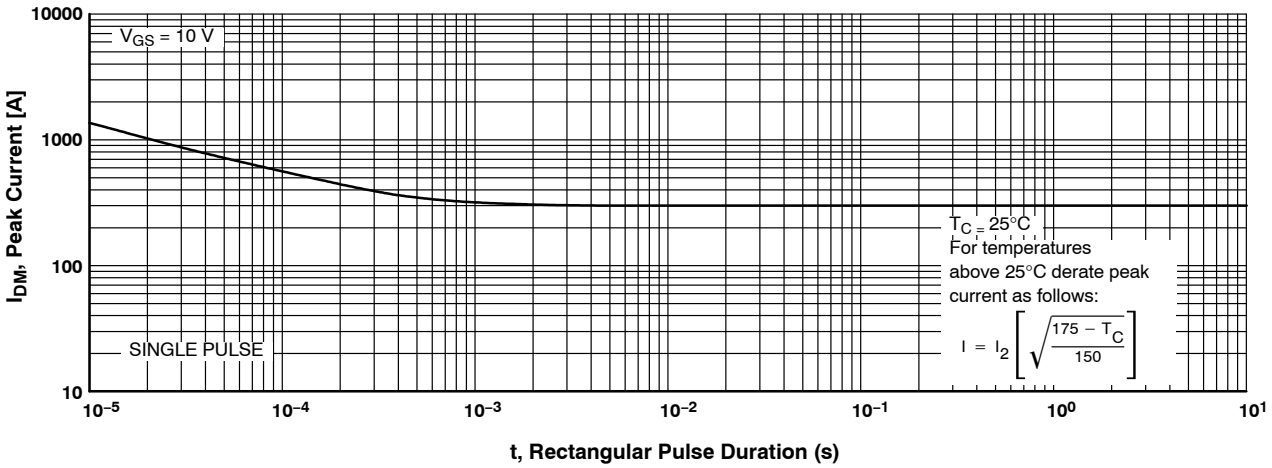


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

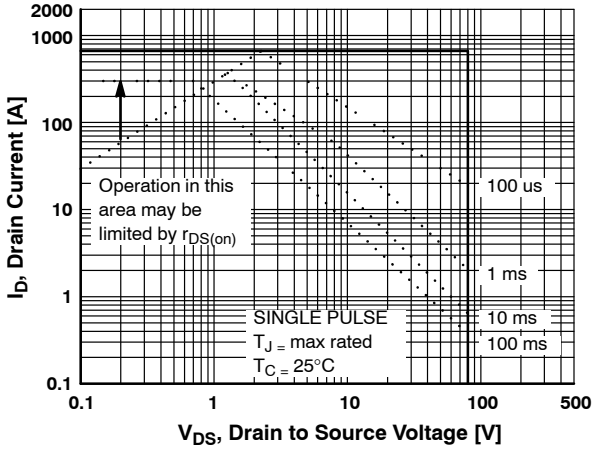
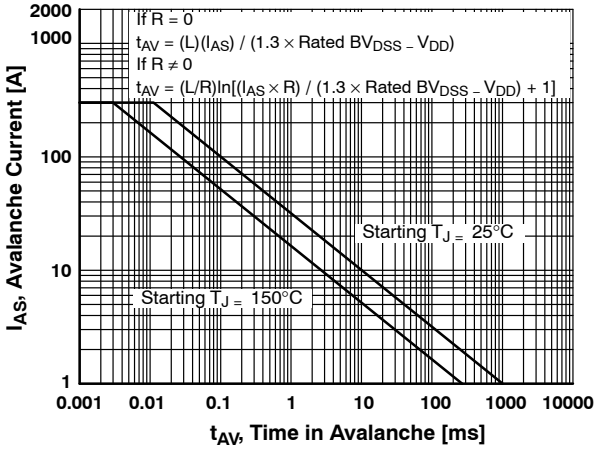


Figure 5. Forward Bias Safe Operating Area



Refer to ON Semiconductor Application Notes AN7514 and AN7515.

Figure 6. Unclamped Inductive Switching Capability

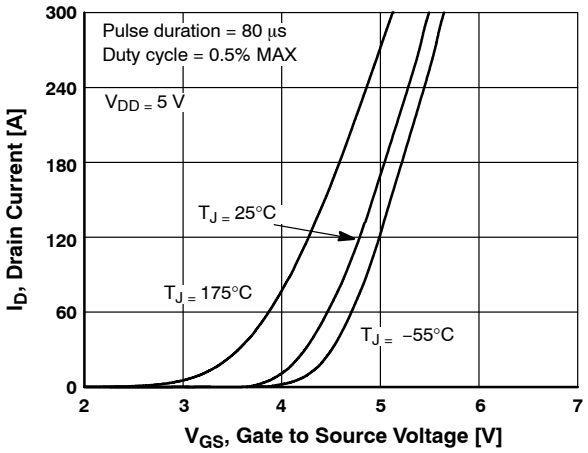


Figure 7. Transfer Characteristics

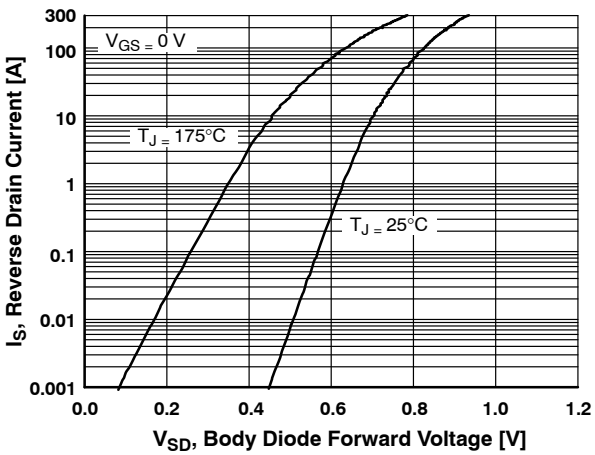


Figure 8. Forward Diode Characteristics

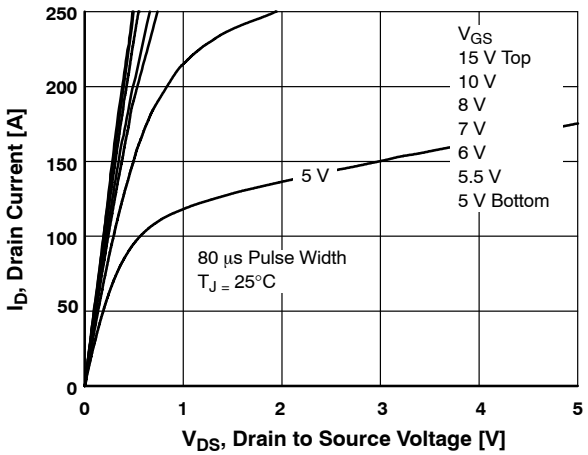


Figure 9. Saturation Characteristics

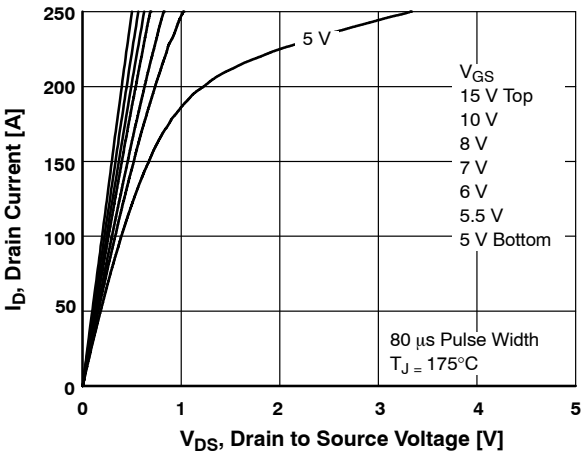


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

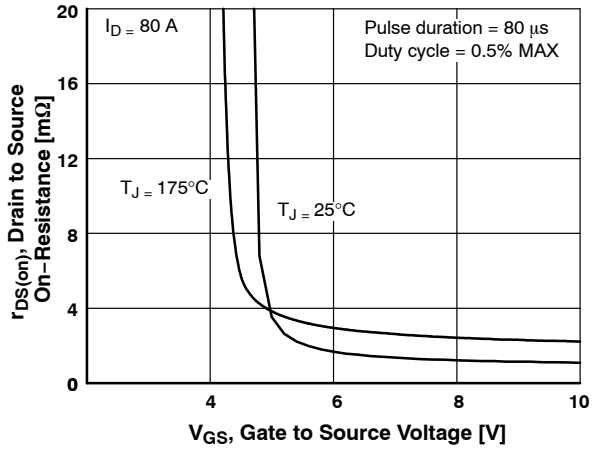


Figure 11. R_{DSON} vs. Gate Voltage

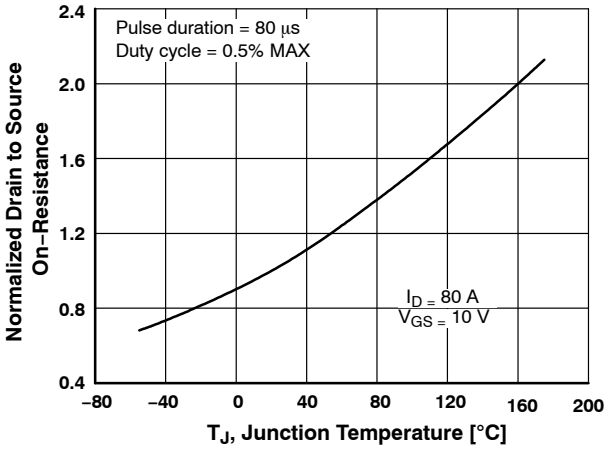


Figure 12. Normalized R_{DSON} vs. Junction Temperature

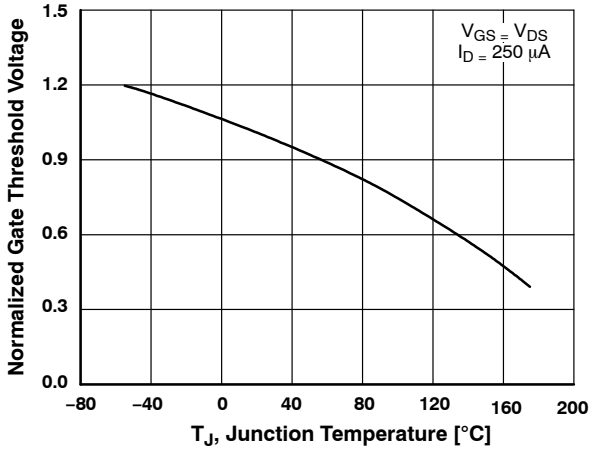


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

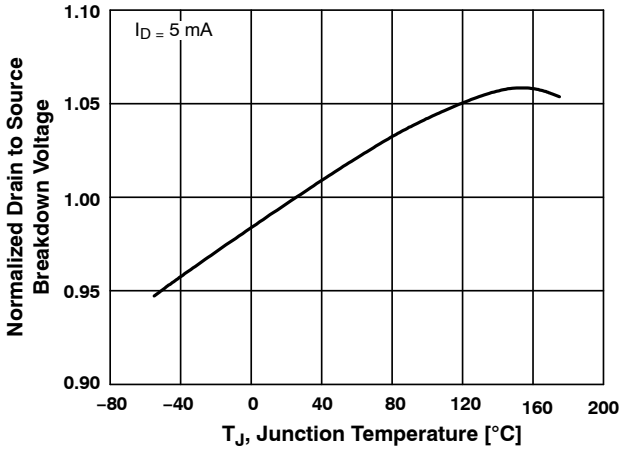


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

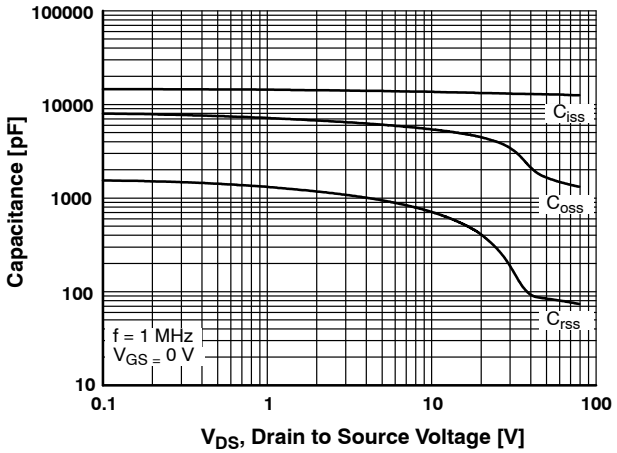


Figure 15. Capacitance vs. Drain to Source Voltage

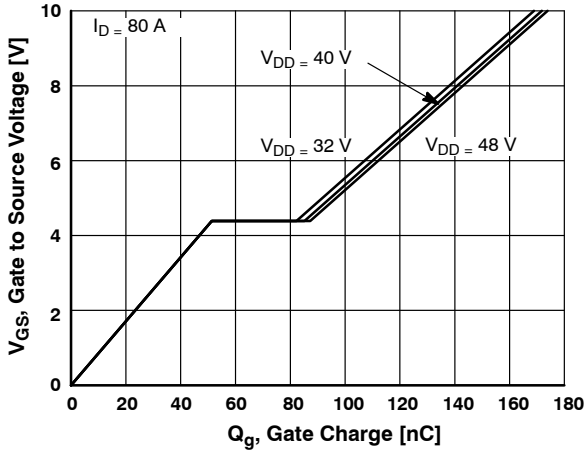
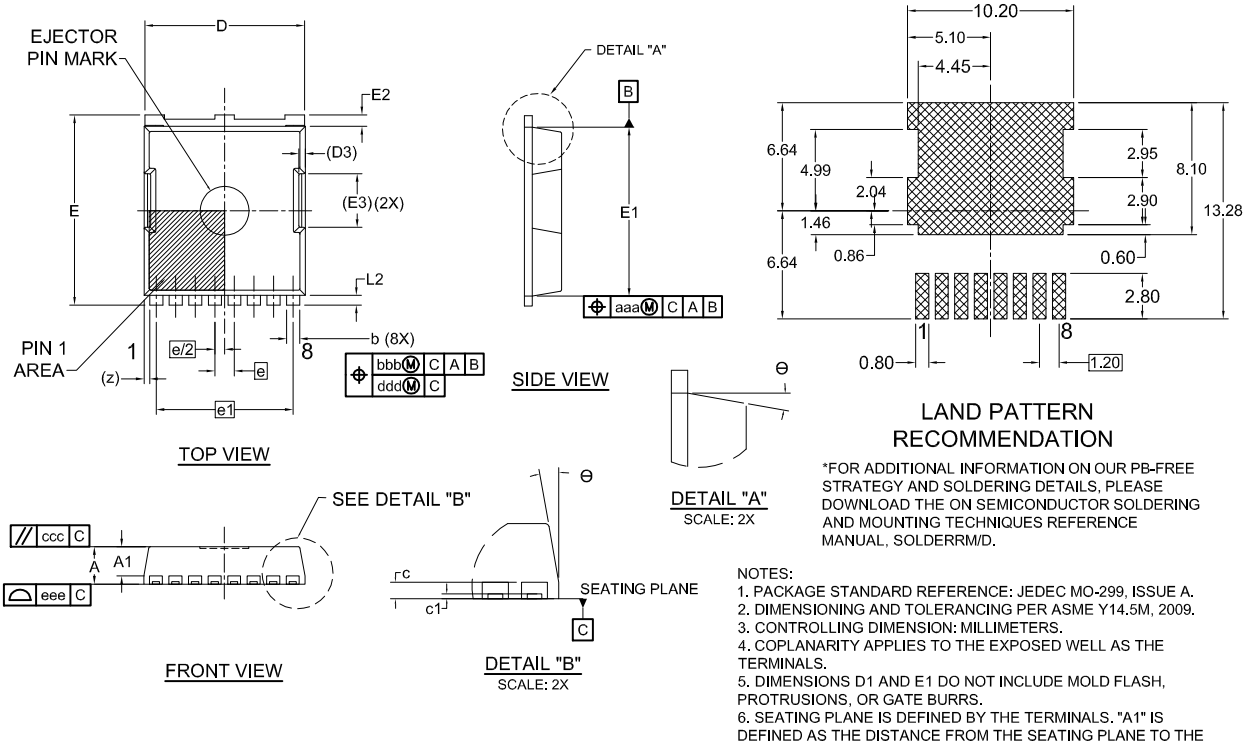


Figure 16. Gate Charge vs. Gate to Source Voltage

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

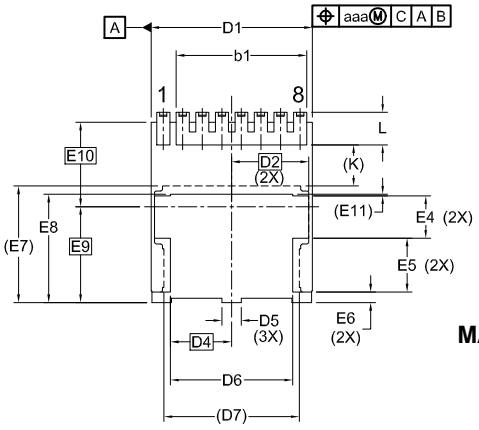
H−PSOF8L 11.68x9.80
CASE 100CU
ISSUE B

DATE 20 MAY 2022



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

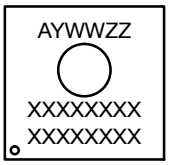
NOTES:
1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1		8.00 REF	
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2		4.73 BSC	
D3		0.40 REF	
D4		3.75 BSC	
D5	---	1.20	---
D6	7.40	7.50	7.60
D7		8.30 REF	
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3		3.30 REF	
E4	---	2.60	---
E5	---	3.30	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	—	0.65	---
E7		7.15 REF	
E8	6.55	6.65	6.75
E9		5.89 BSC	
E10		5.19 BSC	
E11		0.10 REF	
e		1.20 BSC	
e/2		0.60 BSC	
e1		8.40 BSC	
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z		0.35 REF	
θ	0°	---	12°
aaa		0.20	
bbb		0.25	
ccc		0.20	
ddd		0.20	
eee		0.10	

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**H−PSOF8L 11.68x9.80**	**PAGE 1 OF 1**

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