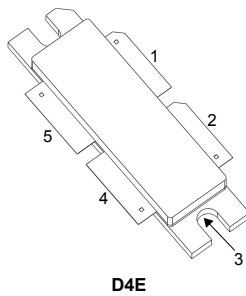


700 W, 40 V, HF to 1 GHz RF power LDMOS transistor



D4E

Pin connection	
Pin	Connection
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF4L10700CB4	915 MHz	40 V	700 W	15 dB	69%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched pair transistors in push-pull configuration
- Large positive and negative gate-source voltage range for improved class C operation
- Optimized for Doherty applications
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- ISM
- RF energy

Description

The RF4L10700CB4 is a 700 W, 40 V, high performance, internally matched LDMOS FET, designed for multiple ISM and RF energy applications up to 1 GHz frequency range. It can be used in class AB, B or C for both CW and pulse applications in narrow-band operation. It is qualified up to 40 V operation.



Product status link

[RF4L10700CB4](#)

Product summary

Order code	RF4L10700CB4
Marking	4L10700
Package	D4E
Packing	Tray
Base/bulk quantity	20/100

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	95	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	42	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.16	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_{DS} = 100\ \mu\text{A}$	95	-		V
I_{DSS}	Zero gate voltage drain leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 42\text{ V}$		-	1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 75\text{ V}$		-		
I_{GSS}	Gate-source leakage current	$V_{GS} = -8/10\text{ V}, V_{DS} = 0\text{ V}$		-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 40\text{ V}, I_{DS} = 600\ \mu\text{A}$	1.75	-	2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}, I_{DS} = 100\text{ mA}$	2	-	5	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}, I_{DS} = 6\text{ A}$		-	1	V
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$		-	2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$		-	1	Ω

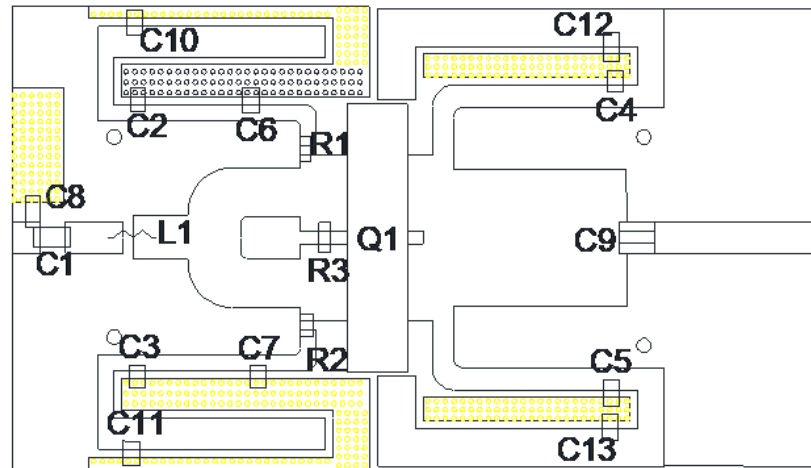
Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$f = 915\text{ MHz}, \text{pulsed CW},$ 1 dB compression	-	700		W
G_{PS}	Power gain		-	15		dB
η_D	Drain efficiency		-	69		%
VSWR	Load mismatch	$P_{OUT} = 700\text{ W}, \text{all phases}$	-		10:1	

Note: $V_{DD} = 40\text{ V}, I_{DQ} = 100\text{ mA}, \text{pulse width} = 100\ \mu\text{s}, \text{duty cycle} = 10\%$.

3 Test circuits

Figure 1. Test circuit layout



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Table 6. Components list

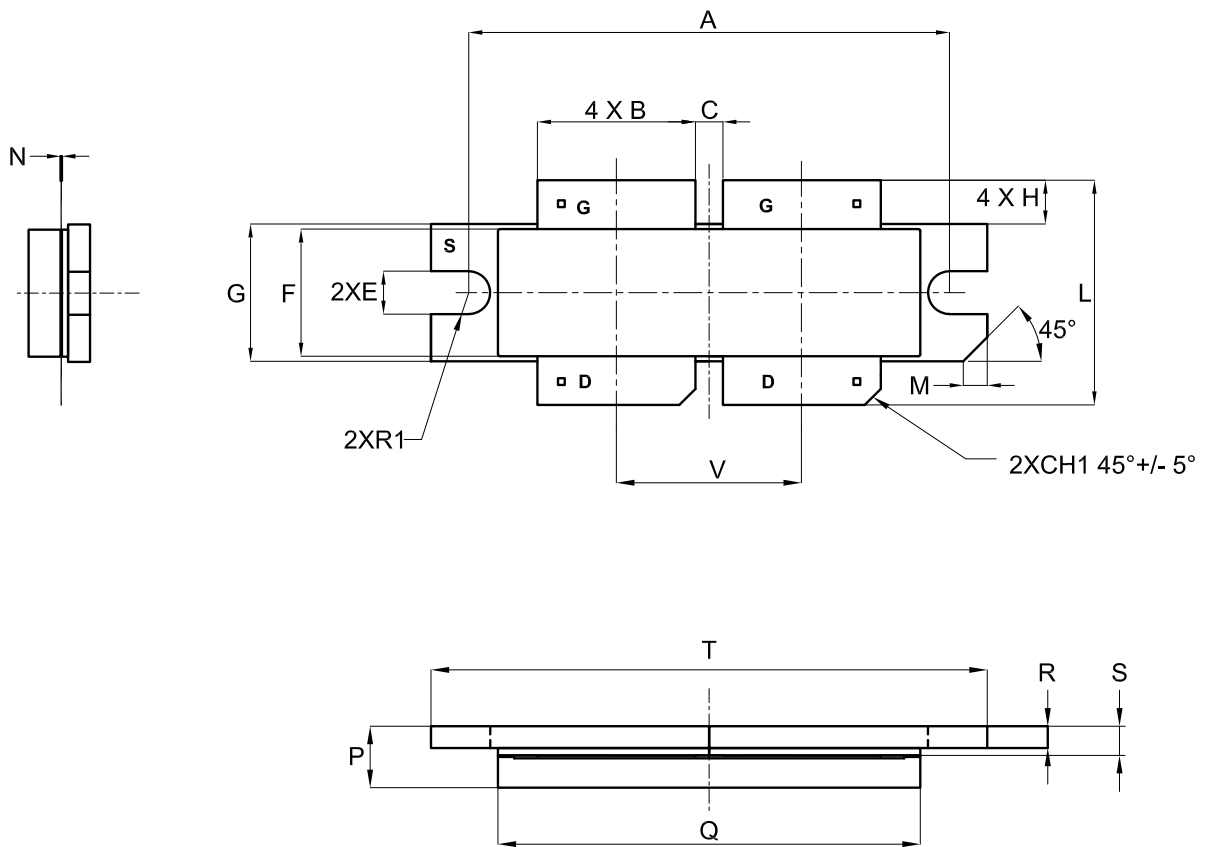
Component	Value	Size	Reference
C1, C2, C3, C4, C5	56 pF		ATC800B
C6, C7	47 pF		ATC800B
C8	1 pF	0805	ATC800B
C9	18 pF (3x)		ATC800B
C10, C11	10 μ F	1210	Ceramic multilayer capacitor
C11, C12	1000 μ F		50V electrolytic capacitor
L1	0.5 turns		Φ 1 mm varnished wire
R1, R2, R3	10 Ω	0603	chip resistor
PCB		Taconic RF-60TC 25 mils	

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D4E package information

Figure 2. D4E package outline



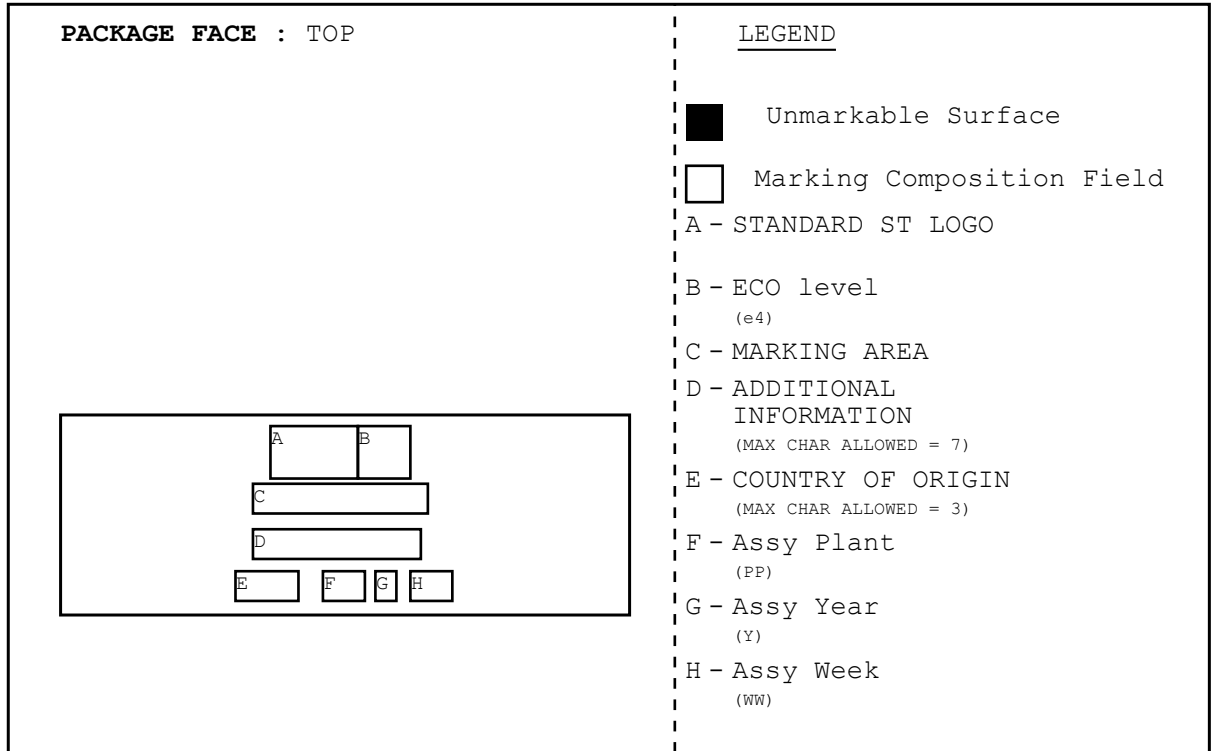
DM0066713_2

Table 7. D4E package mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	35.44	35.56	35.68
B	11.56	11.68	11.80
C	1.92	2.04	2.16
E	3.06	3.18	3.30
F	9.25	9.40	9.50
G	10.04	10.16	10.28
H	5.72	5.85	3.48
L	16.11	16.62	17.13
M	1.51	1.78	2.05
N	0.10	0.13	0.16
P	4.17	4.55	4.93
Q	30.96	31.24	31.52
R	1.55	1.62	1.69
S	2.09	2.16	2.23
T	41.08	41.22	
V	13.60	13.72	13.84
R1		1.59	
CH1		1.19	

4.2 Marking information

Figure 3. Marking composition



GADG040220211644GT

Revision history

Table 8. Document revision history

Date	Version	Changes
17-May-2021	1	First release.

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