Darlington Complementary Silicon Power Transistors

. . . designed for general–purpose amplifier and low frequency switching applications.

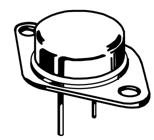
- High DC Current Gain —
  h_{FE} = 3500 (Typ) @ I_C = 5.0 Adc
- Collector–Emitter Sustaining Voltage — @ 100 mA
  $V_{CEO(sus)}$ = 80 Vdc (Min) — 2N6058
  100 Vdc (Min) — 2N6052, 2N6059
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors

PNP
2N6052*

NPN
2N6058
2N6059*

*ON Semiconductor Preferred Device

DARLINGTON
12 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
150 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS (1)

Rating	Symbol	2N6058	2N6052 2N6059	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	12 20		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @T_C = 25°C Derate above 25°C	P_D	150 0.857		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200°C		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Rating	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.17	°C/W

(1) Indicates JEDEC Registered Data.

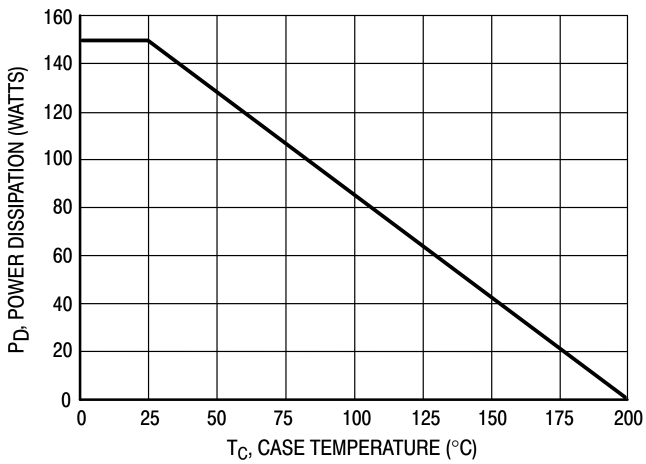


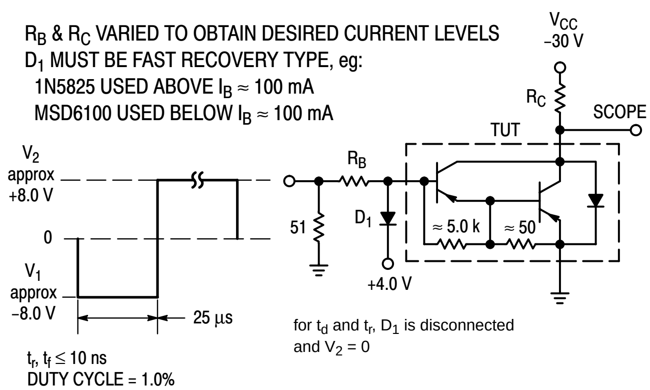
Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

***ELECTRICAL CHARACTERISTICS** (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (2) (I_C = 100 mAdc, I_B = 0)	2N6058 2N6052, 2N6059	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	2N6058 2N6052, 2N6059	I_{CEO}	— —	1.0 1.0	mAdc
Collector Cutoff Current (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CEO}, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)		I_{CEX}	—	0.5 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	—	2.0	mAdc
ON CHARACTERISTICS (2)					
DC Current Gain (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc) (I_C = 12 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750 100	18,000 —	—
Collector–Emitter Saturation Voltage (I_C = 6.0 Adc, I_B = 24 mAdc) (I_C = 12 Adc, I_B = 120 mAdc)		$V_{CE(sat)}$	— —	2.0 3.0	Vdc
Base–Emitter Saturation Voltage (I_C = 12 Adc, I_B = 120 mAdc)		$V_{BE(sat)}$	—	4.0	Vdc
Base–Emitter On Voltage (I_C = 6.0 Adc, V_{CE} = 3.0 Vdc)		$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS					
Magnitude of Common Emitter Small–Signal Short Circuit Forward Current Transfer Ratio (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 MHz)		$\|h_{fe}\|$	4.0	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	2N6052 2N6058/2N6059	C_{ob}	— —	500 300	pF
Small–Signal Current Gain (I_C = 5.0 Adc, V_{CE} = 3.0 Vdc, f = 1.0 kHz)		h_{fe}	300	—	—

*Indicates JEDEC Registered Data.
(2) Pulse test: Pulse Width = 300 μs, Duty Cycle = 2.0%.



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

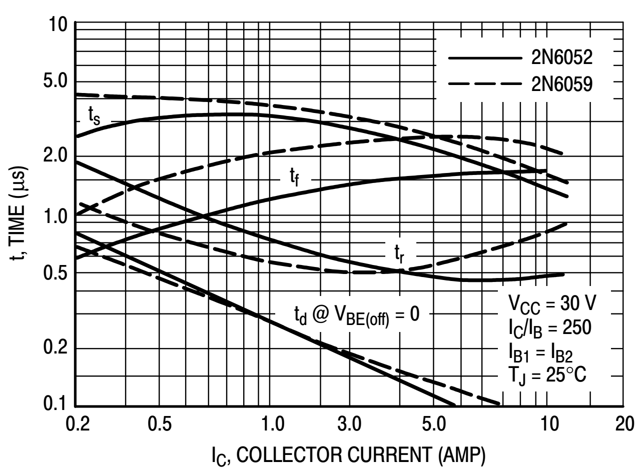


Figure 3. Switching Times

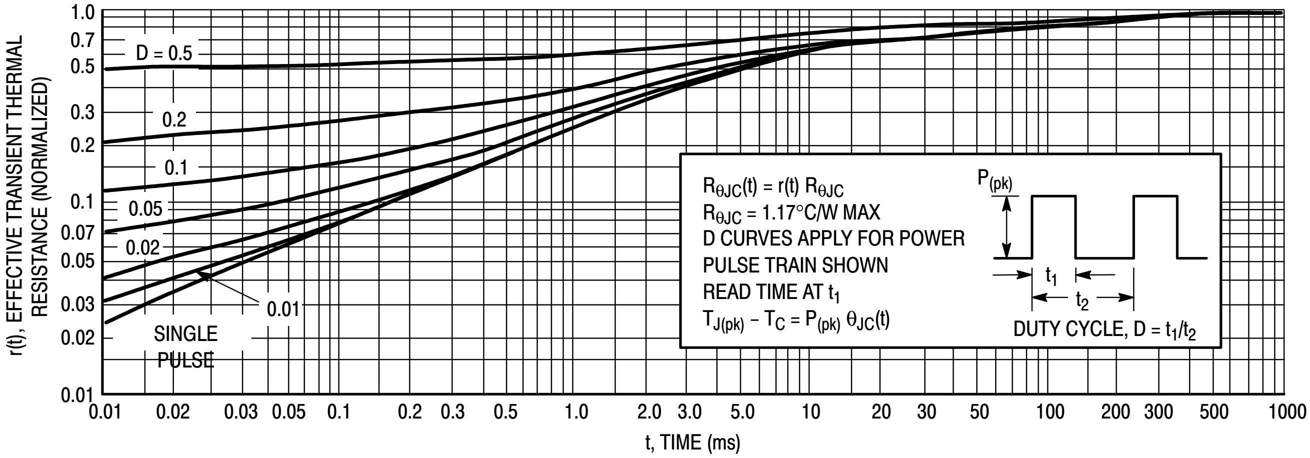


Figure 4. Thermal Response

ACTIVE–REGION SAFE OPERATING AREA

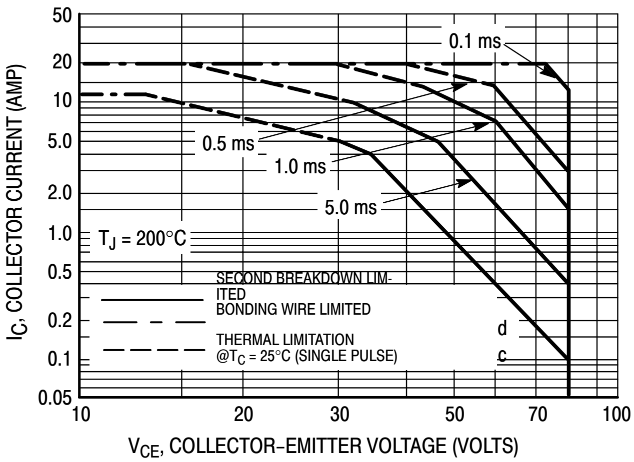


Figure 5. 2N6058

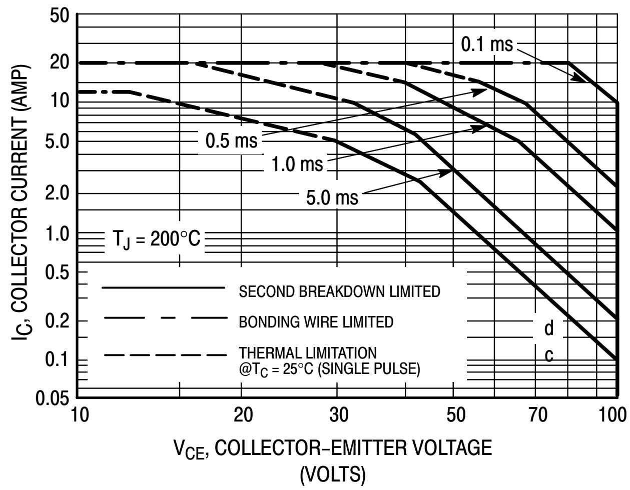


Figure 6. 2N6052, 2N6059

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C – V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5, 6, and 7 is based on $T_{J(pk)} = 200°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 200°C$; $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

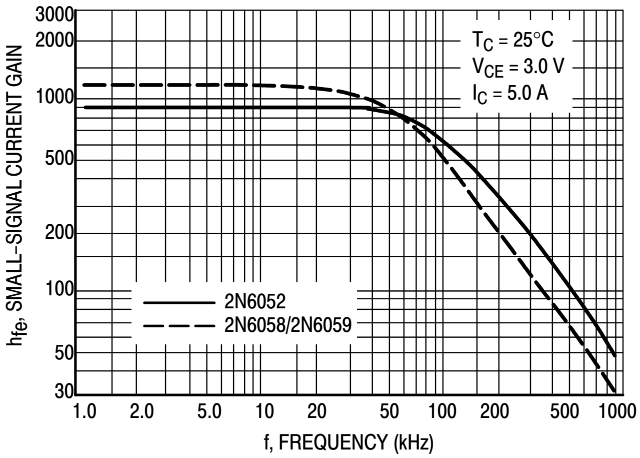


Figure 7. Small−Signal Current Gain

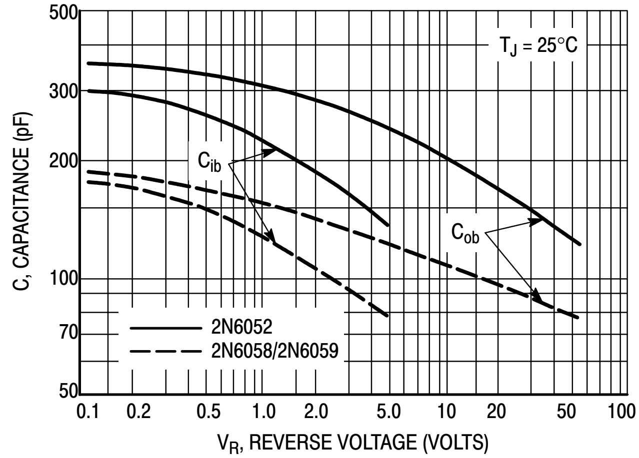


Figure 8. Capacitance

PNP
2N6052

NPN
2N6058, 2N6059

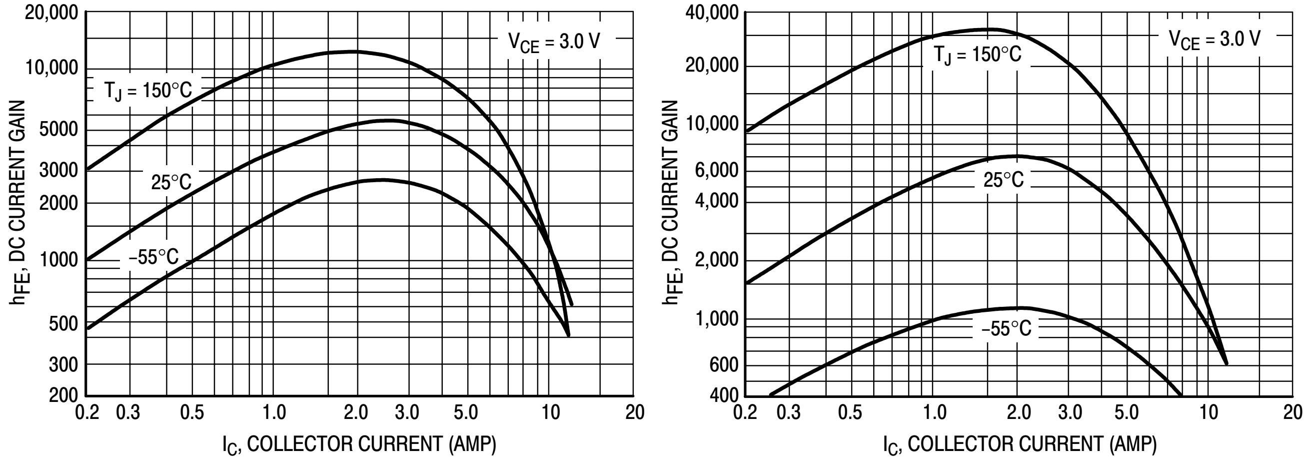


Figure 9. DC Current Gain

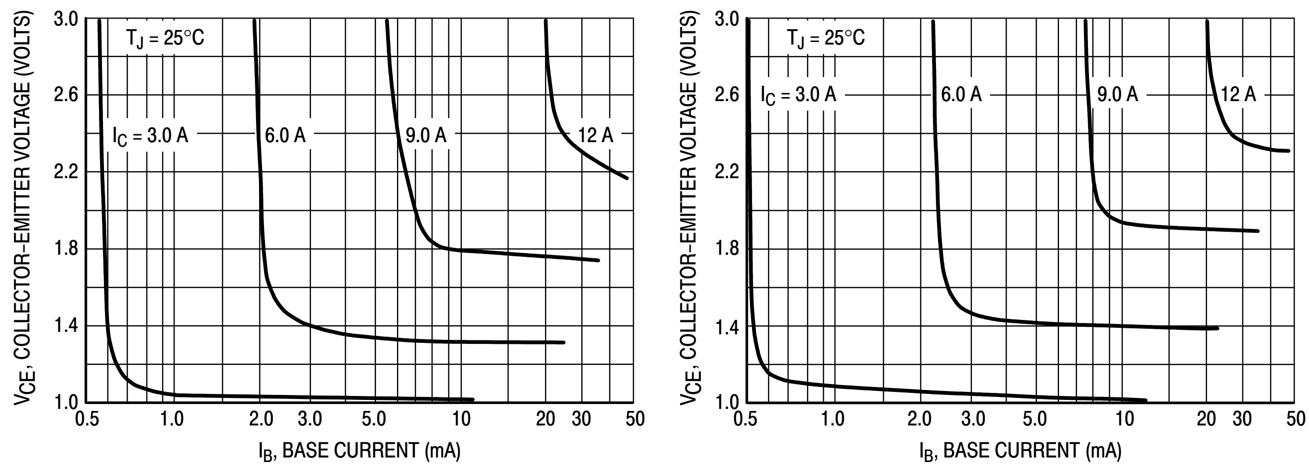


Figure 10. Collector Saturation Region

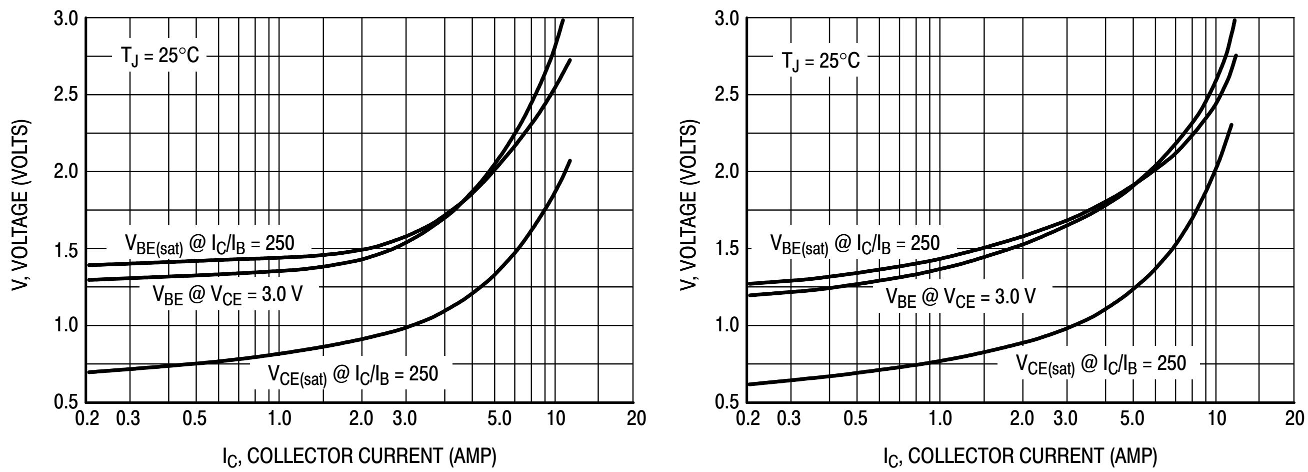
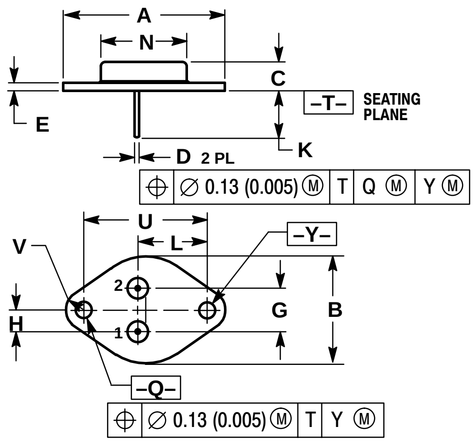


Figure 11. "On" Voltages

PACKAGE DIMENSIONS

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

Notes

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