


Automotive-grade N-channel 650 V, 70 mΩ typ., 38 A Power MOSFET MDmesh DM2 in a TO-247 package

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STW50N65DM2AG	650 V	87 mΩ	38 A

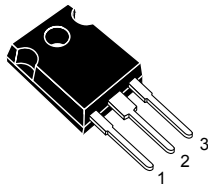
- AEC-Q101 qualified 
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

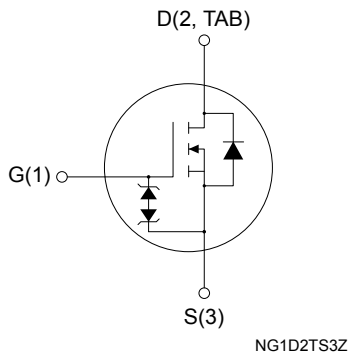
- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low R_{DS(on)}, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.



TO-247



Product status link

[STW50N65DM2AG](#)

Product summary⁽¹⁾

Order code	STW50N65DM2AG
Marking	50N65DM2
Package	TO-247
Packing	Tube

1. The HTRB test was performed at 80% V_{(BR)DSS} in compliance with AEC-Q101 rev. C. All the other tests were performed according to rev. D.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage (static)	±25	V
	Gate-source voltage (dynamic AC (f > 1 Hz))	±30	
I _D	Drain current (continuous) at T _C = 25 °C	38	A
	Drain current (continuous) at T _C = 100 °C	24	
I _{DM} ⁽¹⁾	Drain current (pulsed)	152	A
P _{TOT}	Total power dissipation at T _C = 25 °C	300	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	100	V/ns
di/dt ⁽²⁾	Peak diode recovery current slope	1000	A/μs
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	100	V/ns
T _{stg}	Storage temperature	-55 to 150	°C
T _J	Operating junction temperature		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 38 \text{ A}$, $V_{DS \text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
3. $V_{DS} \leq 520 \text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.42	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive	7.5	A
E _{AS} ⁽¹⁾	Single pulse avalanche energy	850	mJ

1. Starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			10	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 19\text{ A}$		70	87	$\text{m}\Omega$

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3200	-	pF
C_{oss}	Output capacitance		-	130	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	256	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	4	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 38\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	69	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	34	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 19\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	22.5	-	ns
t_r	Rise time		-	21	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	89	-	ns
t_f	Fall time		-	10.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 38\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	150		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	0.96		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	245		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	2.7		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	22		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

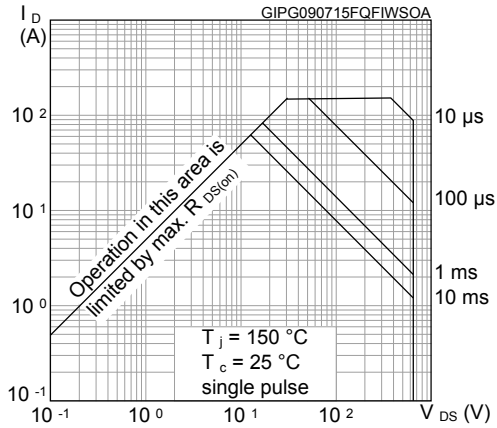


Figure 2. Thermal impedance

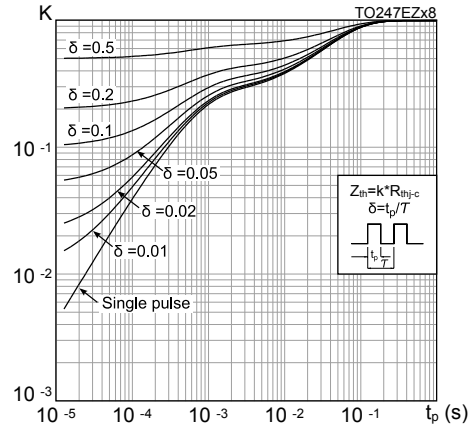


Figure 3. Output characteristics

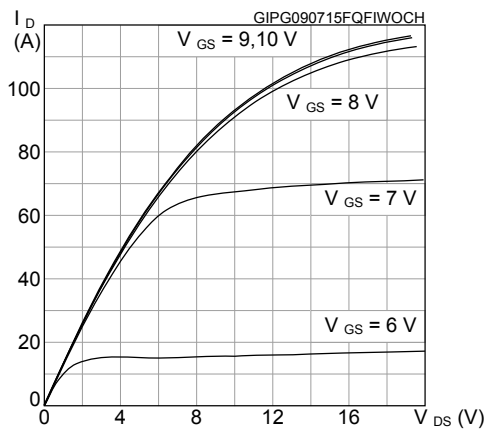


Figure 4. Transfer characteristics

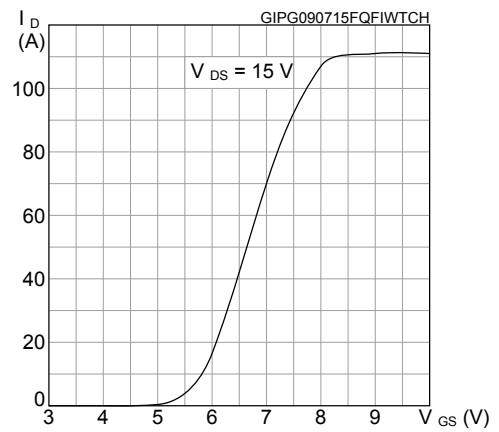


Figure 5. Gate charge vs gate-source voltage

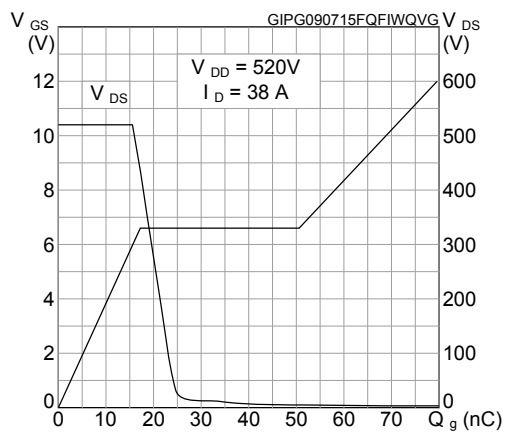


Figure 6. Static drain-source on-resistance

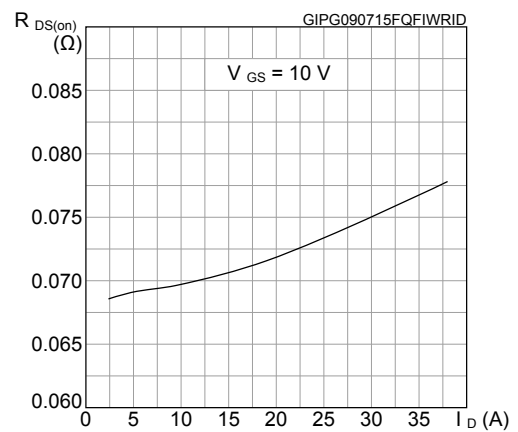


Figure 7. Capacitance variations

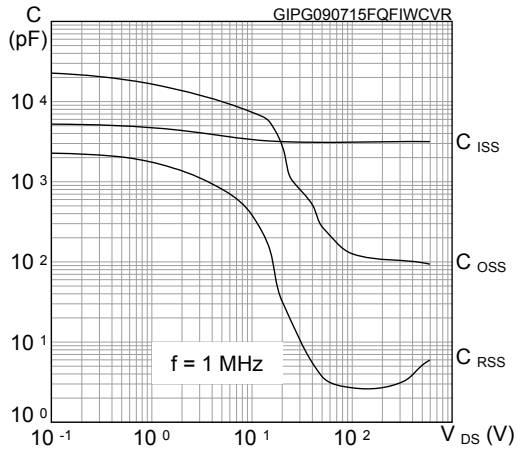


Figure 8. Normalized gate threshold voltage vs temperature

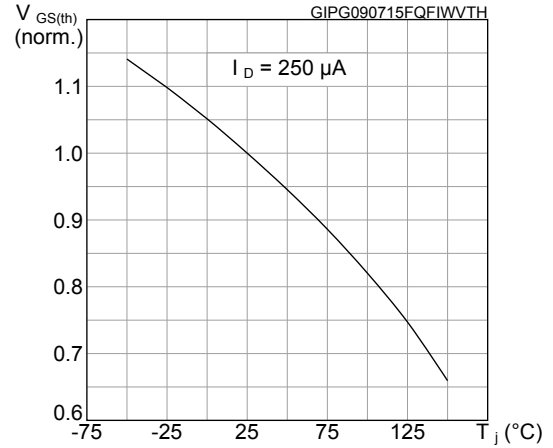


Figure 9. Normalized on-resistance vs temperature

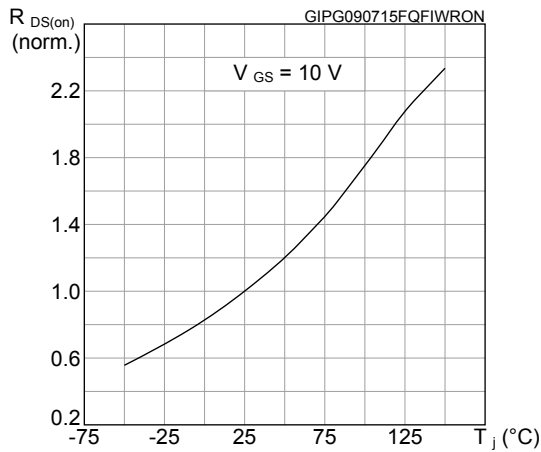


Figure 10. Normalized V_(BR)DSS vs temperature

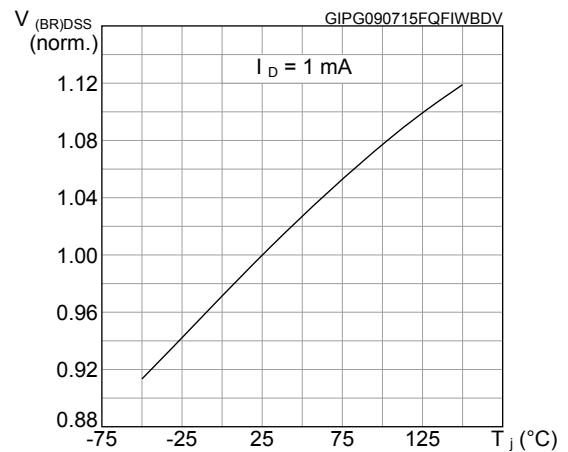


Figure 11. Output capacitance stored energy

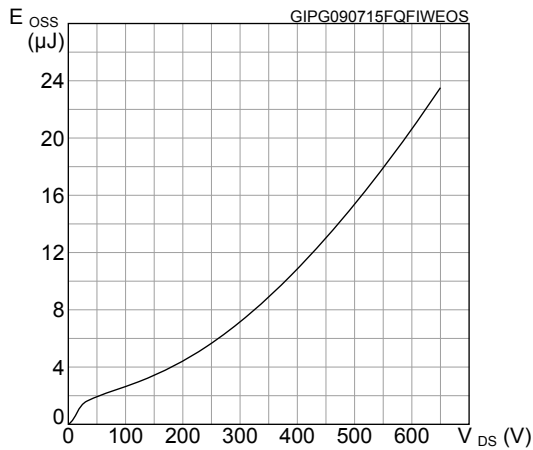
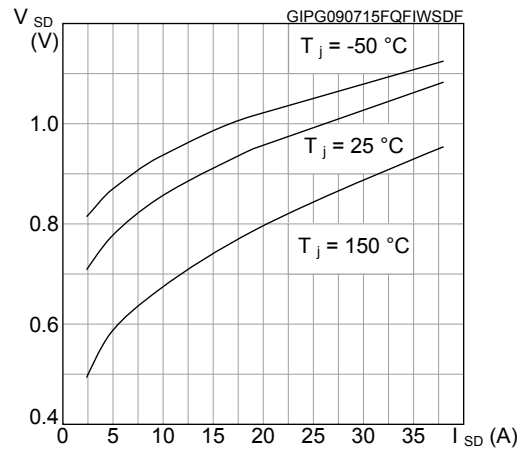
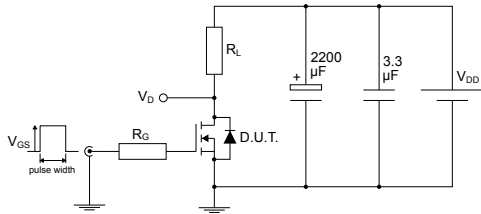


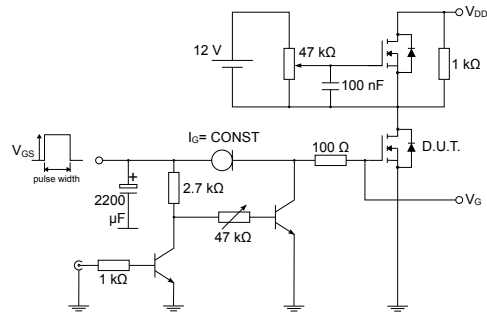
Figure 12. Source-drain diode forward characteristics



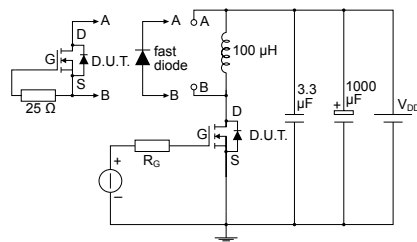
3 Test circuits

Figure 13. Test circuit for resistive load switching times


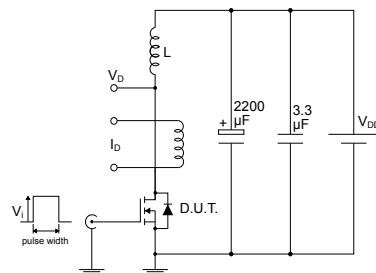
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Figure 14. Test circuit for gate charge behavior


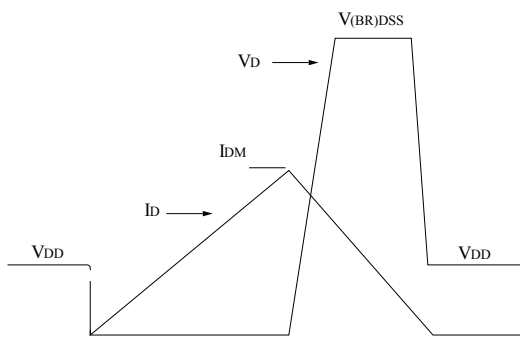
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Figure 15. Test circuit for inductive load switching and diode recovery times


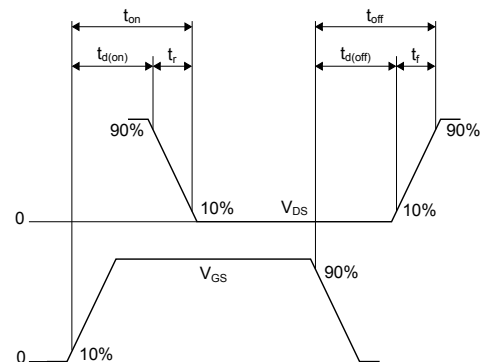
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


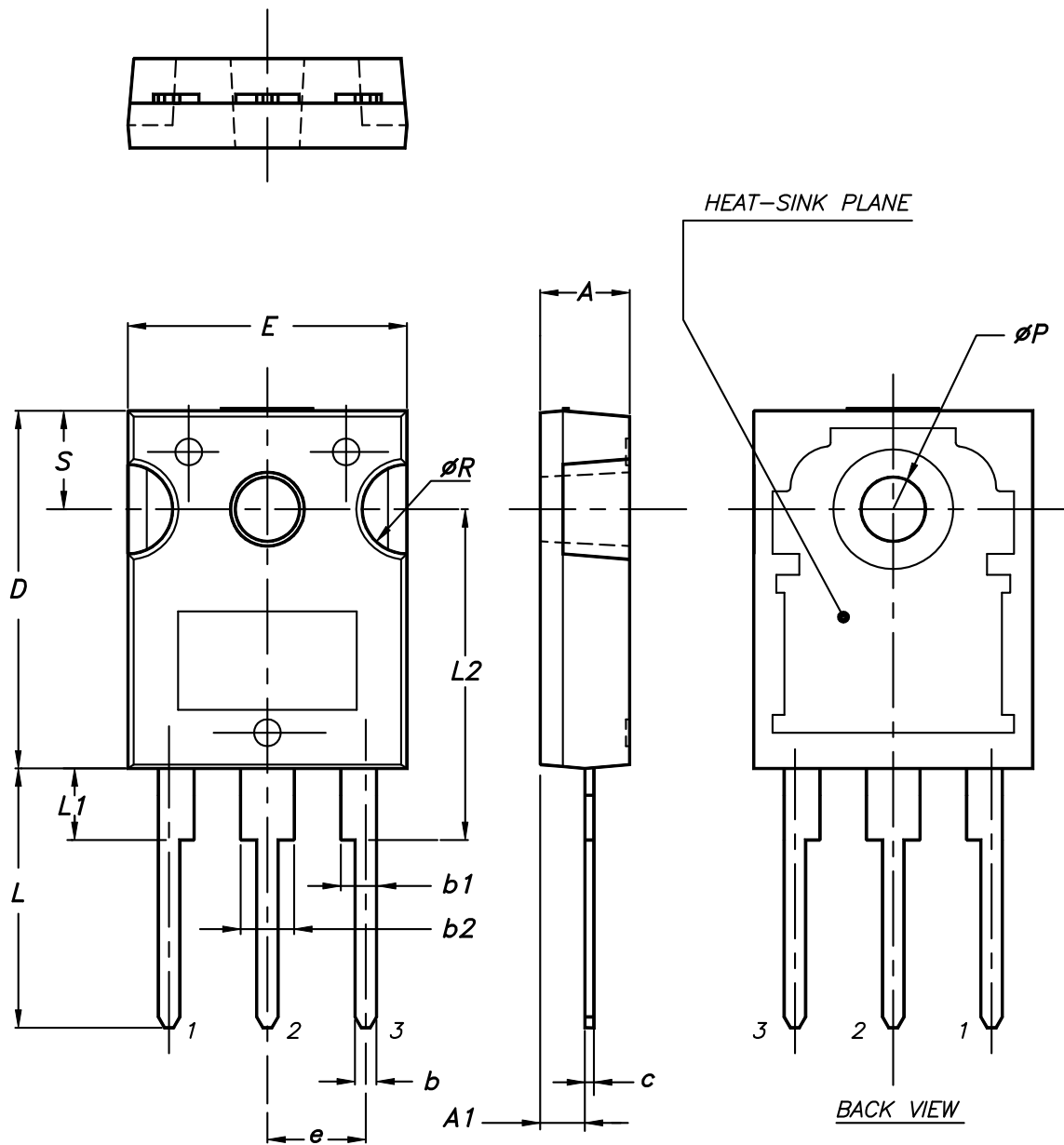
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325_9

Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Jul-2015	1	Initial release.
20-Dec-2017	2	Modified <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "Avalanche characteristics"</i> and <i>Table 8: "Source-drain diode"</i> . Modified <i>Figure 2: "Safe operating area"</i> . Minor text changes.
31-Aug-2020	3	Updated <i>Table 1. Absolute maximum ratings</i> . Minor text changes.

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