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December 2014

# FDPF041N06BL1

## N-Channel PowerTrench<sup>®</sup> MOSFET

60 V, 77 A, 4.1 mΩ

### Features

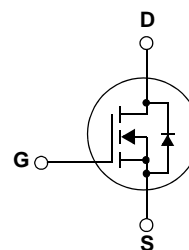
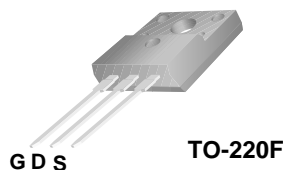
- $R_{DS(on)} = 3.5 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 77 \text{ A}$
- Low FOM  $R_{DS(on)} \cdot Q_G$
- Low Reverse Recovery Charge,  $Q_{rr}$
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted\*

Symbol	Parameter	FDPF041N06BL1	Unit
$V_{DSS}$	Drain to Source Voltage	60	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	A
		- Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	W
		- Derate above $25^\circ\text{C}$	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDPF041N06BL1	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	3.4	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	

## Package Marking and Ordering Information

Device Marking	Device	Package	Packaging Type	Quantity
FDPF041N06BL1	FDPF041N06BL1	TO-220F	Tube	50

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.03	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 48\text{V}$ , $V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 77\text{A}$	-	3.5	4.1	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{V}$ , $I_D = 77\text{A}$	-	125	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 30\text{V}$ , $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	4280	5690	pF
$C_{oss}$	Output Capacitance		-	1050	1400	pF
$C_{rss}$	Reverse Transfer Capacitance		-	23	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 30\text{V}$ , $V_{GS} = 0\text{V}$	-	1787	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 30\text{V}$ , $I_D = 100\text{A}$ $V_{GS} = 10\text{V}$	-	53	69	nC
$Q_{gs}$	Gate to Source Gate Charge		-	23	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	8	-	nC
$V_{plateau}$	Gate Plateau Voltage		-	5.7	-	V
$Q_{sync}$	Total Gate Charge Sync.	$V_{DS} = 0\text{V}$ , $I_D = 50\text{A}$ (Note 5)	-	48.6	-	nC
$Q_{oss}$	Output Charge	$V_{DS} = 30\text{V}$ , $V_{GS} = 0\text{V}$	-	63.8	-	nC

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{V}$ , $I_D = 100\text{A}$ $V_{GS} = 10\text{V}$ , $R_{GEN} = 4.7\Omega$	-	29	68	ns
$t_r$	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	38	86	ns
$t_f$	Turn-Off Fall Time		-	11	32	ns
ESR	Equivalent Series Resistance (G-S)	$f = 1\text{MHz}$	-	0.8	-	$\Omega$

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	77	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	308	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 77A	-	-	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 100A	-	65	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100A/μs	-	63	-	nC

#### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $L = 3\text{mH}$ ,  $I_{AS} = 15.6\text{A}$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 100\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics
5. See the test circuit in page 8

## Typical Performance Characteristics

Figure 1. On-Region Characteristics

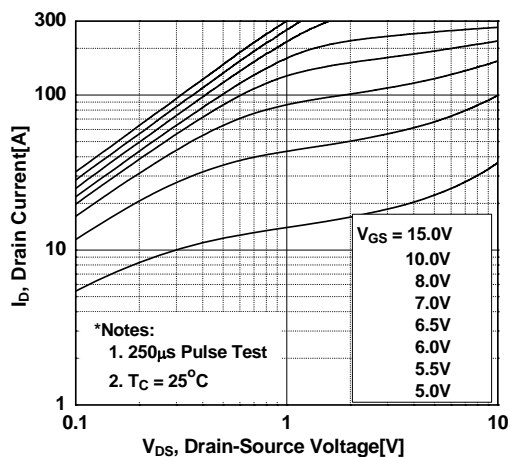


Figure 2. Transfer Characteristics

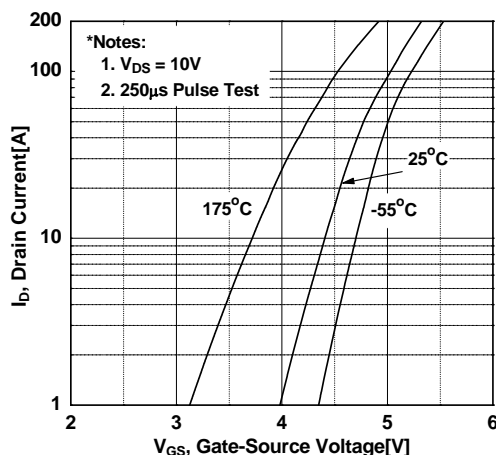


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

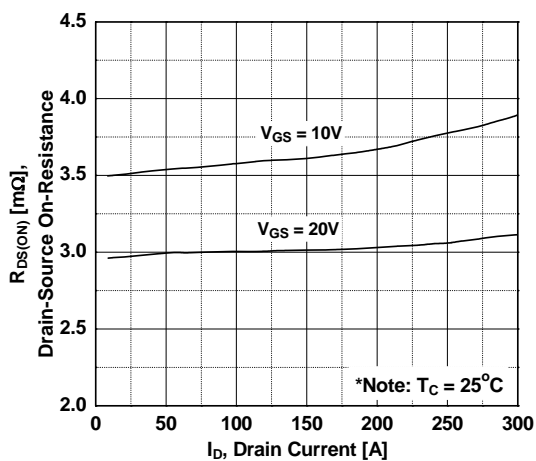


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

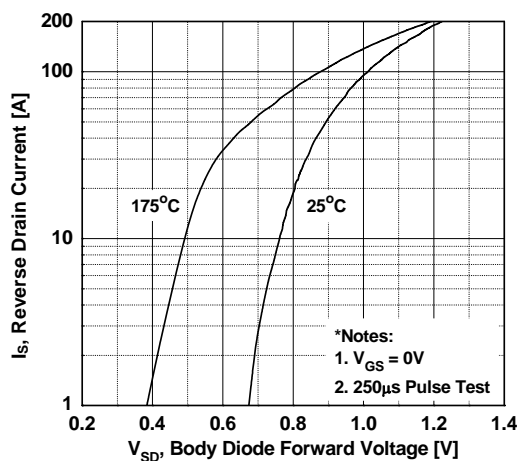


Figure 5. Capacitance Characteristics

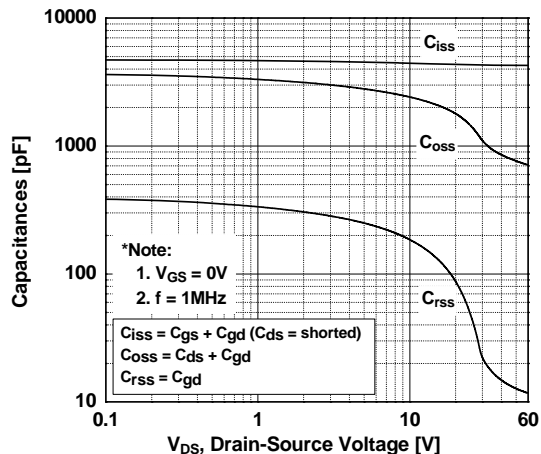
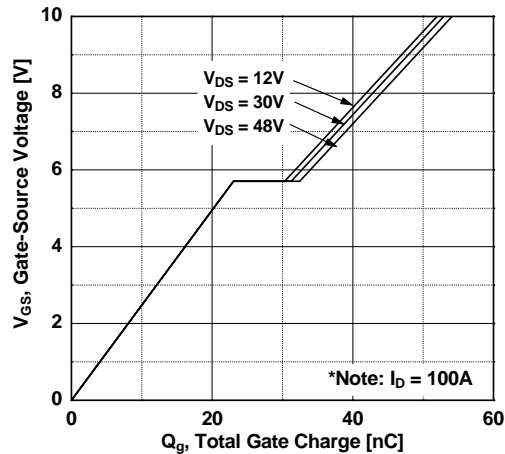


Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

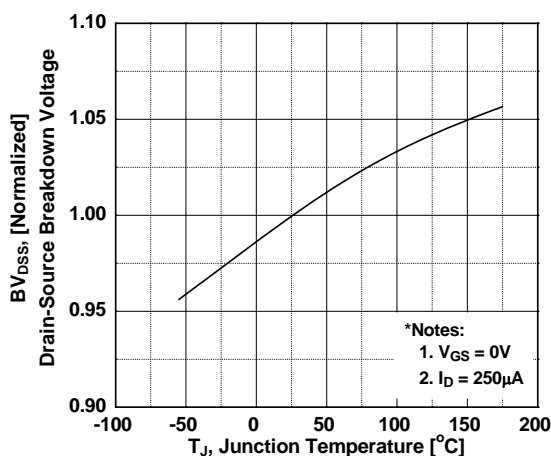


Figure 8. On-Resistance Variation vs. Temperature

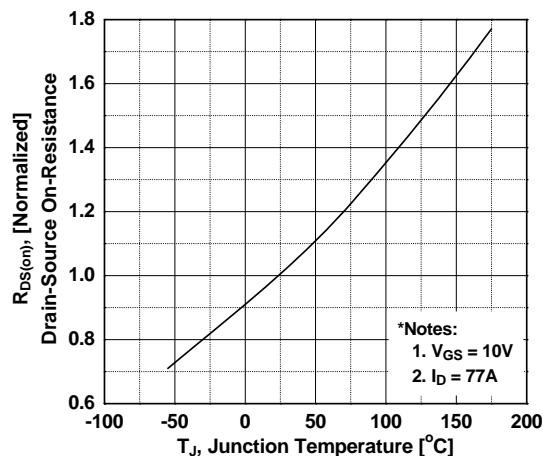


Figure 9. Maximum Safe Operating Area vs. Case Temperature

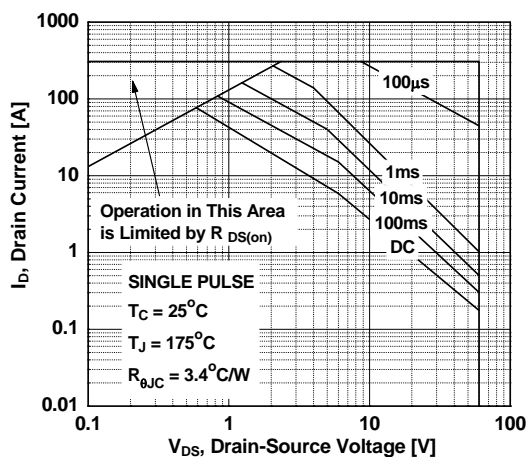


Figure 10. Maximum Drain Current

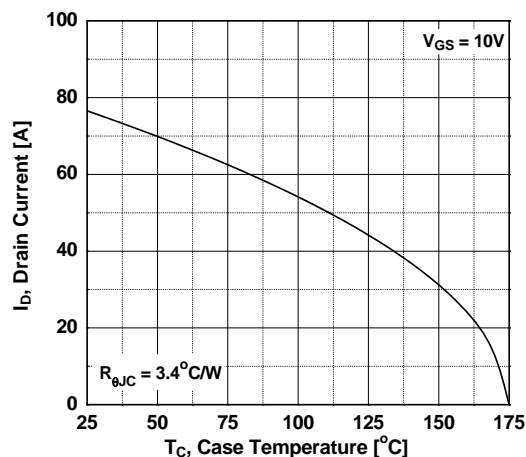


Figure 11. E\_oss vs. Drain to Source Voltage

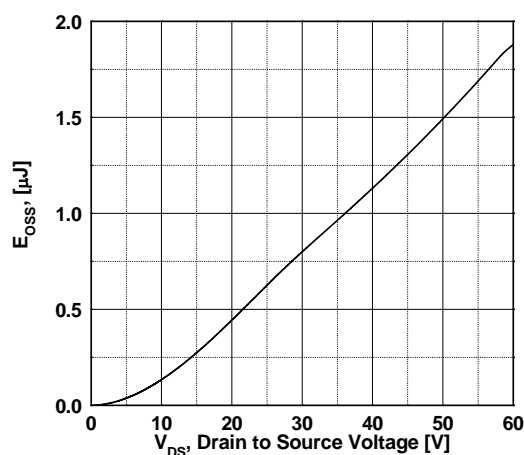
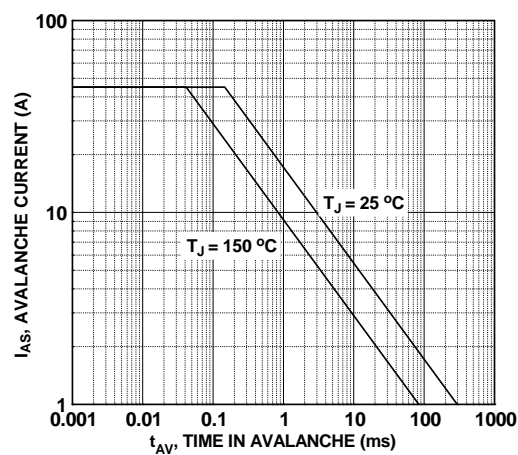
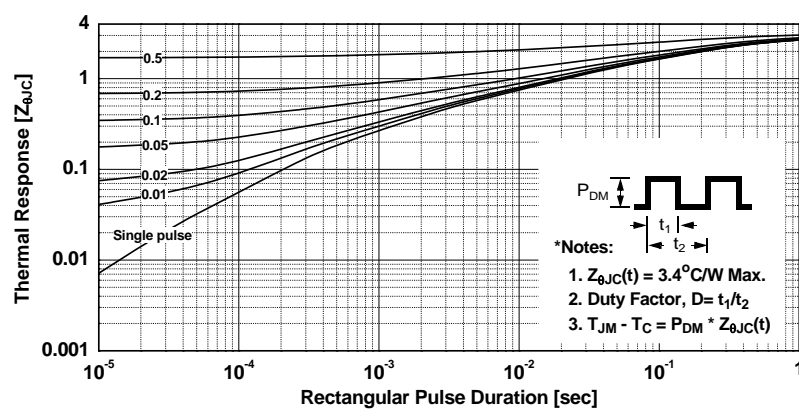


Figure 12. Unclamped Inductive Switching Capability

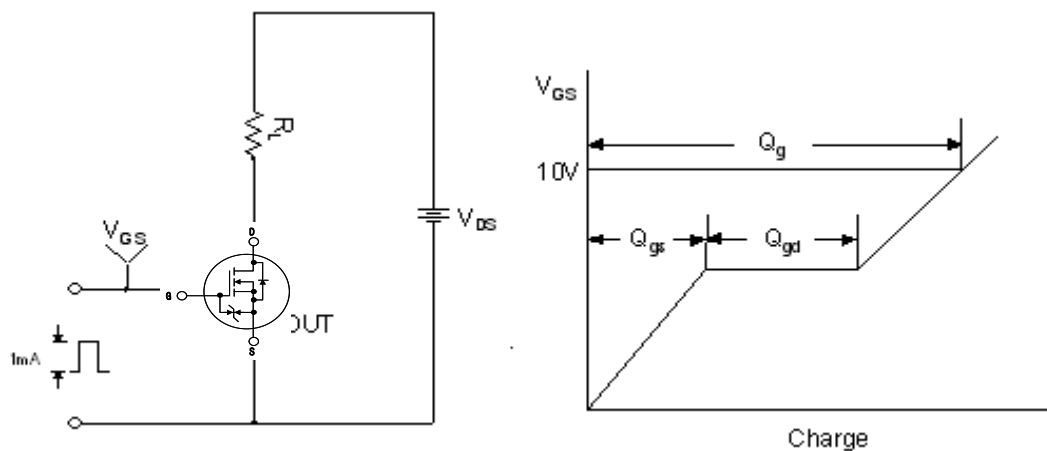


## Typical Performance Characteristics (Continued)

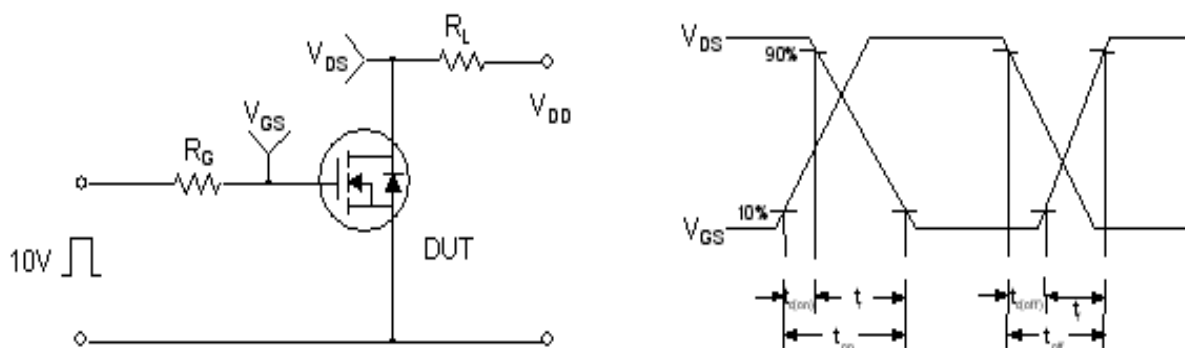
Figure 13. Transient Thermal Response Curve



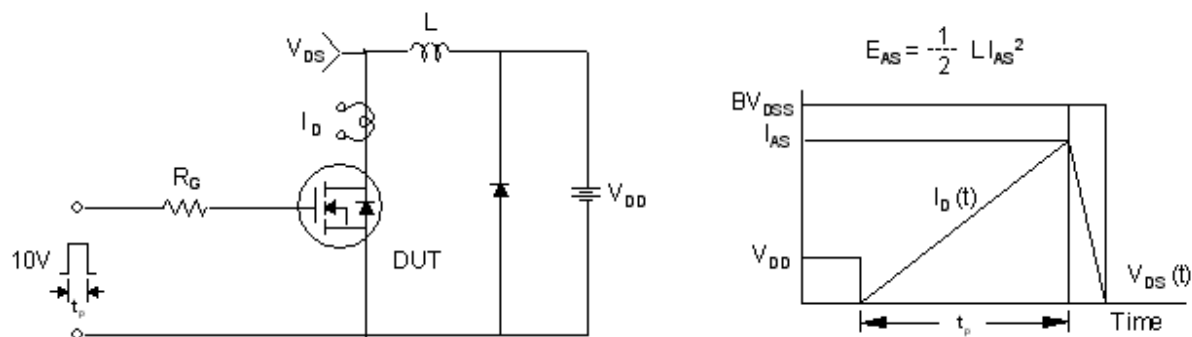
Gate Charge Test Circuit & Waveform



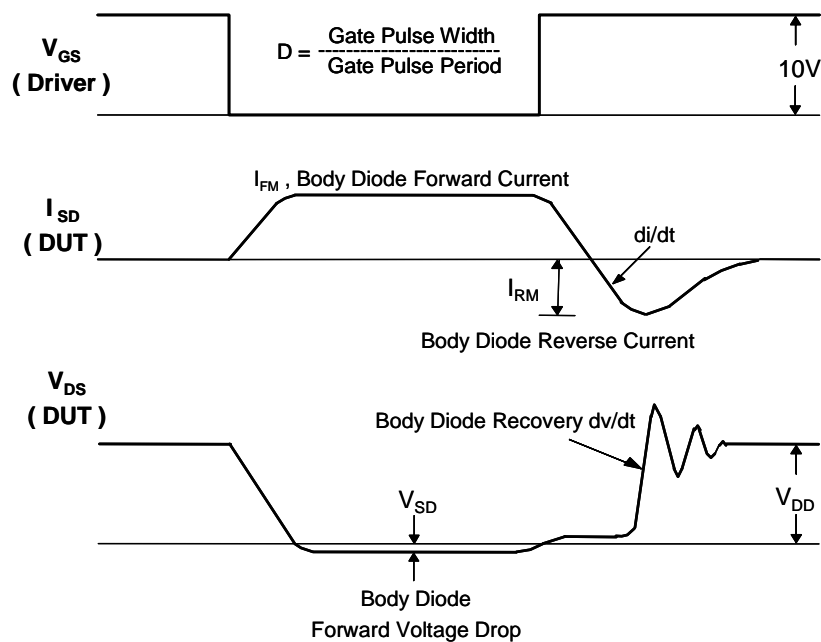
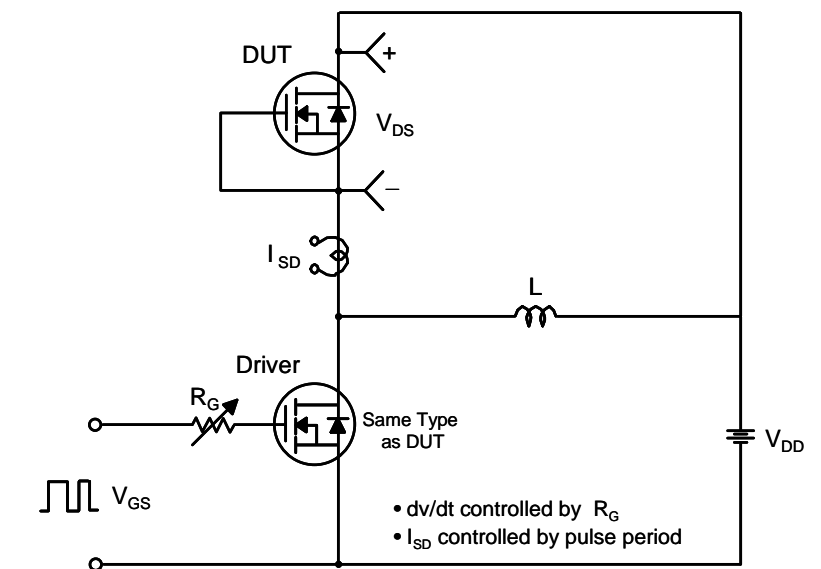
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

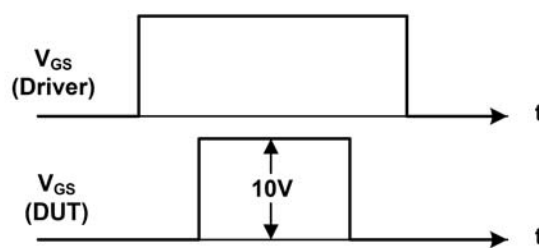
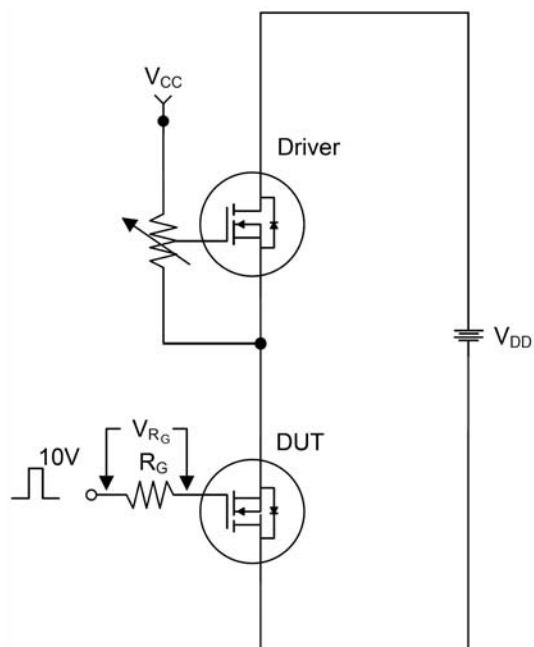


# Peak Diode Recovery dv/dt Test Circuit & Waveforms





# Total Gate Charge $Q_{sync}$ . Test Circuit & Waveforms



$$Q_{sync} = \frac{1}{R_G} \cdot \int V_{RG}(t) dt$$



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