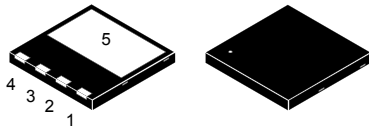
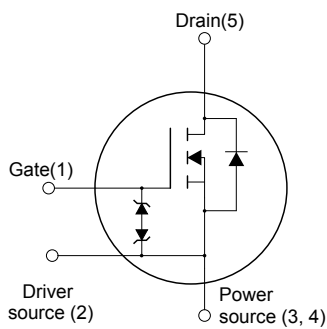


N-channel 650 V, 0.182 Ω typ., 20 A, MDmesh™ DM2 Power MOSFET in a PowerFLAT™ 8x8 HV package



PowerFLAT™ 8x8 HV



NG1DS2PS34D5Z

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL26N65DM2	650 V	0.206 Ω	20 A	140 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STL26N65DM2](#)

Product summary

Order code	STL26N65DM2
Marking	26N65DM2
Package	PowerFLAT™ 8x8 HV
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ °C}$	20	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	12.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	53	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ °C}$	140	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 20\text{ A}$, $di/dt=900\text{ A}/\mu\text{s}$, $V_{DD} = 400\text{ V}$, $V_{DS(peak)} < V_{(BR)DSS}$
3. $V_{DS} \leq 520\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.89	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	

1. When mounted on an 1-inch² FR-4, 2oz Cu board

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	3	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	530	mJ

1. Pulse width limited by T_{jmax}
2. Starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 650\text{ V}$, $T_{\text{case}} = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 10\text{ A}$		0.182	0.206	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iSS}	Input capacitance		-	1480	-	pF
C_{OSS}	Output capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	62	-	
C_{rSS}	Reverse transfer capacitance		-	2	-	
$C_{\text{OSS eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }520\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	140	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	4.6	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 520\text{ V}$, $I_{\text{D}} = 20\text{ A}$, $V_{\text{GS}} = 0\text{ to }10\text{ V}$ (see Figure 14. Gate charge test circuit)	-	35.5	-	nC
Q_{gs}	Gate-source charge		-	8.2	-	
Q_{gd}	Gate-drain charge		-	17.6	-	

1. $C_{\text{OSS eq.}}$ is defined as the constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 325\text{ V}$, $I_{\text{D}} = 10\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$	-	17	-	ns
t_{r}	Rise time		-	7	-	
$t_{\text{d(off)}}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	51	-	
t_{f}	Fall time		-	10	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		53	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 20\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	100		ns
Q_{rr}	Reverse recovery charge		-	0.365		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	7.3		A
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	200		ns
Q_{rr}	Reverse recovery charge		-	1.39		μC
I_{RRM}	Reverse recovery current		(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	13.9	

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

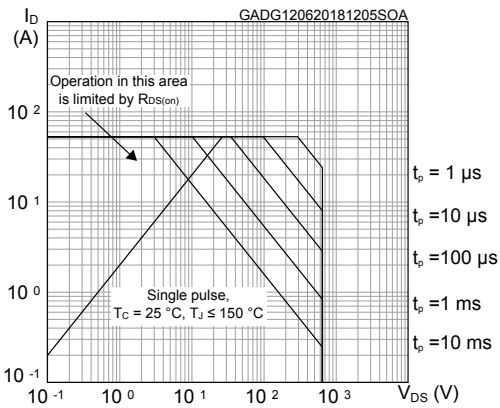


Figure 2. Thermal impedance

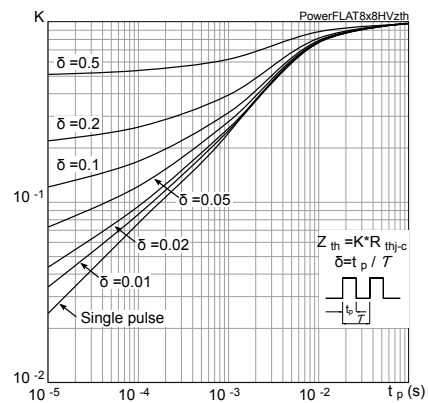


Figure 3. Output characteristics

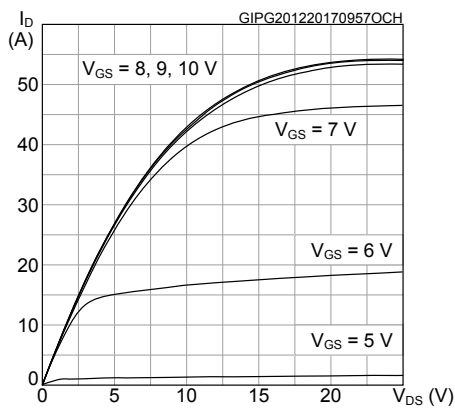


Figure 4. Transfer characteristics

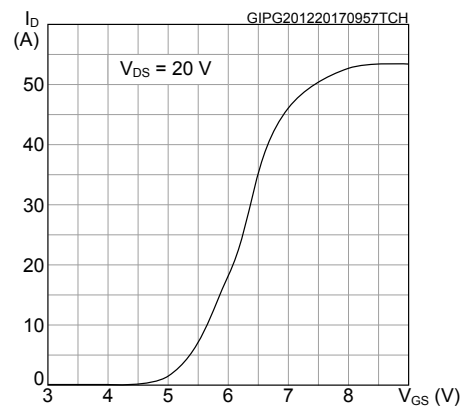


Figure 5. Gate charge vs gate-source voltage

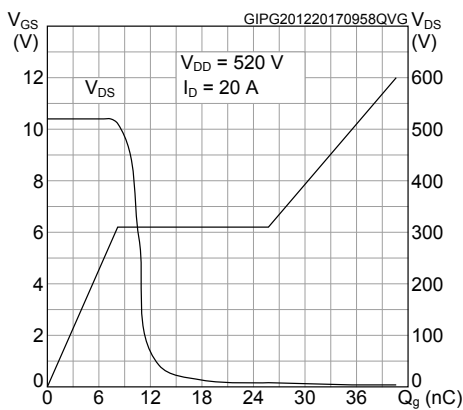


Figure 6. Static drain-source on-resistance

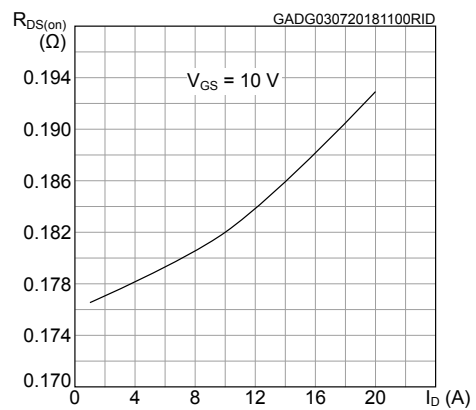


Figure 7. Capacitance variations

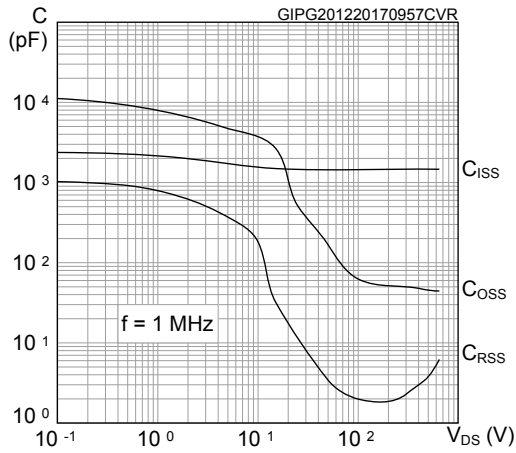


Figure 8. Normalized gate threshold voltage vs temperature

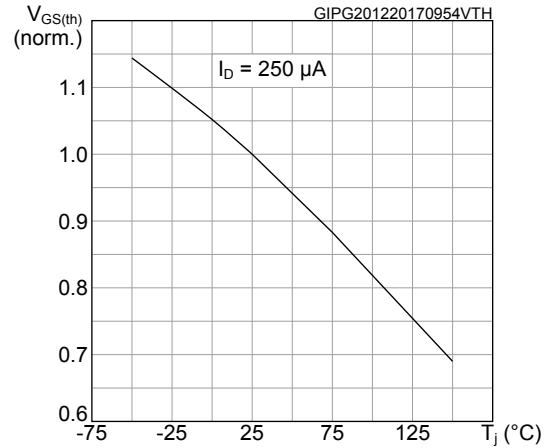


Figure 9. Normalized on-resistance vs temperature

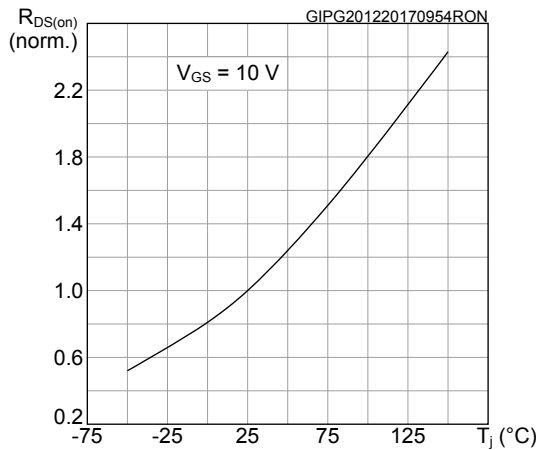


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

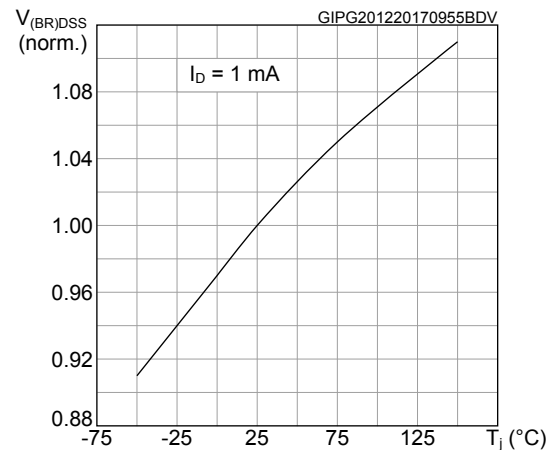


Figure 11. Output capacitance stored energy

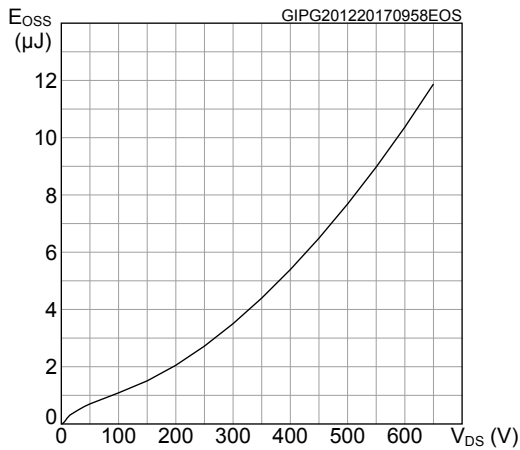
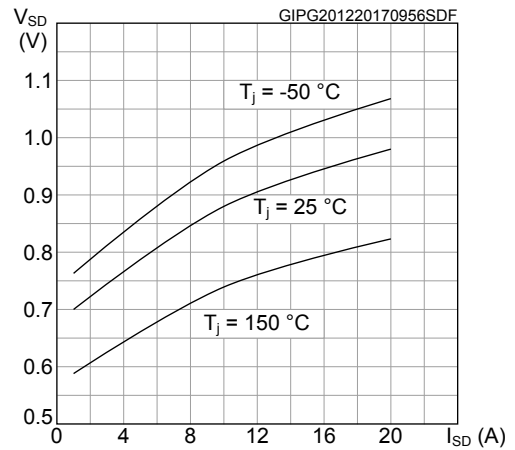
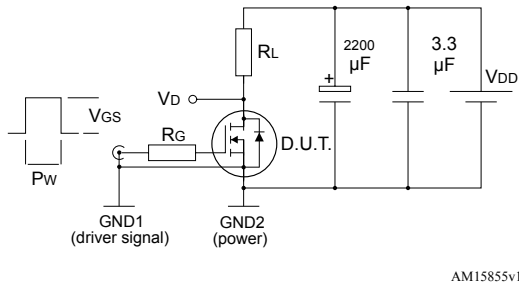
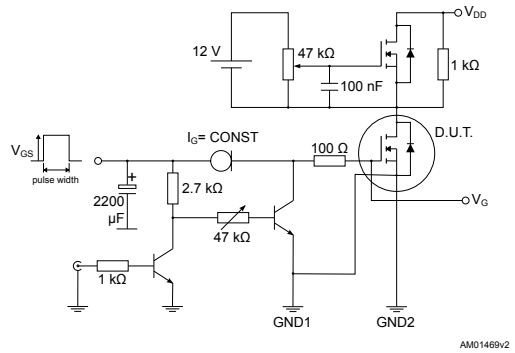
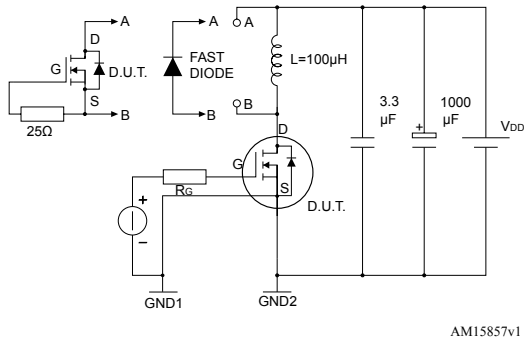
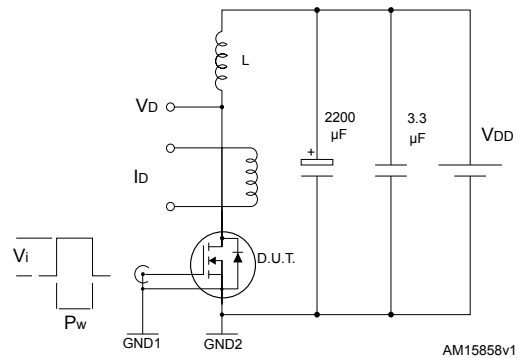
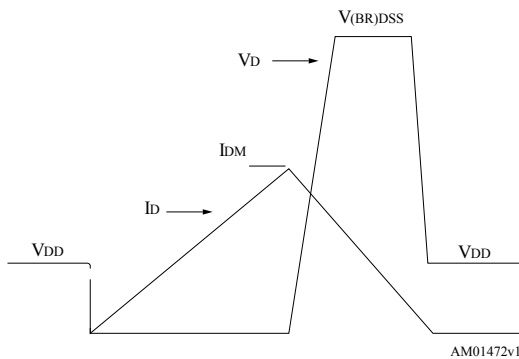
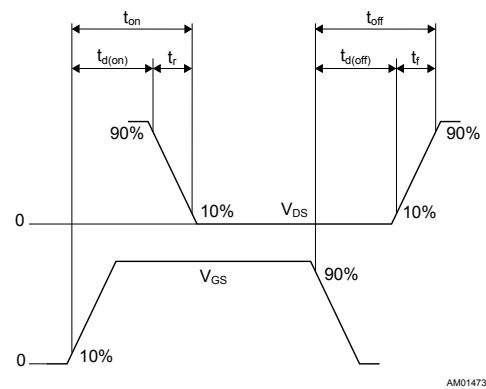


Figure 12. Source-drain diode forward characteristics



3 Test circuits

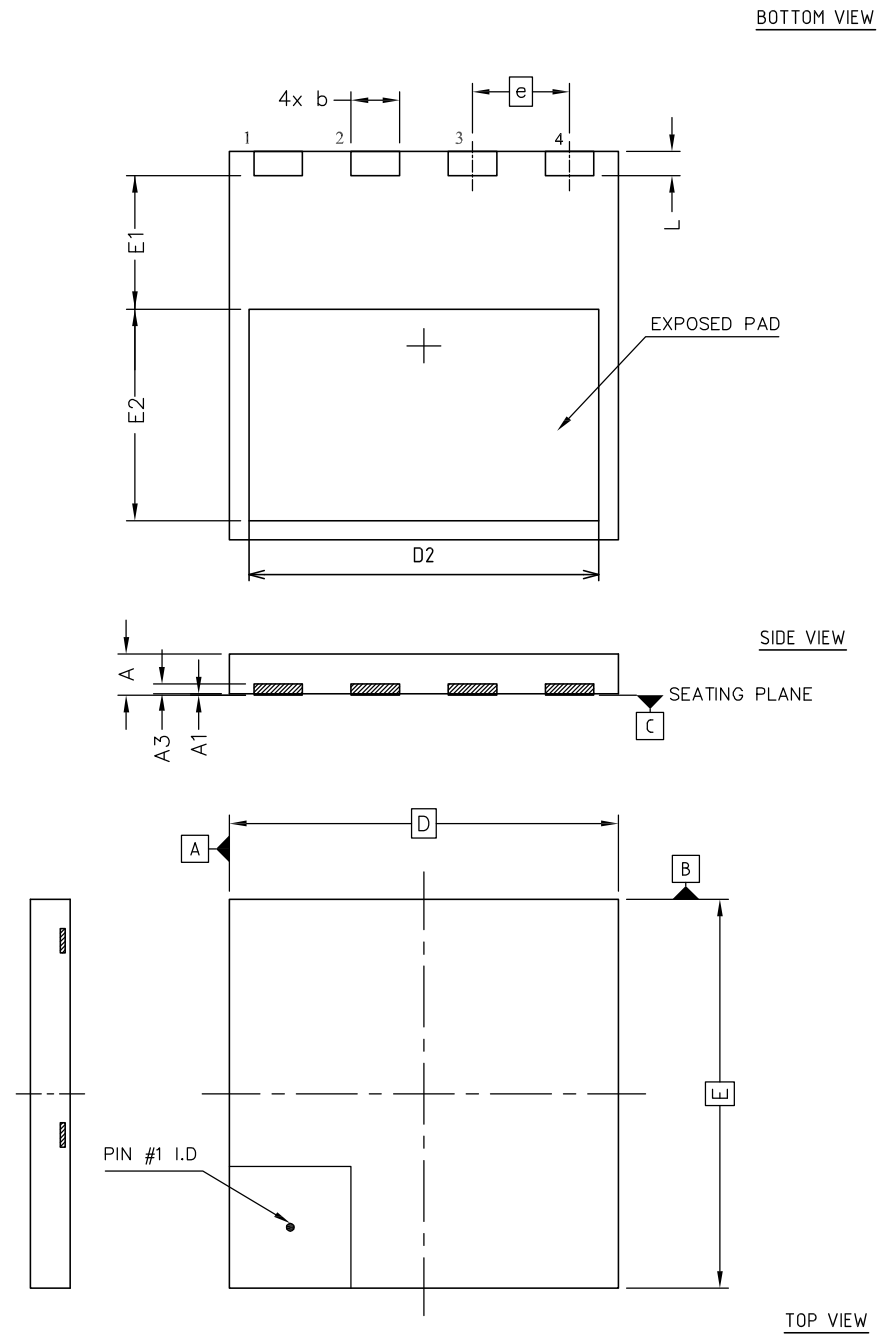
Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 8x8 HV package information

Figure 19. PowerFLAT™ 8x8 HV package outline

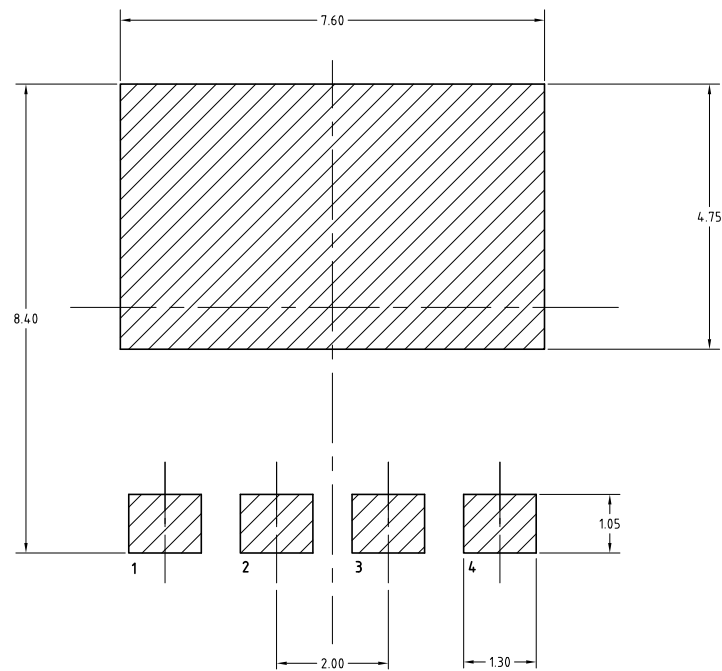


8222871_Rev_4

Table 9. PowerFLAT™ 8x8 HV mechanical data

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

Figure 20. PowerFLAT™ 8x8 HV footprint

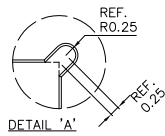
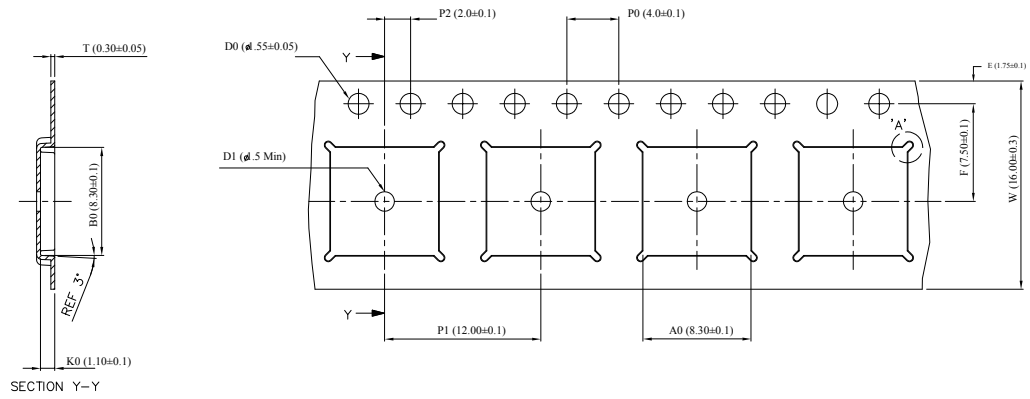


8222871_REV_4_footprint

Note: All dimensions are in millimeters.

4.2 PowerFLAT™ 8x8 HV packing information

Figure 21. PowerFLAT™ 8x8 HV tape



Note: Base and Bulk quantity 3000 pcs

8229819_Tape_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape

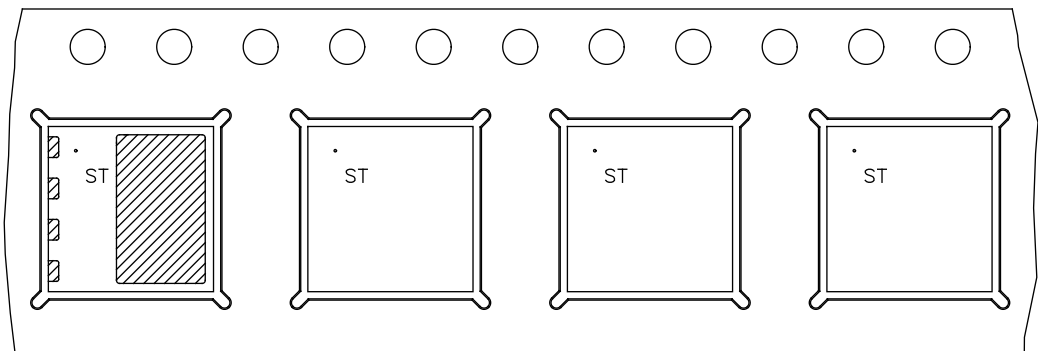
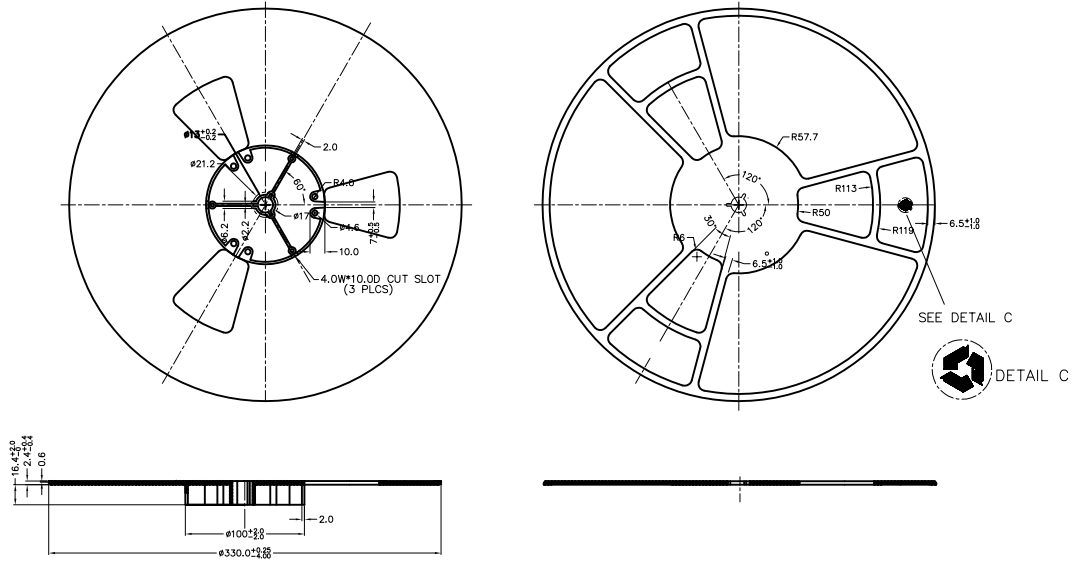


Figure 23. PowerFLAT™ 8x8 HV reel



8229819_Reel_revA

Note: All dimensions are in millimeters.

Revision history

Table 10. Document revision history

Date	Version	Changes
03-Jul-2018	1	Initial release.

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2	Electrical characteristics	3
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