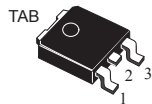
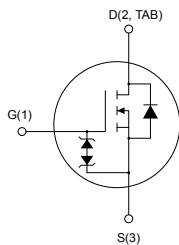


## N-channel 600 V 670 mΩ typ., 6 A MDmesh M6 Power MOSFET in a DPAK package


**DPAK**


AM01476v1\_tab

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD9N60M6	600 V	750 mΩ	6 A

- Reduced switching losses
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters, resonant converters
- Boost PFC converters

### Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



#### Product status link

[STD9N60M6](#)

#### Product summary

<b>Order code</b>	STD9N60M6
<b>Marking</b>	9N60M6
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	6	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	13.4	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	76	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	100	V/ns
$T_j$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		

1. Pulse width limited by package.
2.  $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 400\text{ V}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ .
3.  $V_{DS} \leq 480\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.65	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	°C/W

1. When mounted on an 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{jmax}$ )	1.1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	95	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$		670	750	m $\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	273	-	pF
$C_{oss}$	Output capacitance		-	24	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.65	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	49	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	10.0	-	nC
$Q_{gs}$	Gate-source charge		-	1.9	-	nC
$Q_{gd}$	Gate-drain charge		-	5.4	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	7	-	ns
$t_r$	Rise time		-	4.1	-	ns
$t_{d(off)}$	Turn-off delay time		-	16.5	-	ns
$t_f$	Fall time		-	8.8	-	ns

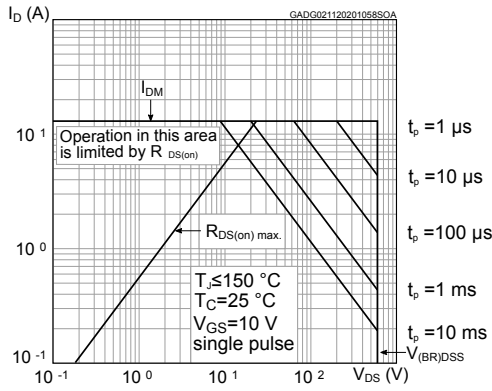
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		13.4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	153		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	0.813		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	10.3		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	248		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	1.33		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	10.7		A

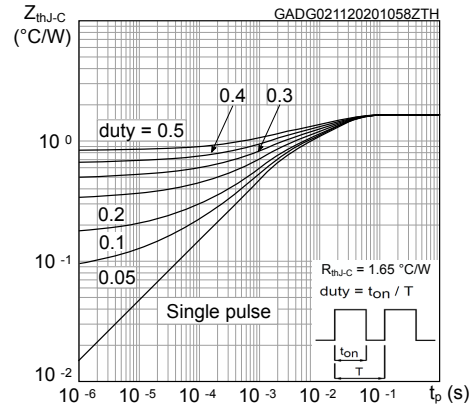
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

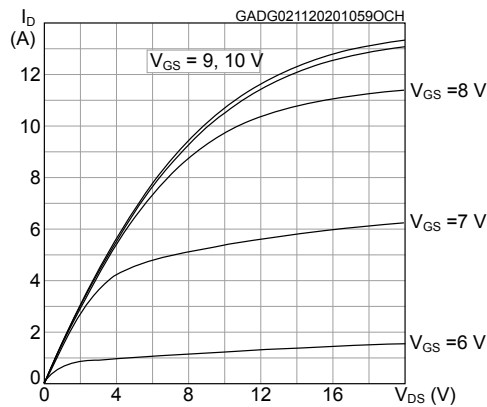
**Figure 1. Safe operating area**



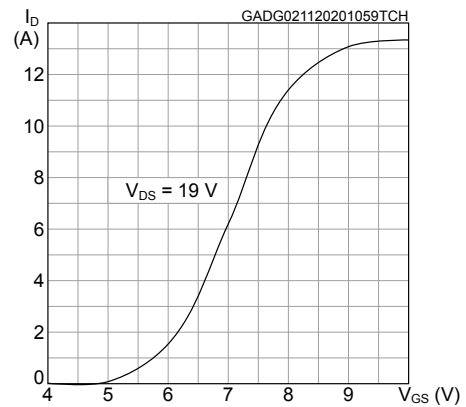
**Figure 2. Maximum transient thermal impedance**



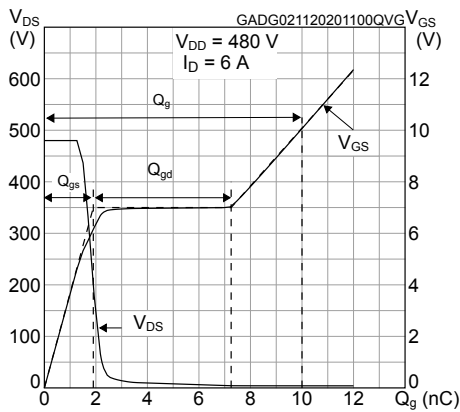
**Figure 3. Typical output characteristics**



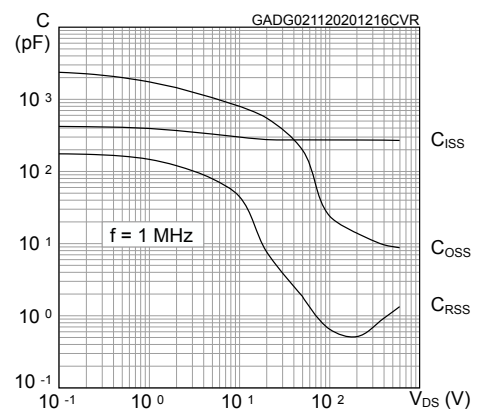
**Figure 4. Typical transfer characteristics**



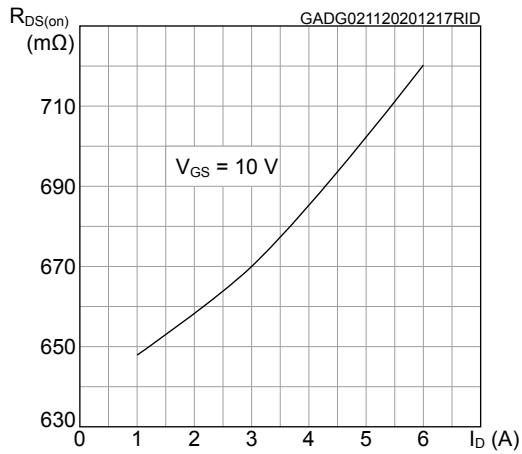
**Figure 5. Typical gate charge characteristics**



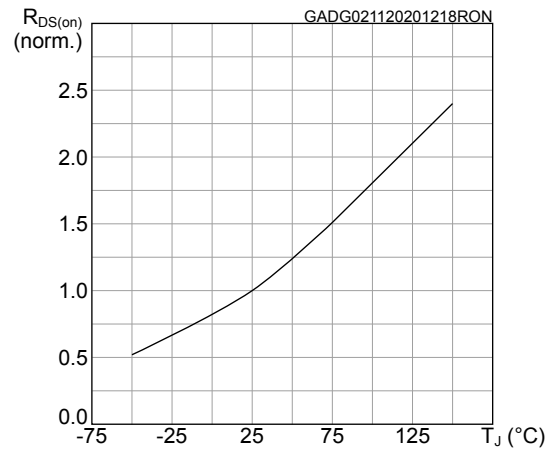
**Figure 6. Typical capacitance characteristics**



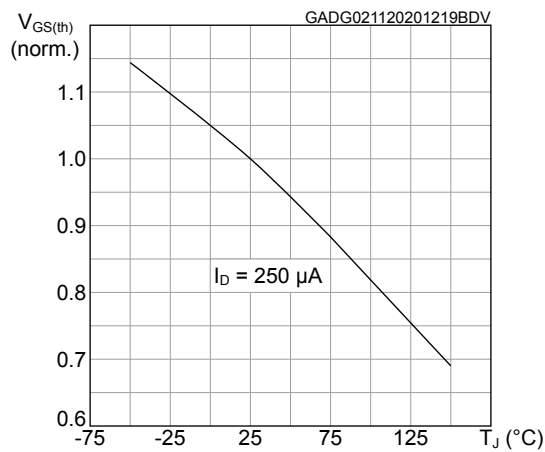
**Figure 7. Typical drain-source on-resistance**



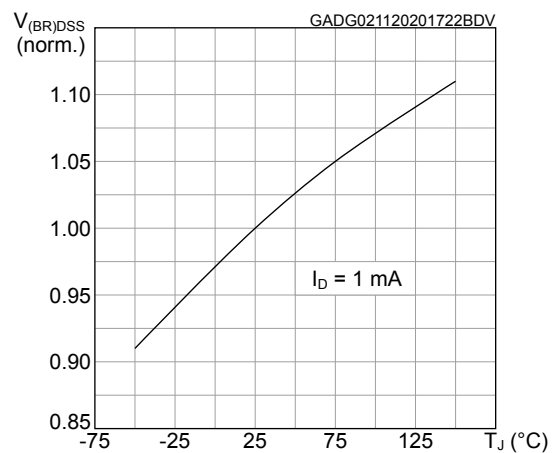
**Figure 8. Normalized on-resistance vs temperature**



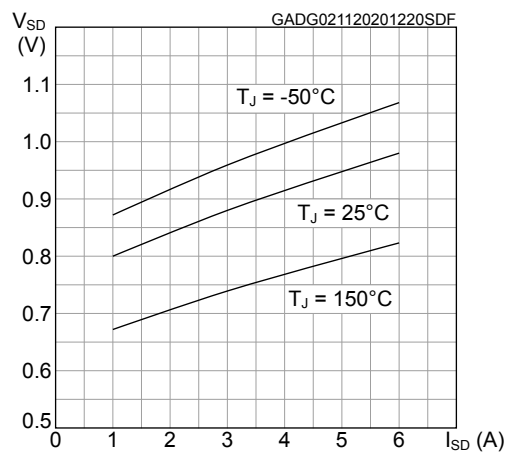
**Figure 9. Normalized gate threshold vs temperature**



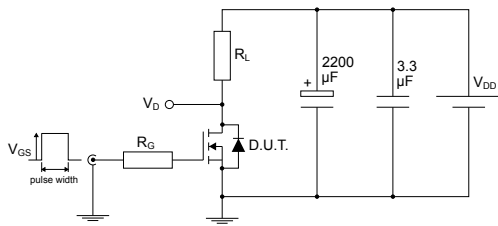
**Figure 10. Normalized breakdown voltage vs temperature**



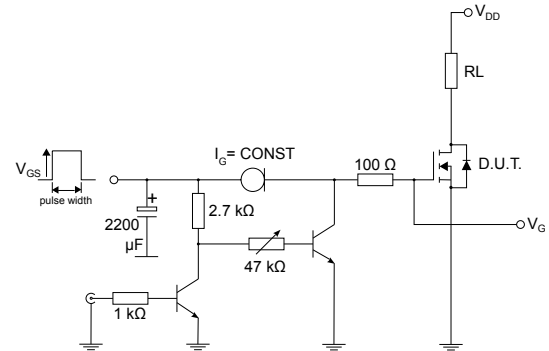
**Figure 11. Typical reverse diode forward characteristics**



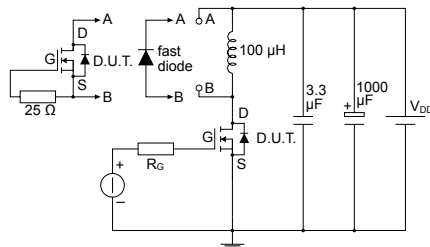
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


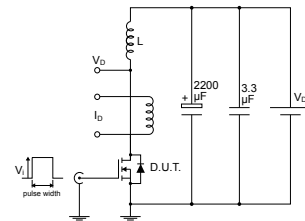
AM01468v1

**Figure 13. Test circuit for gate charge behavior**


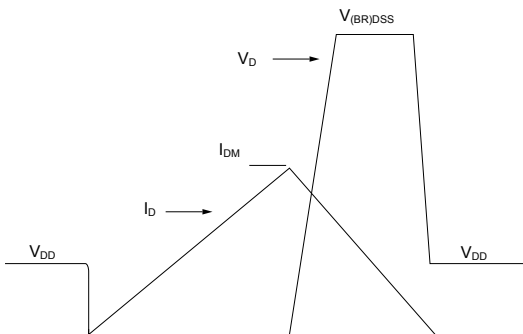
AM01469v10

**Figure 14. Test circuit for inductive load switching and diode recovery times**


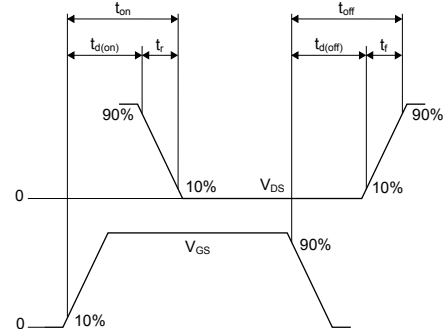
AM01470v1

**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


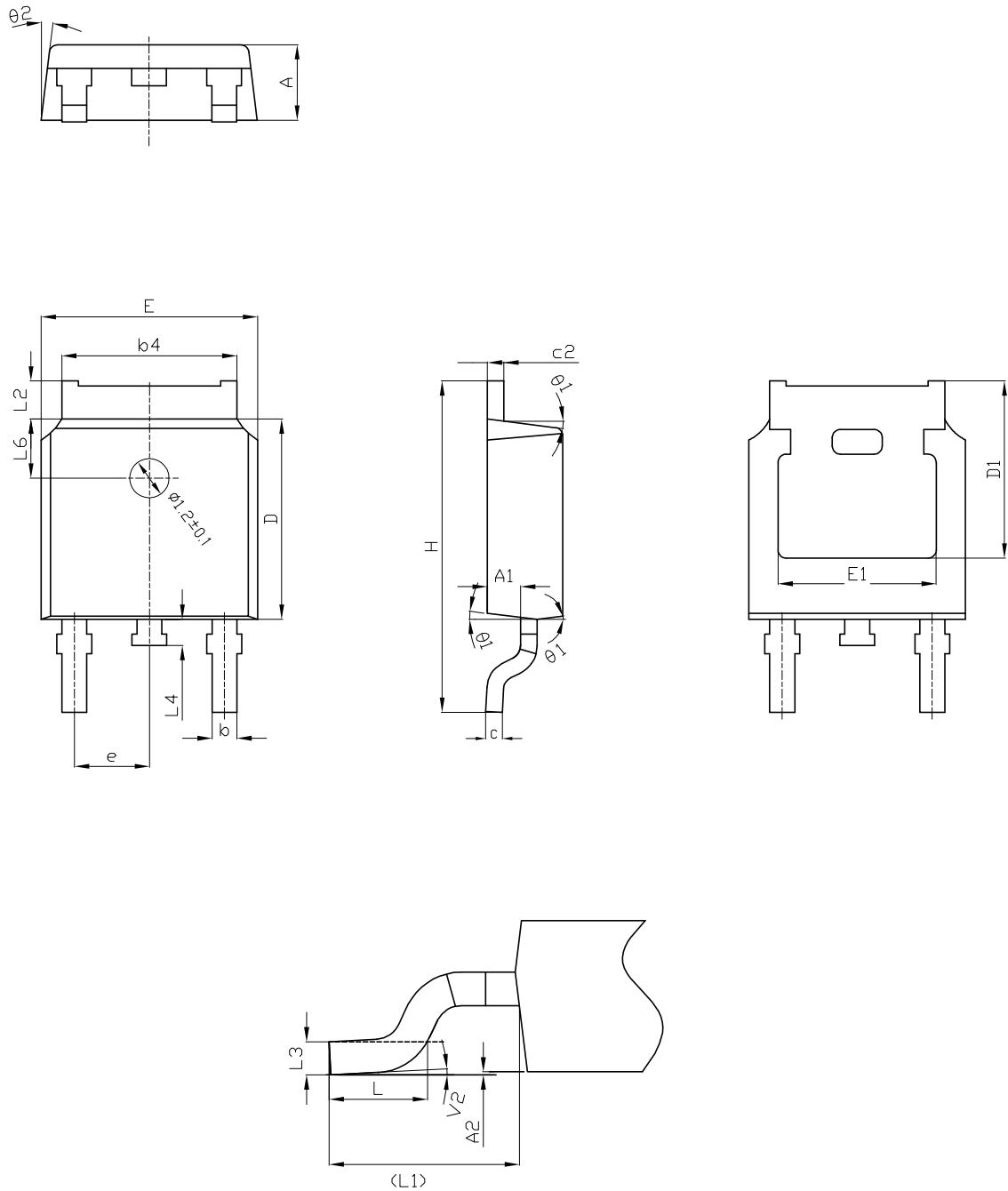
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type C package information

Figure 18. DPAK (TO-252) type C package outline



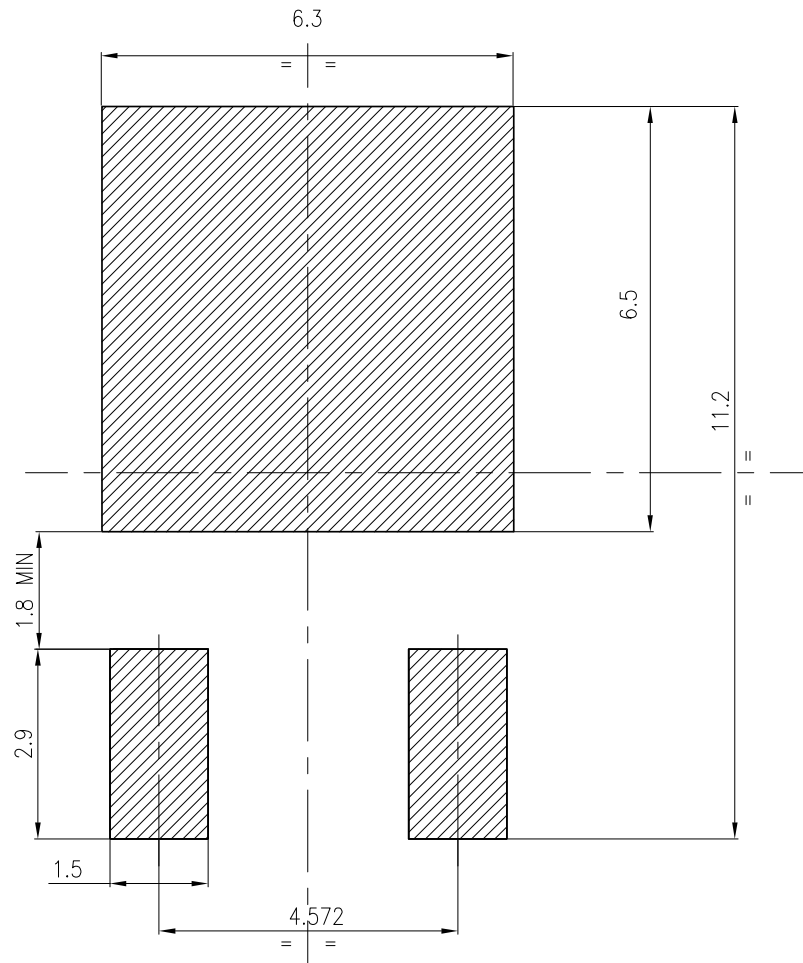
0068772\_C\_29



**Table 8. DPAK (TO-252) type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

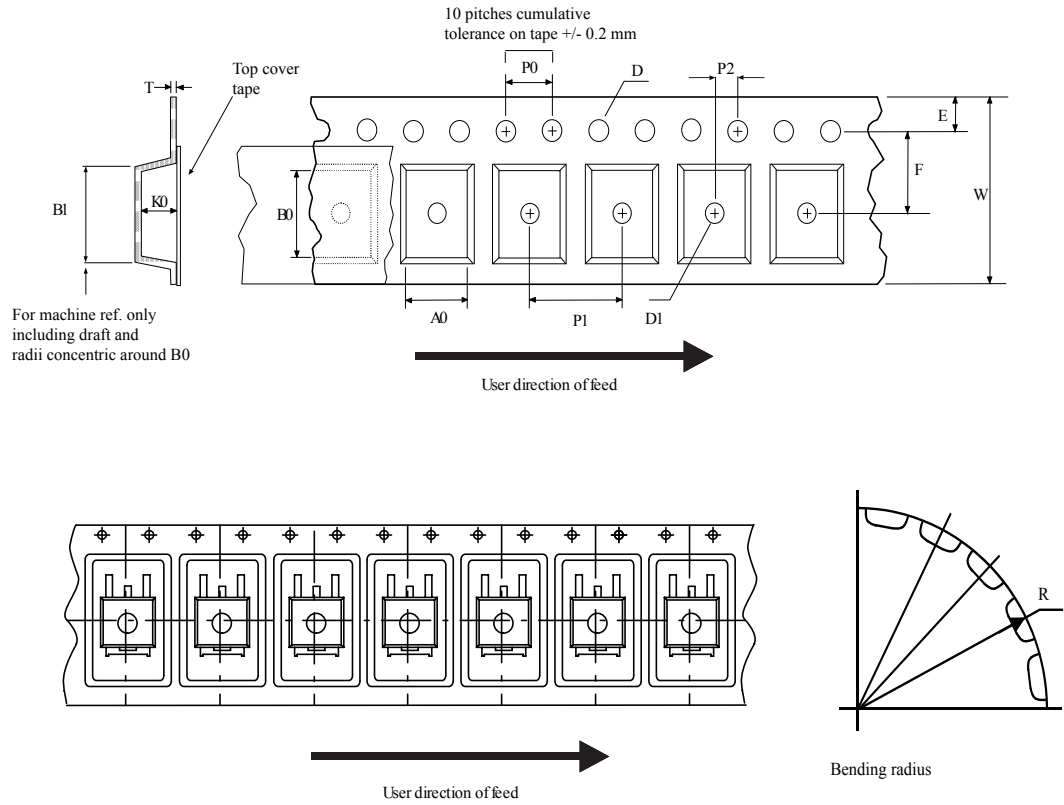
Figure 19. DPAK (TO-252) recommended footprint (dimensions are in mm)



FP\_0068772\_30

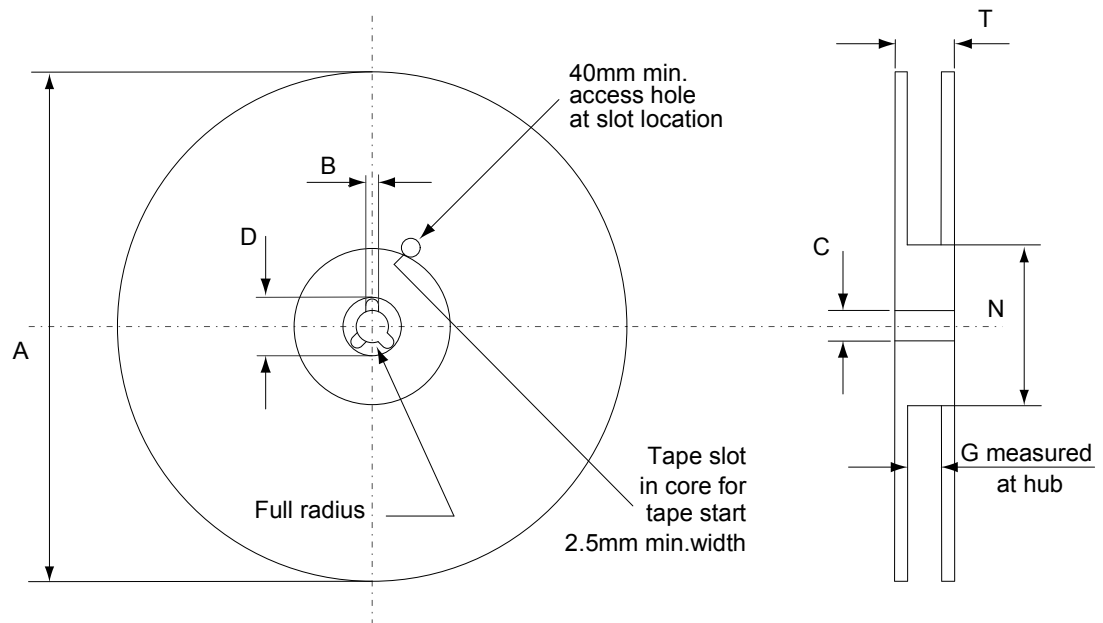
## 4.2 DPAK (TO-252) packing information

Figure 20. DPAK (TO-252) tape outline



AM08852v1

**Figure 21. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
02-Nov-2020	1	First release.

---

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Electrical characteristics (curves) .....	<b>5</b>
<b>3</b>	<b>Test circuits</b> .....	<b>7</b>
<b>4</b>	<b>Package information</b> .....	<b>8</b>
<b>4.1</b>	DPAK (TO-252) type C package information .....	<b>8</b>
<b>4.2</b>	DPAK (TO-252) packing information .....	<b>11</b>
	<b>Revision history</b> .....	<b>13</b>

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved