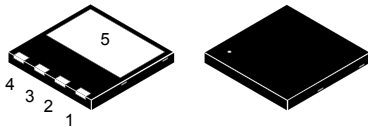
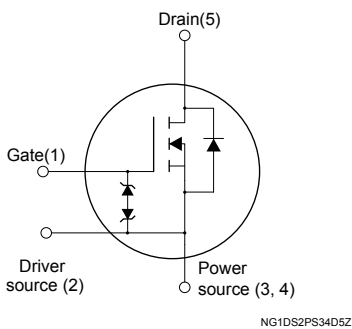


N-channel 600 V, 0.278 Ω typ., 11 A MDmesh M2 Power MOSFET in a PowerFLAT 8x8 HV package



PowerFLAT 8x8 HV



Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D |
|------------|----------|-------------------|-------|
| STL19N60M2 | 600 V | 0.308 Ω | 11 A |

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.



Product status link

[STL19N60M2](#)

Product summary

| | |
|-------------------|------------------|
| Order code | STL19N60M2 |
| Marking | 19N60M2 |
| Package | PowerFLAT 8x8 HV |
| Packing | Tape and reel |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 25 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 11 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 6.9 | A |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 44 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 90 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 15 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | V/ns |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 1.39 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 45 | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of inch^2 , 2oz Cu.

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_J max) | 3 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$) | 135 | mJ |

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|-------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 600 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^\circ\text{C}$ ⁽¹⁾ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 5.5\text{ A}$ | | 0.278 | 0.308 | Ω |

1. Defined by design, not subject to production test.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------|-------------------------------|--|------|-------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 791 | - | pF |
| C_{oss} | Output capacitance | | - | 40 | - | pF |
| C_{riss} | Reverse transfer capacitance | | - | 1.3 | - | pF |
| $C_{oss\ eq.}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0$ to 480 V , $V_{GS} = 0\text{ V}$ | - | 164.5 | - | pF |
| R_G | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 5.6 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 480\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 0$ to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 21.5 | - | nC |
| Q_{gs} | Gate-source charge | | - | 3.2 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 11.3 | - | nC |

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 300\text{ V}$, $I_D = 6.5\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform) | - | 12 | - | ns |
| t_r | Rise time | | - | 9 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 47 | - | ns |
| t_f | Fall time | | - | 10.6 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 11 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 44 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $V_{GS} = 0\text{ V}, I_{SD} = 11\text{ A}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 13\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 305 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 3.3 | | μC |
| I_{RRM} | Reverse recovery current | | - | 22 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 13\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 60\text{ V}, T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 417 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 4.6 | | μC |
| I_{RRM} | Reverse recovery current | | - | 22 | | A |

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

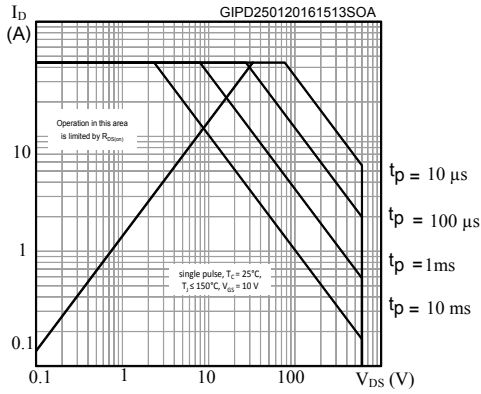


Figure 2. Thermal impedance

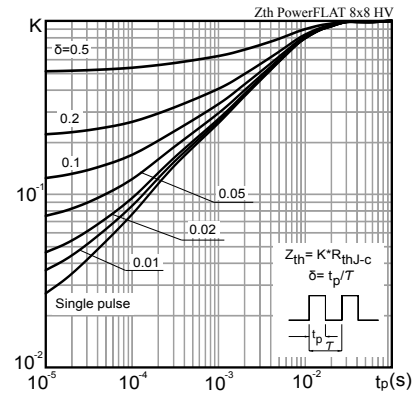


Figure 3. Output characteristics

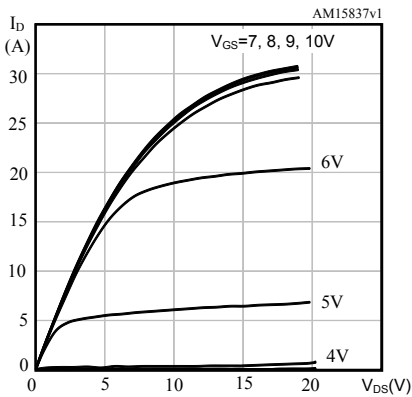


Figure 4. Transfer characteristics

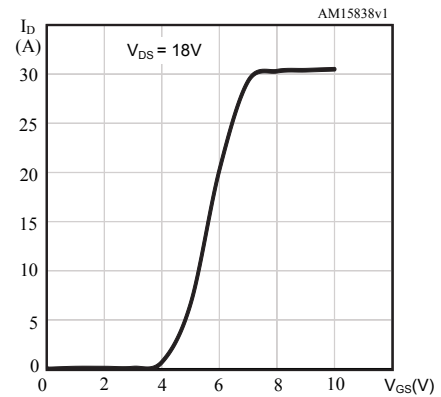


Figure 5. Gate charge vs gate-source voltage

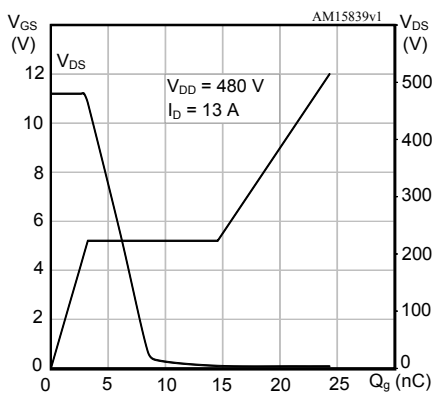


Figure 6. Static drain-source on-resistance

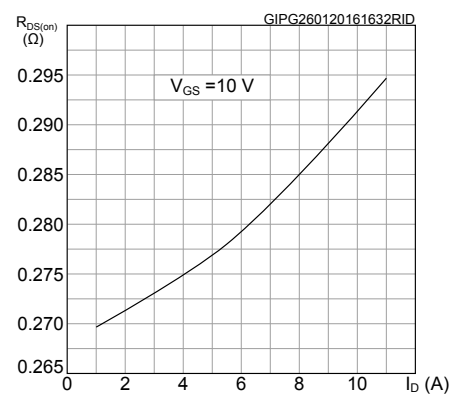


Figure 7. Capacitance variations

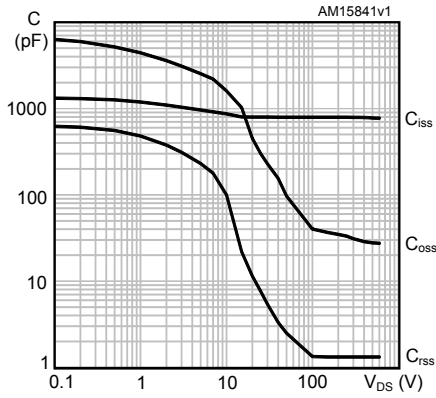


Figure 8. Normalized gate threshold voltage vs temperature

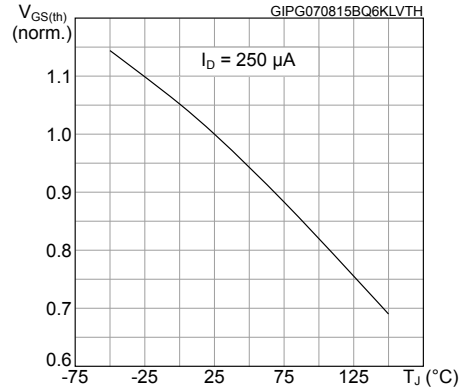


Figure 9. Normalized on-resistance vs temperature

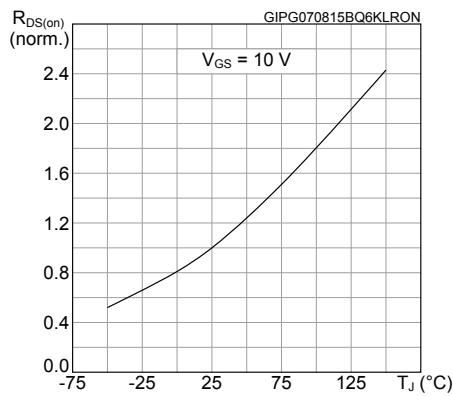


Figure 10. Normalized V_{(BR)DSS} vs temperature

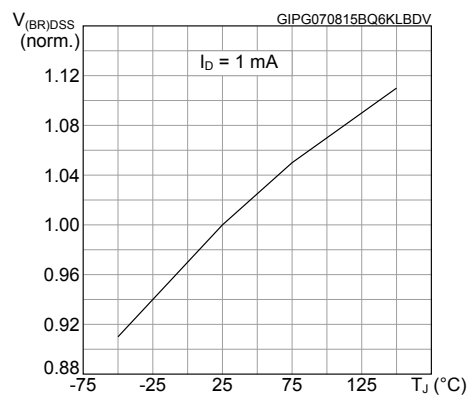


Figure 11. Output capacitance stored energy

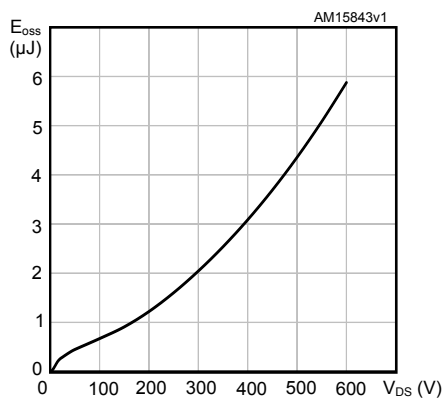
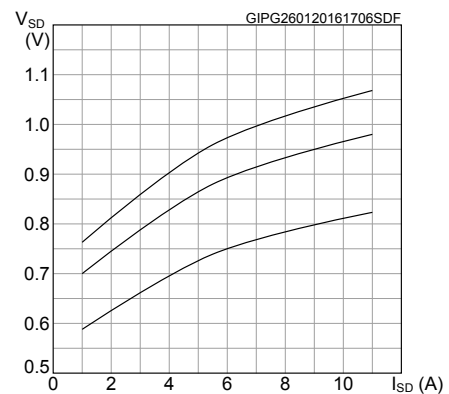
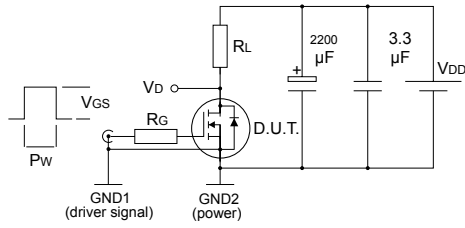


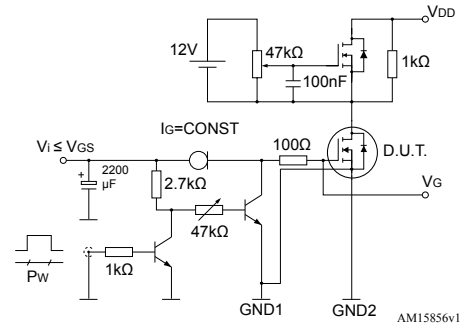
Figure 12. Source-drain diode forward characteristics



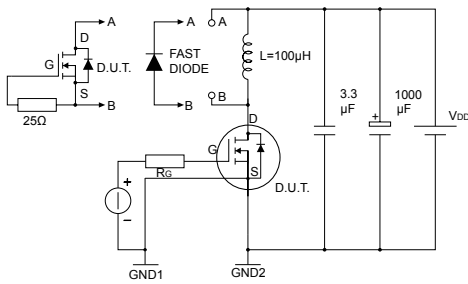
3 Test circuits

Figure 13. Switching times test circuit for resistive load


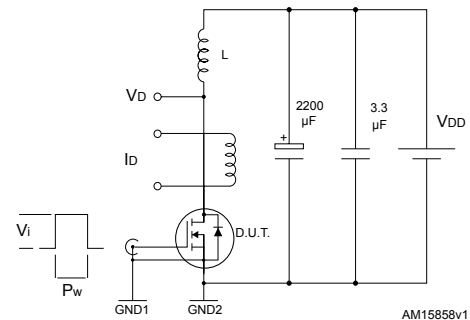
AM15855v1

Figure 14. Test circuit for gate charge behavior


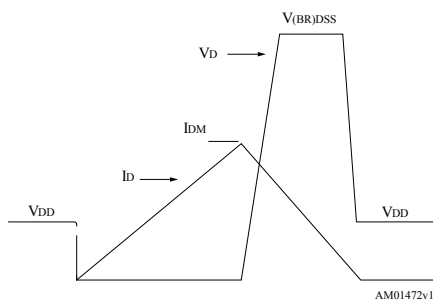
AM15856v1

Figure 15. Test circuit for inductive load switching and diode recovery times


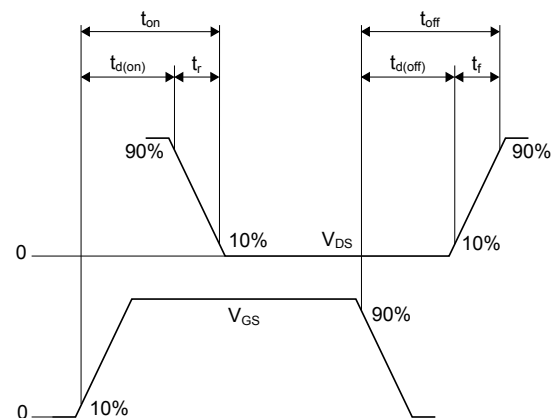
AM15857v1

Figure 16. Unclamped inductive load test circuit


AM15858v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


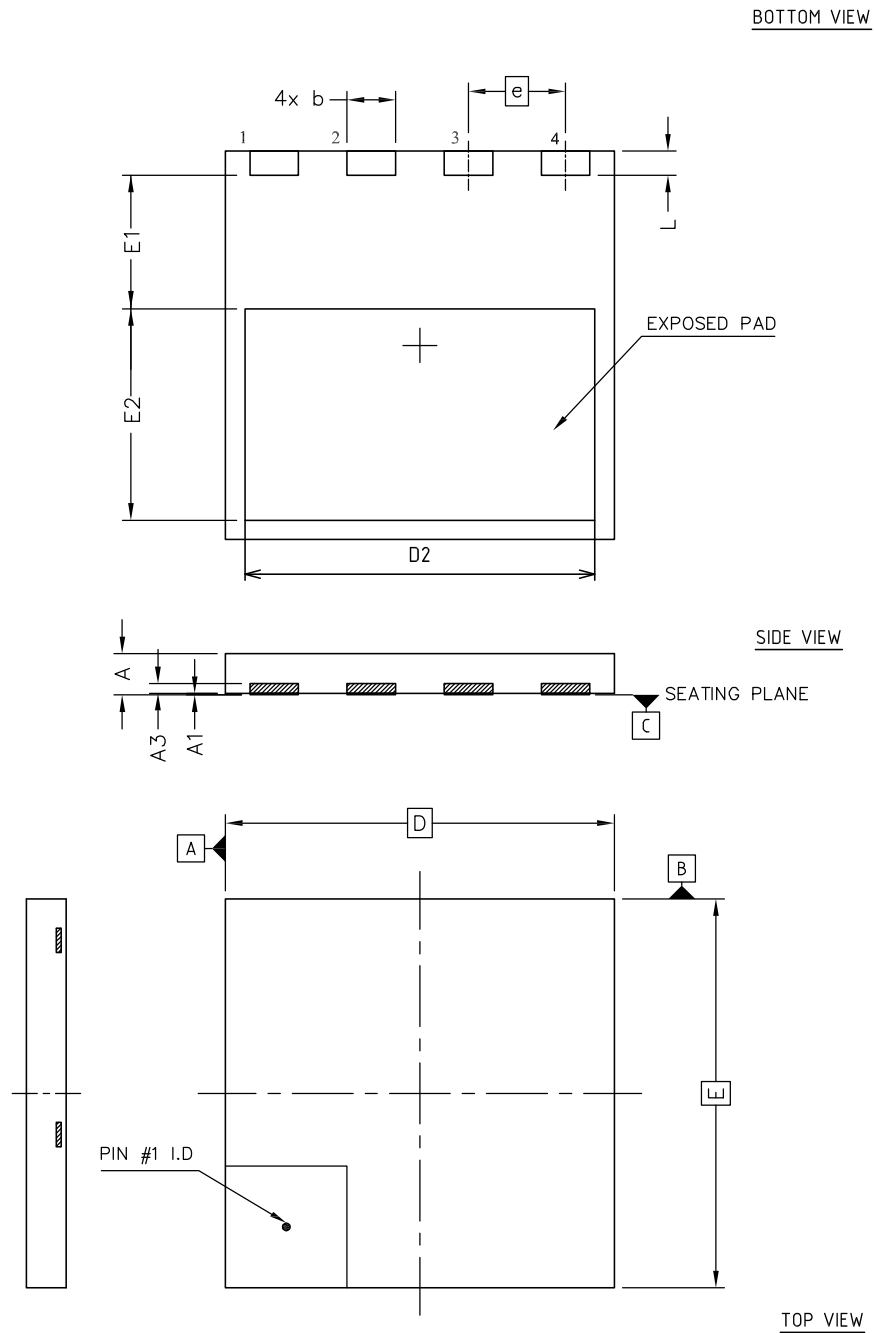
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 PowerFLAT 8x8 HV package information

Figure 19. PowerFLAT 8x8 HV package outline

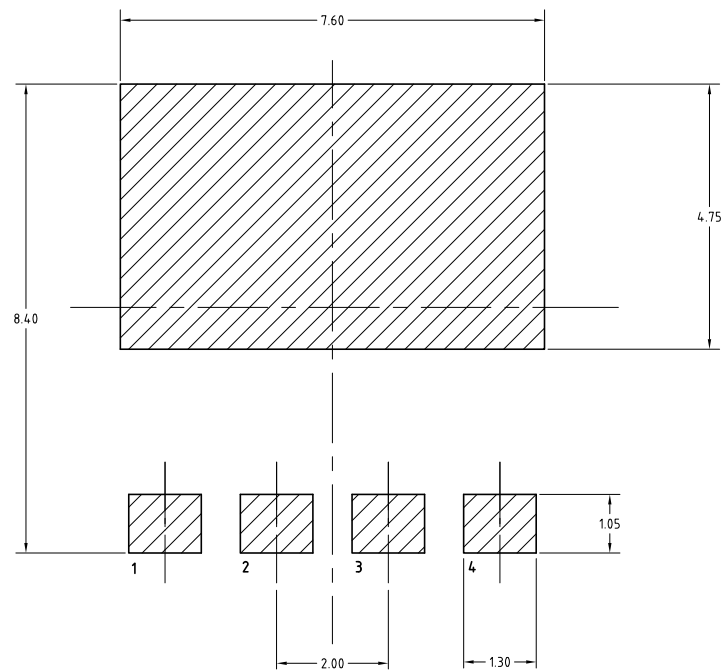


8222871_Rev_4

Table 8. PowerFLAT 8x8 HV mechanical data

| Ref. | Dimensions (in mm) | | |
|------|--------------------|------|------|
| | Min. | Typ. | Max. |
| A | 0.75 | 0.85 | 0.95 |
| A1 | 0.00 | | 0.05 |
| A3 | 0.10 | 0.20 | 0.30 |
| b | 0.90 | 1.00 | 1.10 |
| D | 7.90 | 8.00 | 8.10 |
| E | 7.90 | 8.00 | 8.10 |
| D2 | 7.10 | 7.20 | 7.30 |
| E1 | 2.65 | 2.75 | 2.85 |
| E2 | 4.25 | 4.35 | 4.45 |
| e | 2.00 BSC | | |
| L | 0.40 | 0.50 | 0.60 |

Figure 20. PowerFLAT 8x8 HV footprint

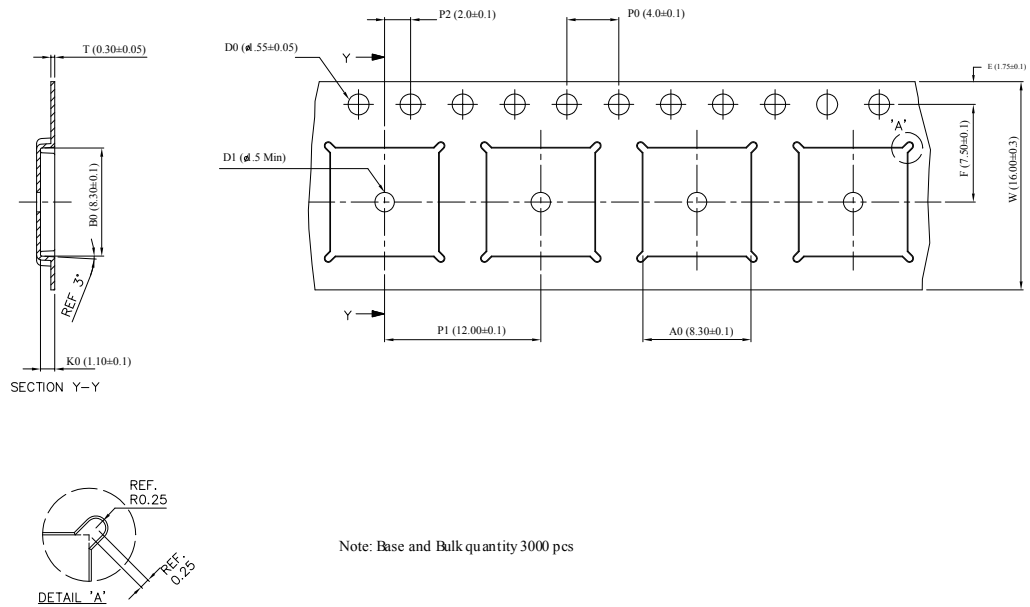


8222871_REV_4_footprint

Note: All dimensions are in millimeters.

4.2 PowerFLAT 8x8 HV packing information

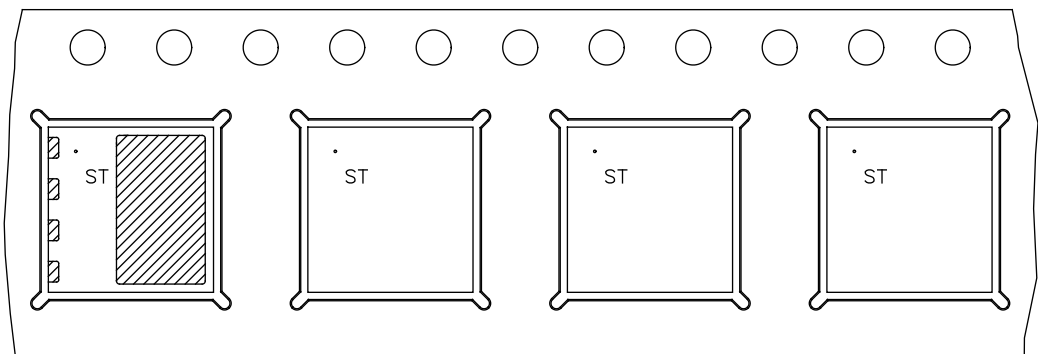
Figure 21. PowerFLAT 8x8 HV tape



8229819_Tape_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT 8x8 HV package orientation in carrier tape



Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 27-Jan-2016 | 1 | First release. |
| 15-Nov-2018 | 2 | Updated <i>Table 1. Absolute maximum ratings</i> , <i>Table 2. Thermal data</i> , <i>Table 4. On/off states</i> , <i>Table 5. Dynamic</i> , <i>Table 6. Switching times</i> , <i>Table 7. Source drain diode</i> and <i>Figure 7. Capacitance variations</i> . |
| 11-Jun-2019 | 3 | Updated description in cover page. Updated Table 5. Dynamic and Table 6. Switching times . Minor text changes. |

Contents

| | | |
|------------|--|-----------|
| 1 | Electrical ratings | 2 |
| 2 | Electrical characteristics | 3 |
| 2.1 | Electrical characteristics (curves) | 5 |
| 3 | Test circuits | 7 |
| 4 | Package information | 8 |
| 4.1 | PowerFLAT 8x8 HV package information | 8 |
| 4.2 | PowerFLAT 8x8 HV packing information | 9 |
| | Revision history | 12 |

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved