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March 2011

## **FDMS2734**

# N-Channel UltraFET Trench<sup>®</sup> MOSFET 250V, 14A, 122m $\Omega$

#### **Features**

- Max  $r_{DS(on)}$  = 122m $\Omega$  at  $V_{GS}$  = 10V,  $I_D$  = 2.8A
- Max  $r_{DS(on)}$  = 130m $\Omega$  at  $V_{GS}$  = 6V,  $I_D$  = 1.7A
- Low Miller Charge
- Optimized efficiency at high frequencies
- RoHS Compliant

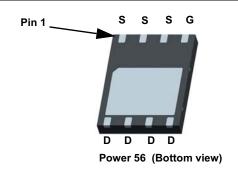
## **General Description**

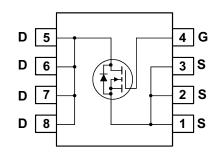
UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for  $r_{DS(on)}$ , low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

## **Application**

■ DC - DC Conversion







## **MOSFET Maximum Ratings** T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
$V_{DS}$	Drain to Source Voltage			250	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous (Silicon limited)	T <sub>C</sub> = 25°C		14	
I <sub>D</sub>	-Continuous	T <sub>A</sub> = 25°C	(Note 1a)	2.8	Α
	-Pulsed			30	
В	Power Dissipation	T <sub>C</sub> = 25°C		78	w
$P_{D}$	Power Dissipation $T_A = 25^{\circ}C$ (Note 1a)		(Note 1a)	2.5	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature F	Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	C/VV

### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS2734	FDMS2734	Power 56	13"	12mm	3000 units

## Electrical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	octeristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	250			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		250		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200V,			1	μΑ
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20V, V_{GS} = 0V$			±100	nA

### On Characteristics (Note 2)

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, referenced to 25°C		-11		mV/°C
		$V_{GS} = 10V, I_D = 2.8A$		105	122	
r <sub>DS(on)</sub>	r <sub>DS(on)</sub> Drain to Source On Resistance	$V_{GS} = 6V$ , $I_{D} = 1.7A$		110	130	mΩ
	$V_{GS} = 10V$ , $I_D = 2.8A$ $T_J = 125$ °C		217	258		
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10V, I_D = 2.8A$		11		S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V - 400V V - 0V	1775	2365	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, f = 1MHz	80	110	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1141112	25	40	pF
$R_g$	Gate Resistance	f = 1MHz	0.9		Ω

## **Switching Characteristics**

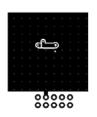
t <sub>d(on)</sub>	Turn-On Delay Time	., ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,		22	36	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 125V, I_{D} = 2.8A$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		10	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	V <sub>GS</sub> = 10V, R <sub>GEN</sub> = 652		36	58	ns
t <sub>f</sub>	Fall Time			12	22	ns
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V \text{ to } 10V V_{DD} = 125V$		30	42	nC
$Q_{gs}$	Gate to Source Gate Charge	I <sub>D</sub> = 2.8A		7		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			9		nC

#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.8A (Note 2)	0.75	1.20	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 2.8A. di/dt = 100A/us	79	119	ns
Q <sub>rr</sub>	Reverse Recovery Charge	1F - 2.6A, αι/αι - 100A/μS	214	321	nC

#### Notes

<sup>1:</sup> R<sub>0JA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a. 50°C/W when mounted on a 1 in² pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper



2: Pulse Test: Pulse Width < 300 $\mu$ s, Duty cycle < 2.0%.

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### Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

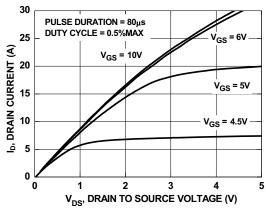


Figure 1. On Region Characteristics

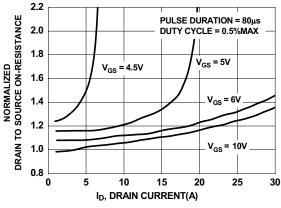


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

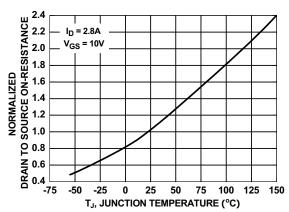


Figure 3. Normalized On Resistance vs Junction Temperature

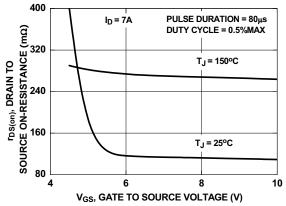


Figure 4. On-Resistance vs Gate to Source Voltage

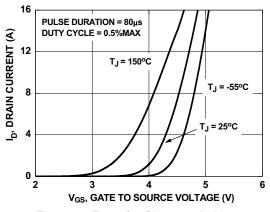


Figure 5. Transfer Characteristics

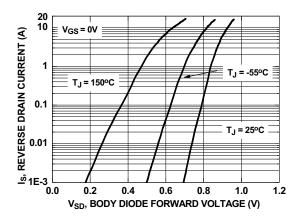


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

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## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

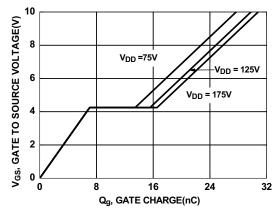
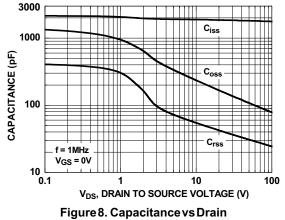


Figure 7. Gate Charge Characteristics



to Source Voltage

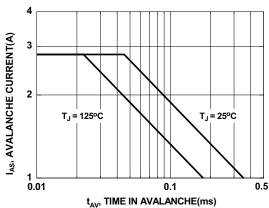


Figure 9. Unclamped Inductive **Switching Capability** 

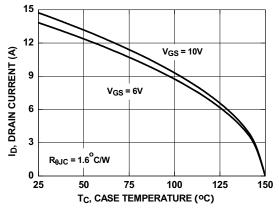


Figure 10. Maximum Continuous Drain **Current vs Case Temperature** 

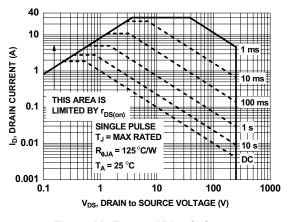


Figure 11. Forward Bias Safe **Operating Area** 

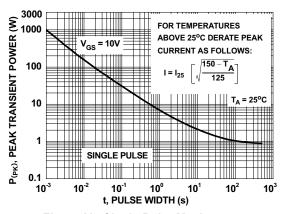


Figure 12. Single Pulse Maximum **Power Dissipation** 

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## Typical Characteristics T<sub>J</sub> = 25°C unless otherwise noted

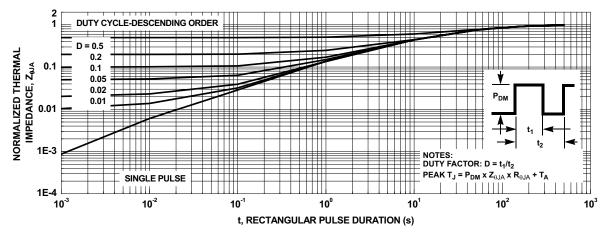
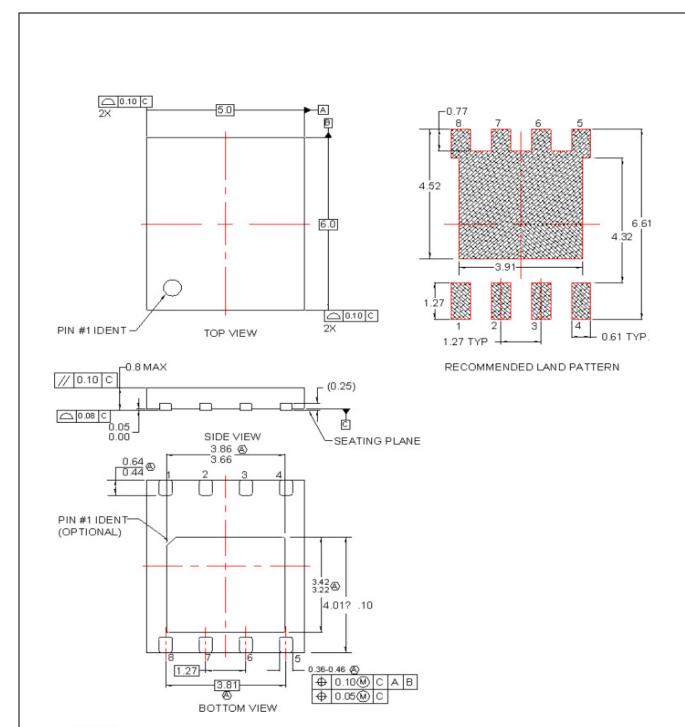


Figure 13. Transient Thermal Response Curve



#### NOTES:

- (A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229. DATED 11/2001.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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