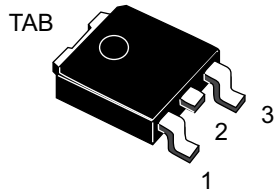
STD4NK100Z

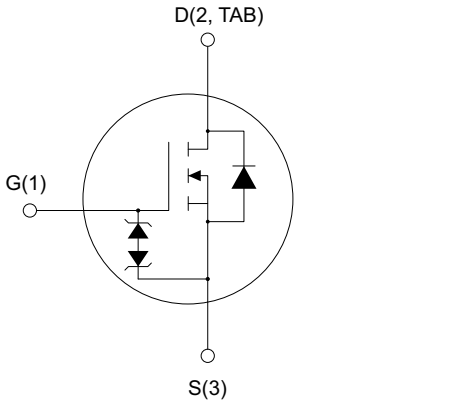
Automotive-grade N-channel 1000 V, 5.6 Ω typ., 2.2 A SuperMESH™ Power MOSFET Zener-protected in a DPAK

Datasheet - production data



DPAK

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)max}$	I_D
STD4NK100Z	1000 V	6.8 Ω	2.2 A

- Designed for automotive applications and AEC-Q101 qualified
- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching application

Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1. Device summary

Order code	Marking	Package	Packaging
STD4NK100Z	4NK100Z	DPAK	Tape and reel

Note: HTRB test has been performed at 80% of $V_{(BR)DSS}$ according to AEC-Q101 rev. C. All the other tests have been done according to the new rev. D.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1000	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	2.2	A
I_D	Drain current (continuous) at T_C=100 °C	1	A
I_{DM}(1)	Drain current (pulsed)	8.8	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	W
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100pF, R=1.5 kΩ)	3000	V
d_v/d_t (2)	Peak diode recovery voltage slope	4.5	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 2.2$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.39	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb max	50	°C/W

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{JMAX})	2.2	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	110	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	1000			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 1000 V, V_{DS} = 1000 V, Tc = 125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{GS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 1.1 A		5.6	6.8	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	601	-	pF
C_{oss}	Output capacitance		-	53	-	pF
C_{rss}	Reverse transfer capacitance		-	12	-	pF
$C_{oss.\ eq}$ (1)	Equivalent output capacitance	V_{GS}=0, V_{DS} =0 V to 800 V	-	15	-	pF
$t_{d(on)}$	Turn-on delay time	V_{DD}=500 V, I_D= 1.25 A, R_G=4.7 Ω, V_{GS}=10 V (see *Figure 16*)	-	15	-	ns
t_r	Rise time		-	7.5	-	ns
$t_{d(off)}$	Off-voltage rise time		-	32	-	ns
t_f	Fall time		-	39	-	ns
Q_g	Total gate charge	V_{DD}=800 V, I_D = 2.5 A V_{GS} =10 V (see *Figure 15*)	-	18	-	nC
Q_{gs}	Gate-source charge		-	3.6	-	nC
Q_{gd}	Gate-drain charge		-	9.2	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.2	A
I_{SDM}(1)	Source-drain current (pulsed)		-		8.8	A
V_{SD}(2)	Forward on voltage	I_{SD}= 2.2 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD}= 2.5 A, di/dt = 100 A/µs, V_{DD}=100 V (see *Figure 14*)	-	584		ns
Q_{rr}	Reverse recovery charge		-	2.3		µC
I_{RRM}	Reverse recovery current		-	8		A
t_{rr}	Reverse recovery time	I_{SD}= 2.5 A, di/dt = 100 A/µs, V_{DD}=100 V, T_j=150 °C (see *Figure 14*)	-	628		ns
Q_{rr}	Reverse recovery charge		-	2.5		µC
I_{RRM}	Reverse recovery current		-	8.1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{gs}=± 1 mA, I_D=0	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

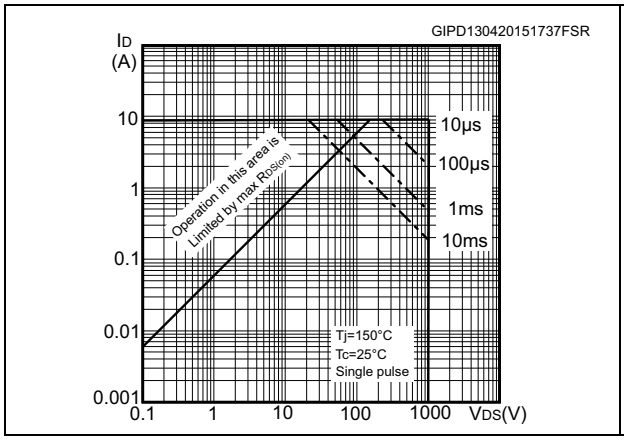


Figure 3. Thermal impedance

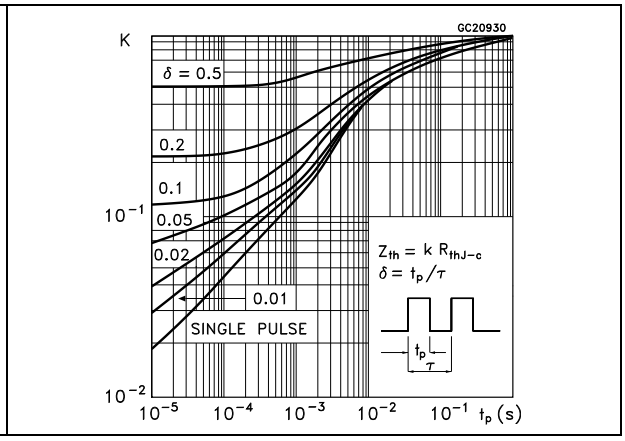


Figure 4. Output characteristics

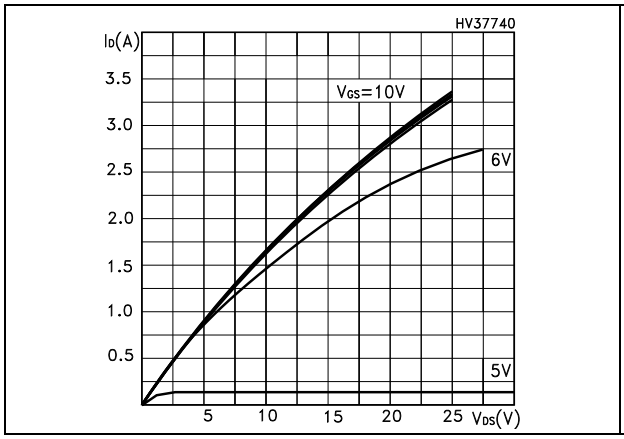


Figure 5. Transfer characteristics

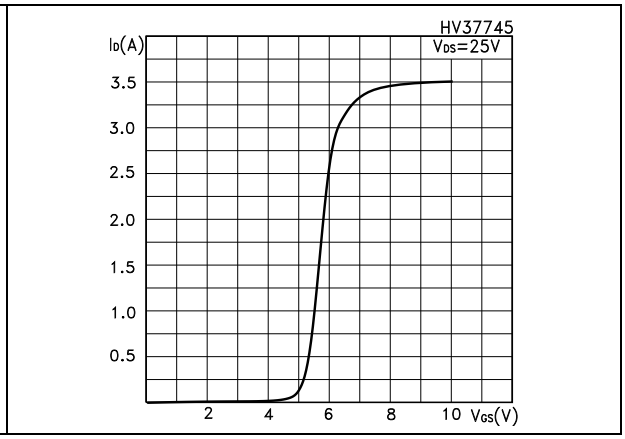


Figure 6. Normalized $V_{(BR)DSS}$ vs. temperature

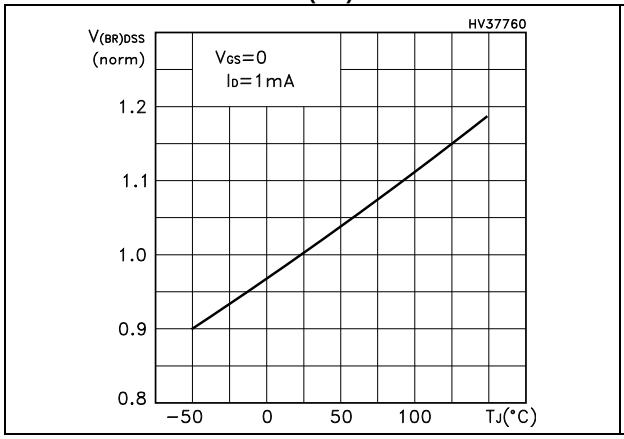


Figure 7. Static drain-source on-resistance

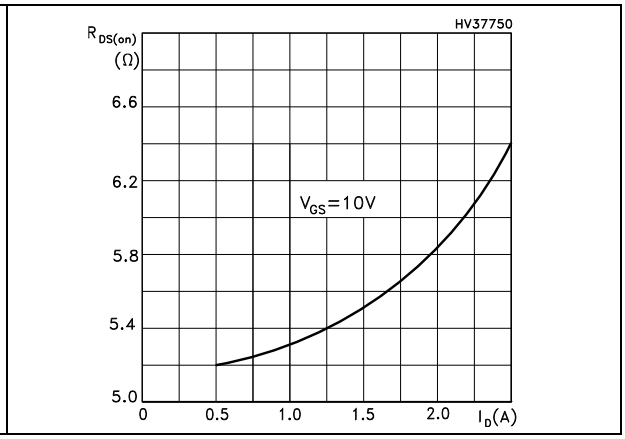


Figure 8. Gate charge vs. gate-source voltage

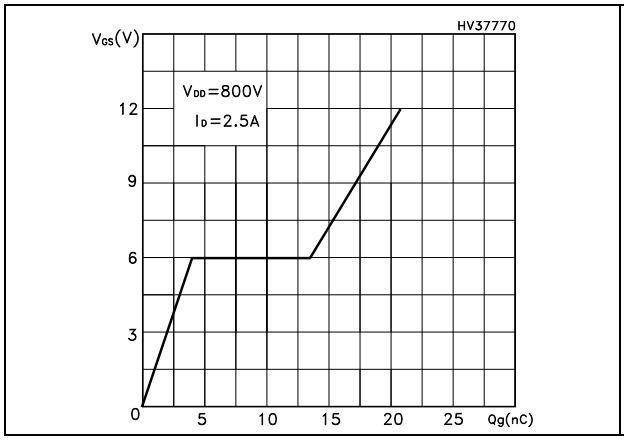


Figure 9. Capacitance variations

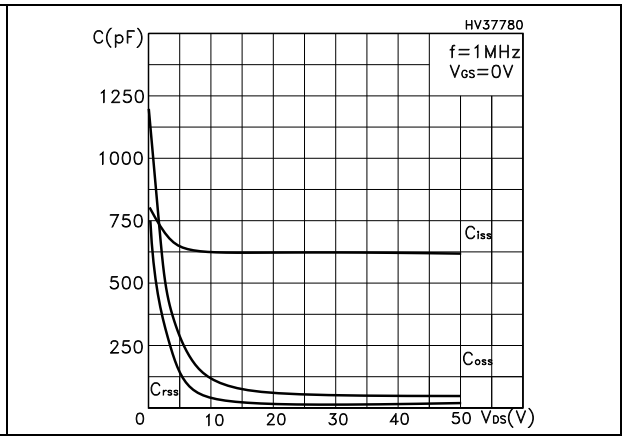


Figure 10. Normalized gate threshold voltage vs. temperature

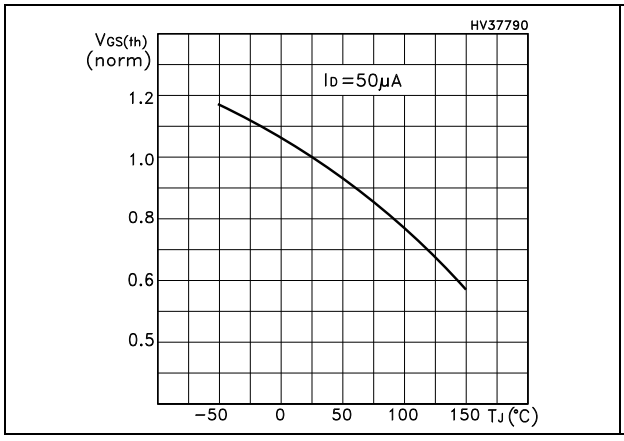


Figure 11. Normalized on-resistance vs. temperature

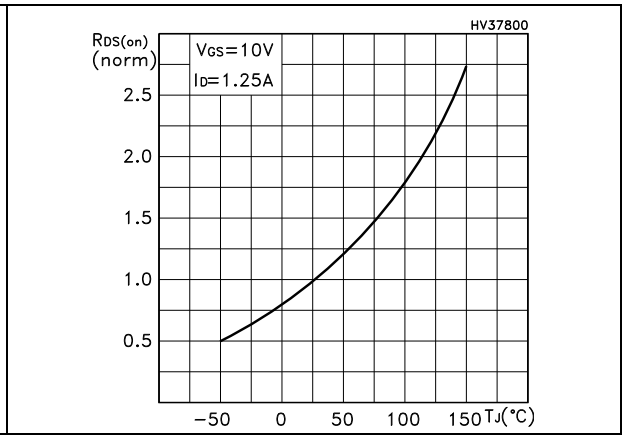


Figure 12. Source-drain diode forward characteristics

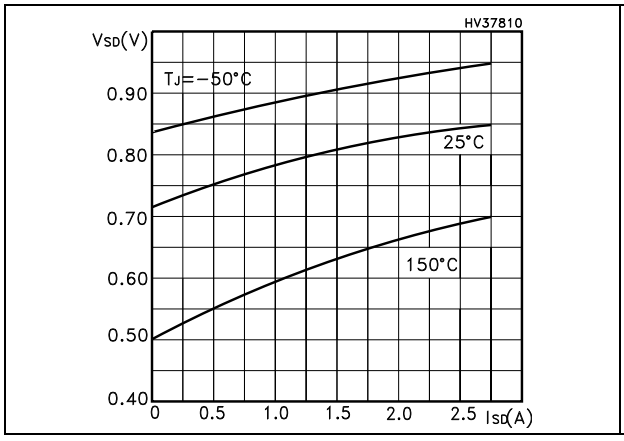
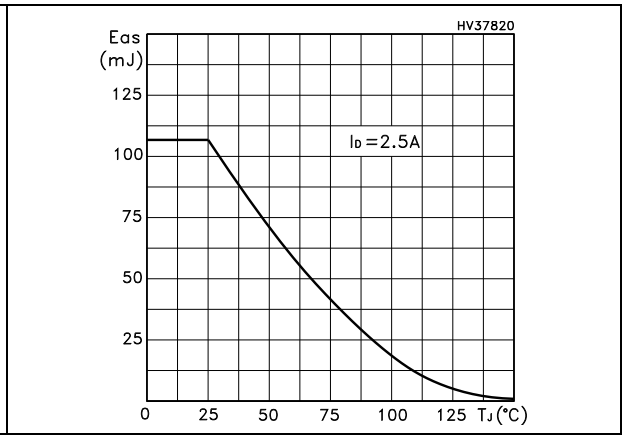


Figure 13. Maximum avalanche energy vs Tj



3 Test circuits

Figure 14. Switching times test circuit for resistive load

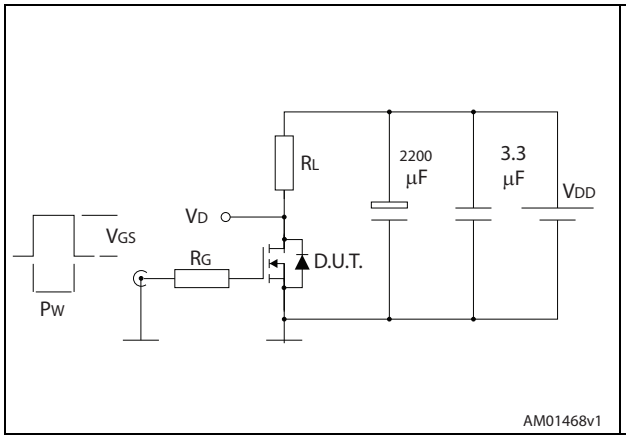


Figure 15. Gate charge test circuit

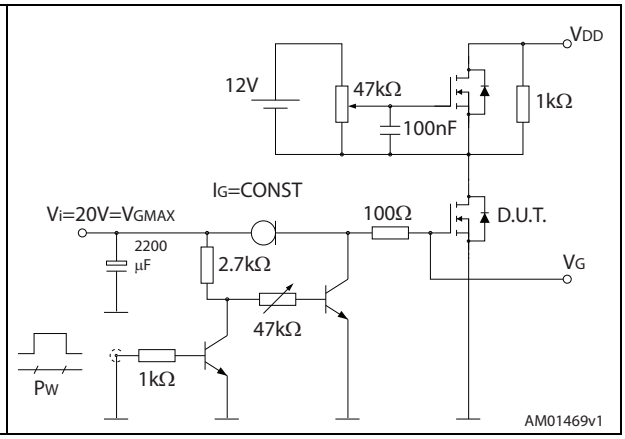


Figure 16. Test circuit for inductive load switching and diode recovery times

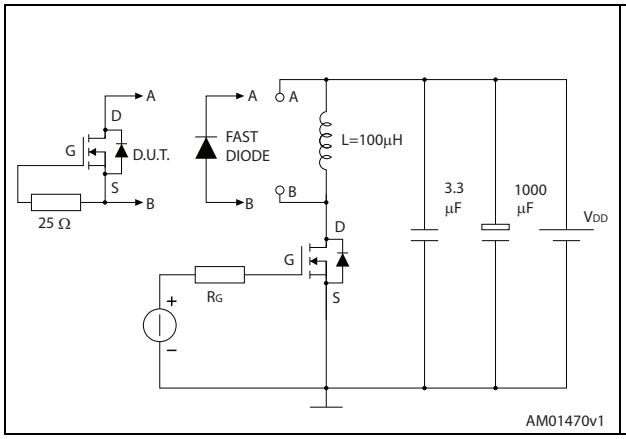


Figure 17. Unclamped inductive load test circuit

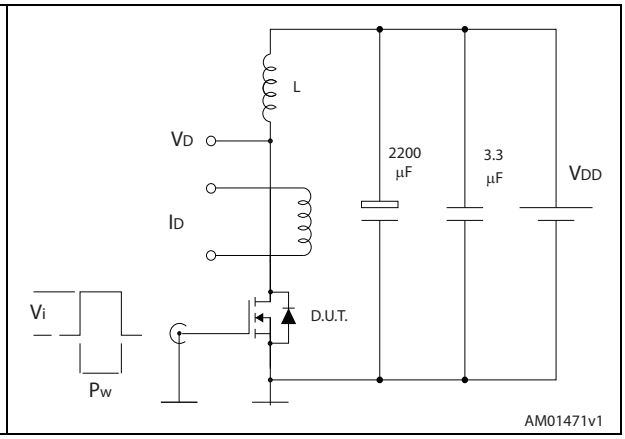


Figure 18. Unclamped inductive waveform

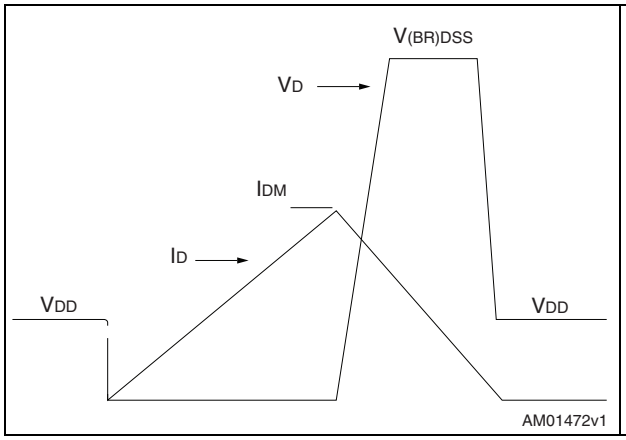
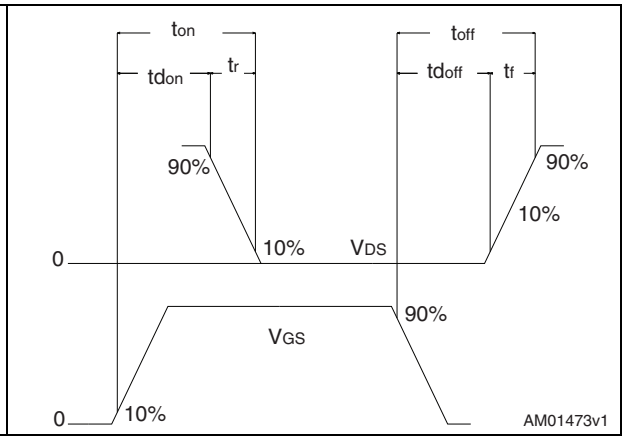


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 20. DPAK (TO-252) type A2 outline

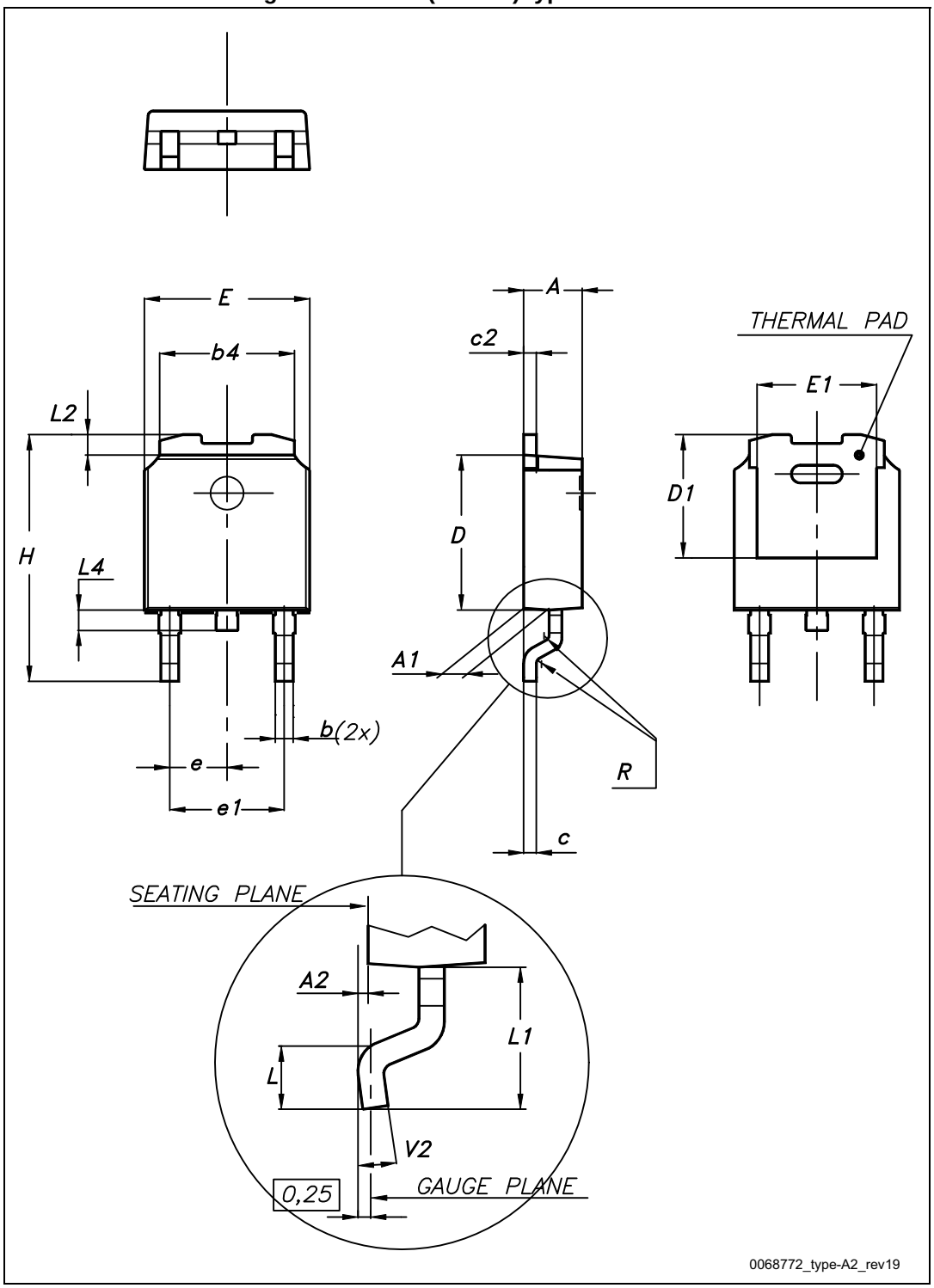
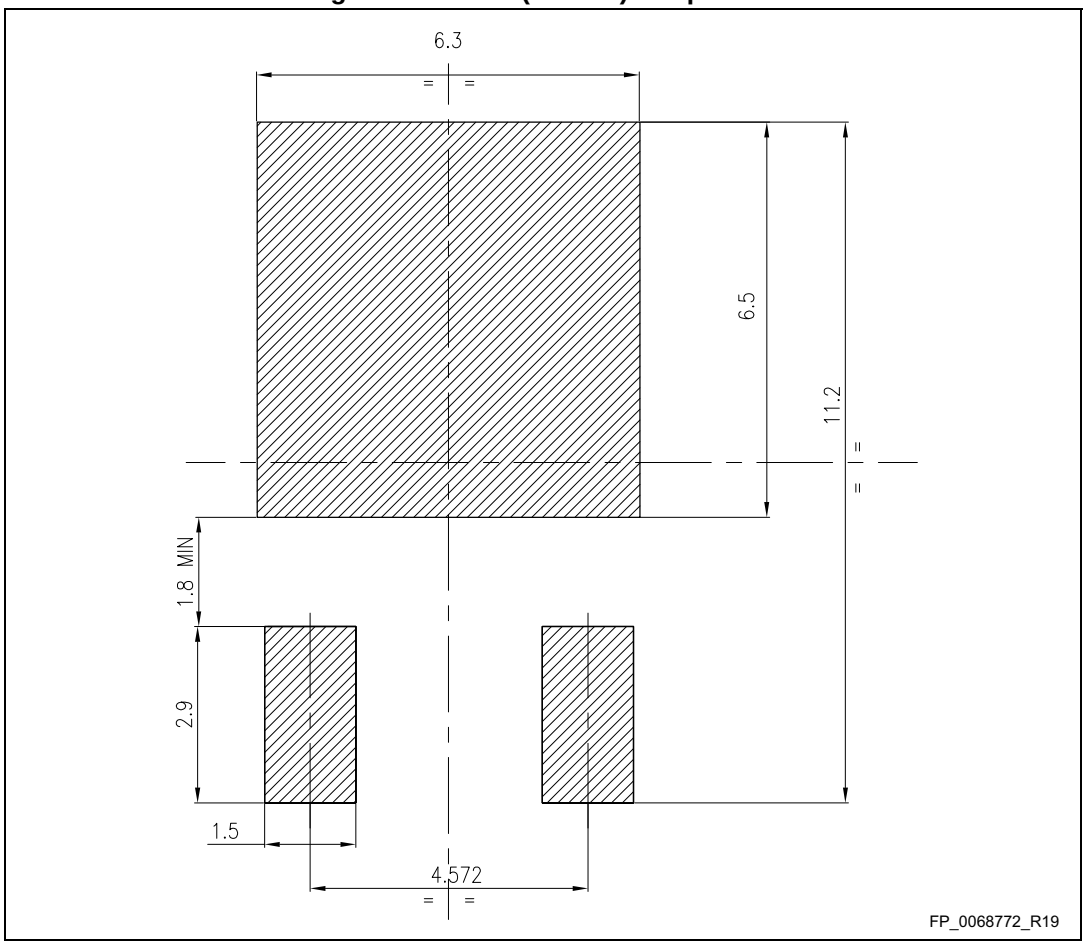


Table 9. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21. DPAK (TO-252) footprint [(a)]



a. All dimensions are in millimeters

5 Packing information

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape for DPAK (TO-252)

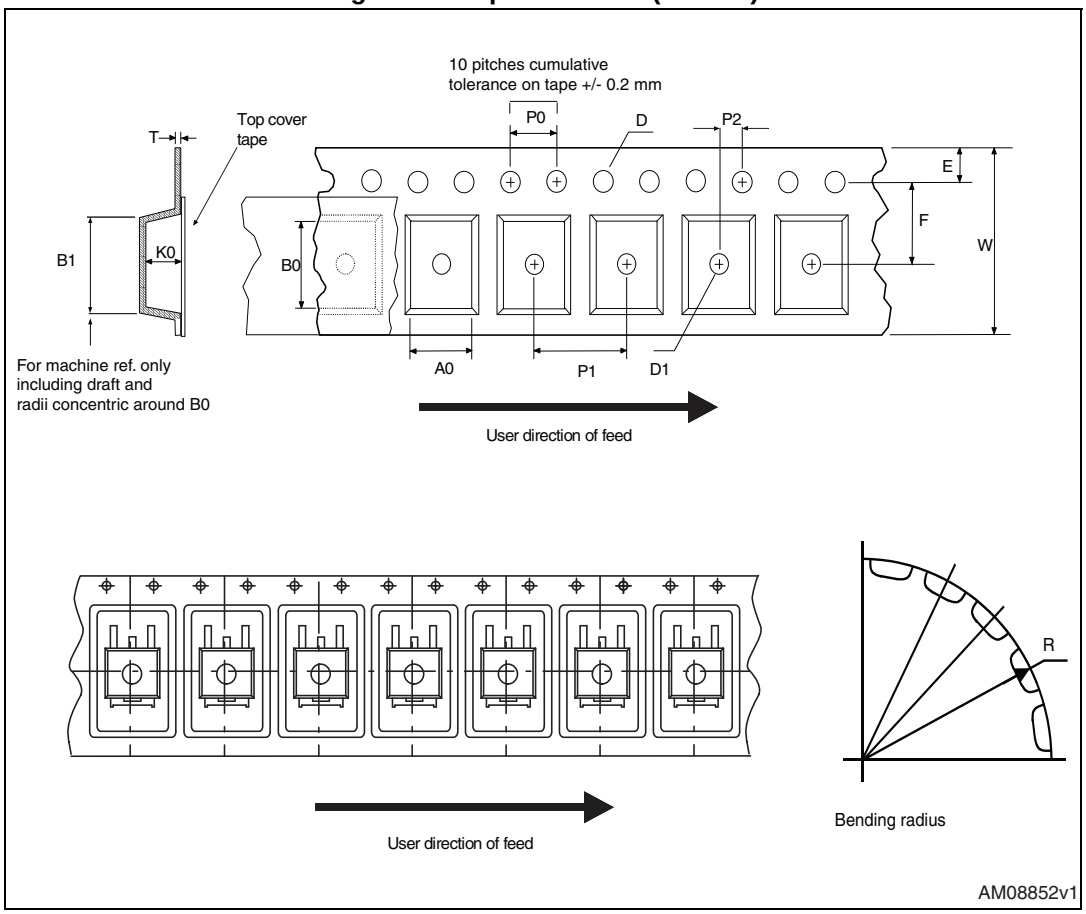
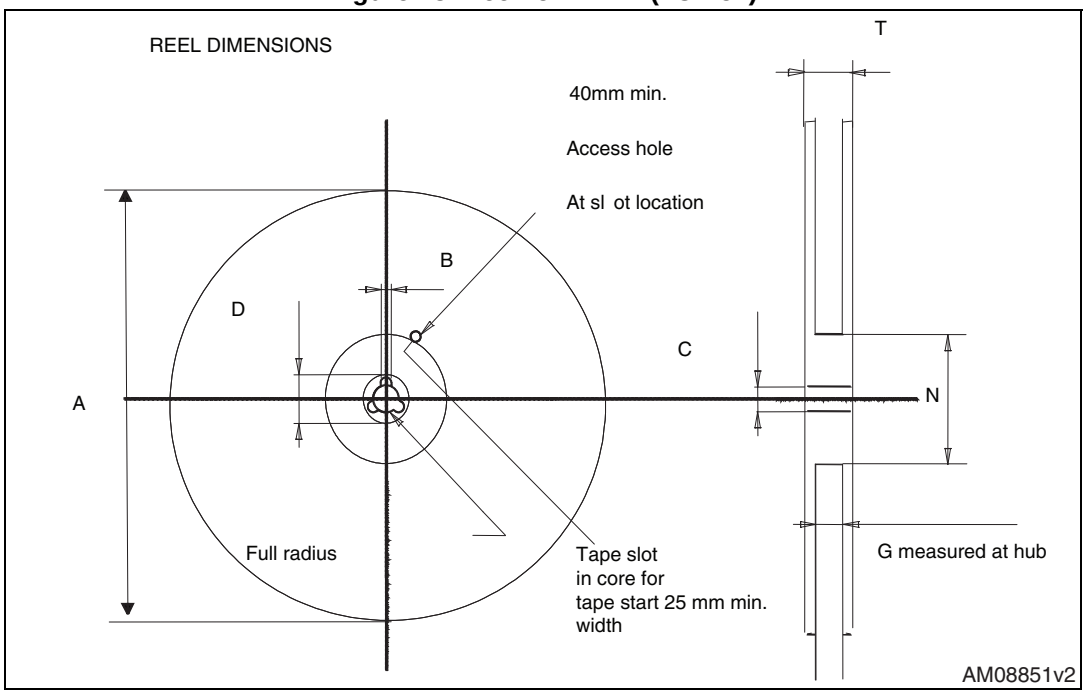


Figure 23. Reel for DPAK (TO-252)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
01-Oct-2013	1	First release.
13-Apr-2015	2	Document status promoted from preliminary to production data. Updated title and features in cover page. Updated *Section 2.1: Electrical characteristics (curves)* and *Section 4: Package information*. Minor text changes.