NTD4804NA

Advance Information

Power MOSFET

25 V, 117 A, Single N−Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb−Free Devices

Applications

- CPU Power Delivery
- DC−DC Converters
- Low Side Switching

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	Steady State	T_A = 25°C	I_D	19	A
		T_A = 85°C		15	
Power Dissipation ($R_{\theta JA}$) (Note 1)		T_A = 25°C	P_D	2.5	W
Continuous Drain Current ($R_{\theta JA}$) (Note 2)		T_A = 25°C	I_D	14.5	A
		T_A = 85°C		11	
Power Dissipation ($R_{\theta JA}$) (Note 2)		T_A = 25°C	P_D	1.43	W
Continuous Drain Current ($R_{\theta JC}$) (Note 1)		T_C = 25°C	I_D	117	A
		T_C = 85°C		91	
Power Dissipation ($R_{\theta JC}$) (Note 1)		T_C = 25°C	P_D	93.75	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	230	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	78	A
Drain to Source dV/dt			dV/dt	6.0	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 30 V, V_{GS} = 10 V, L = 1.0 mH, $I_{L(pk)}$ = 30 A, R_G = 25 Ω)			E_{AS}	450	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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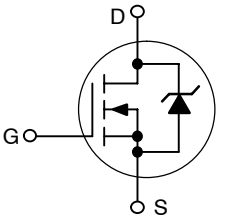
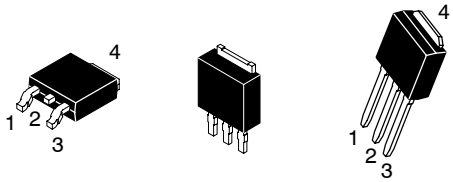
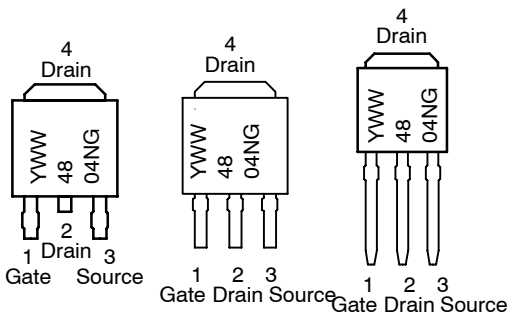
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
25 V	4.0 mΩ @ 10 V	117 A
	5.5 mΩ @ 4.5 V	





DPAK (Bend Lead) CASE 369C STYLE 2 | **3 IPAK (Straight Lead) CASE 369AD** | **DPAK (Straight Lead) CASE 369D STYLE 2**

MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
WW = Work Week
4804N = Device Code
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	1.6	°C/W
Junction−to−TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	60	
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	105	

1. Surface−mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				7.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 to 11.5 V	I_D = 30 A		3.4	4.0	mΩ
			I_D = 15 A		3.4		
		V_{GS} = 4.5 V	I_D = 30 A		4.7	5.5	
			I_D = 15 A		4.6		
Forward Transconductance	gFS	V_{DS} = 15 V, I_D = 15 A			23		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			4490		pF
Output Capacitance	C_{oss}				952		
Reverse Transfer Capacitance	C_{rss}				556		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 30 A			30	40	nC
Threshold Gate Charge	$Q_{G(TH)}$				5.5		
Gate−to−Source Charge	Q_{GS}				13		
Gate−to−Drain Charge	Q_{GD}				13		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 30 A			73		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			28		ns
Rise Time	t_r				256		
Turn−Off Delay Time	$t_{d(off)}$				23		
Fall Time	t_f				73		
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 30 A, R_G = 3.0 Ω			13		ns
Rise Time	t_r				88		
Turn−Off Delay Time	$t_{d(off)}$				36		
Fall Time	t_f				29		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.81	1.2	V
			T_J = 125°C		0.72		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 30 A			34		ns
Charge Time	ta				19		
Discharge Time	tb				15		
Reverse Recovery Time	Q_{RR}				30		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			2.49		nH
Drain Inductance, DPAK	L_D				0.0164		
Drain Inductance, IPAK	L_D				1.88		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				0.6		Ω

TYPICAL PERFORMANCE CURVES

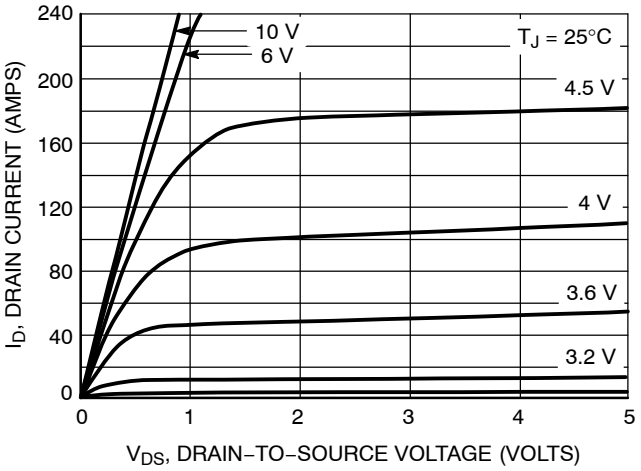


Figure 1. On−Region Characteristics

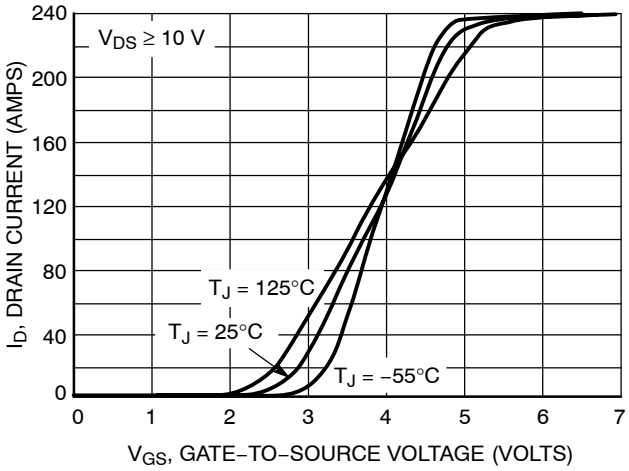


Figure 2. Transfer Characteristics

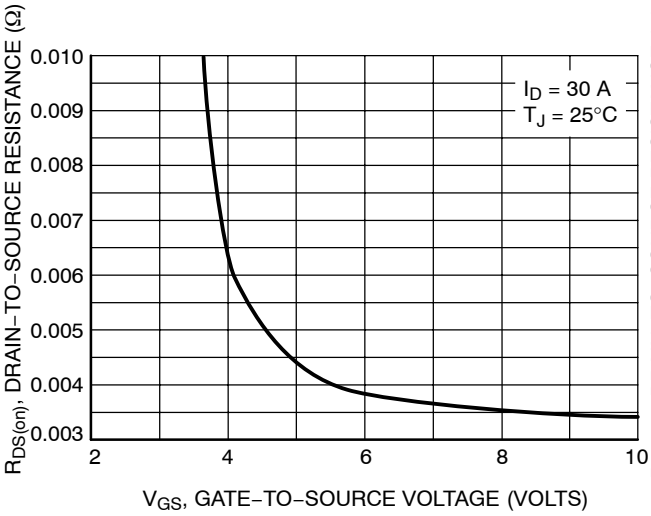


Figure 3. On−Resistance vs. Gate−to−Source Voltage

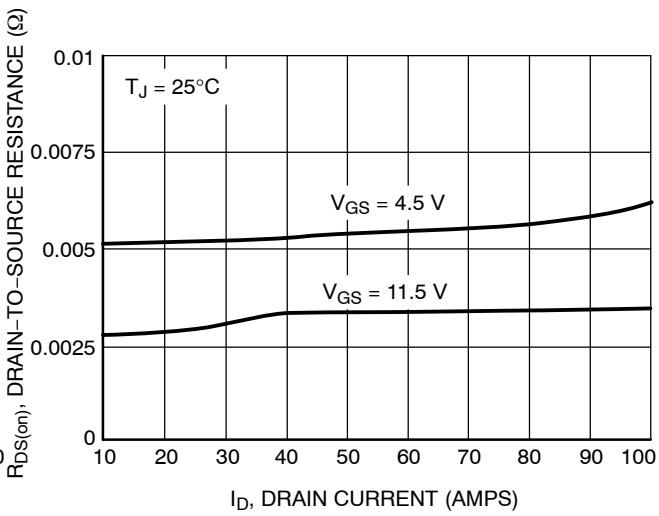


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

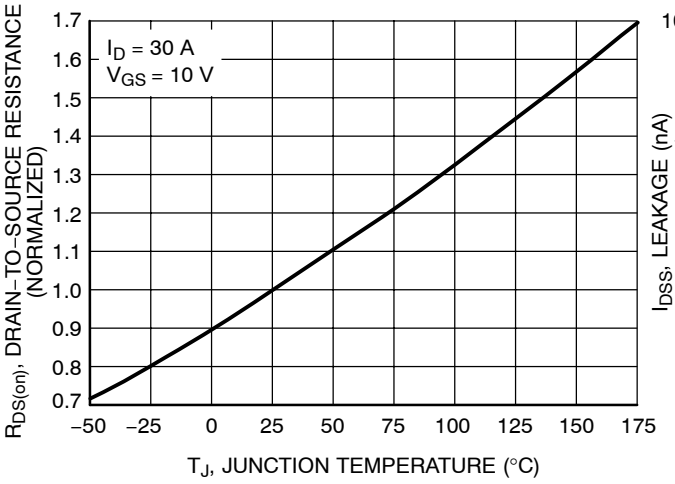


Figure 5. On−Resistance Variation with Temperature

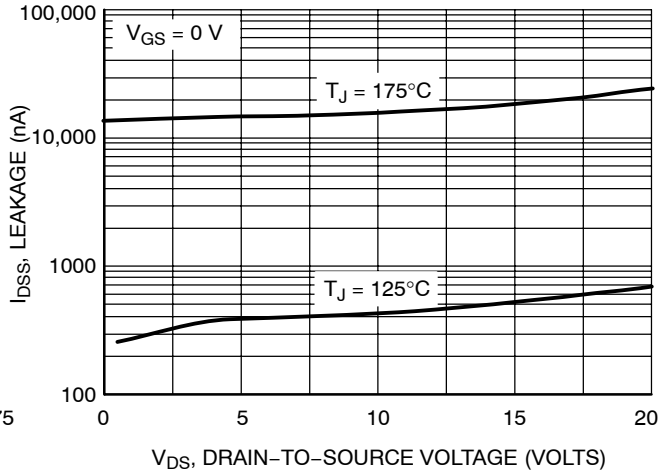


Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

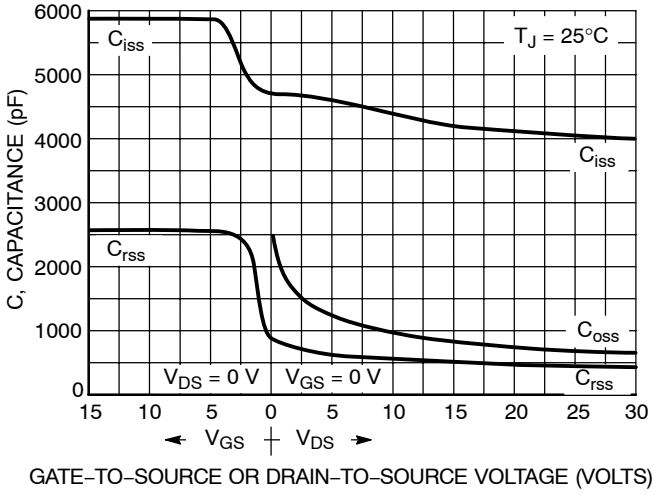


Figure 7. Capacitance Variation

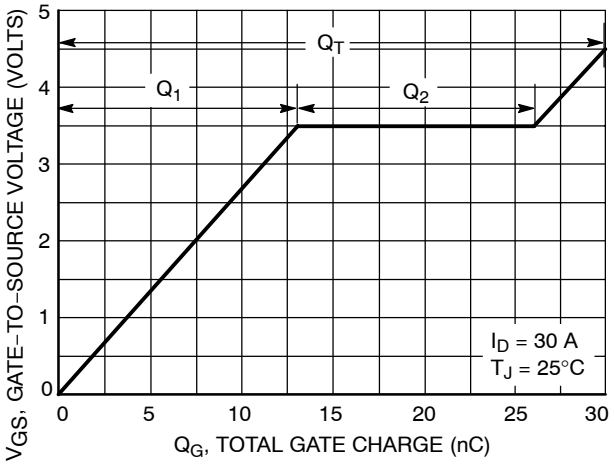


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

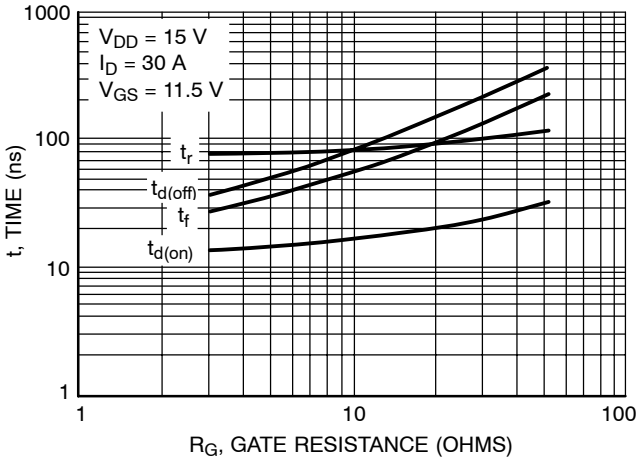


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

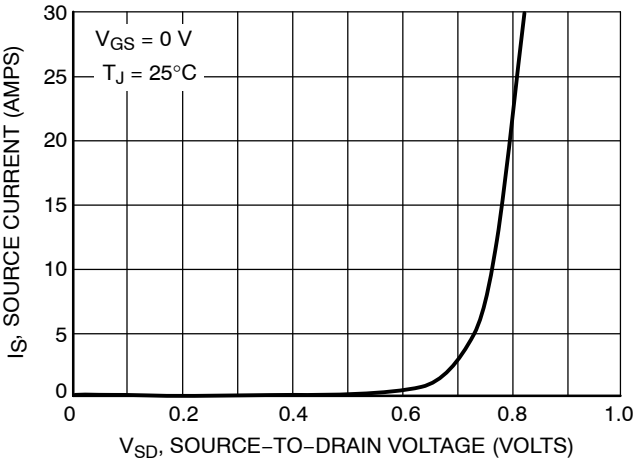


Figure 10. Diode Forward Voltage vs. Current

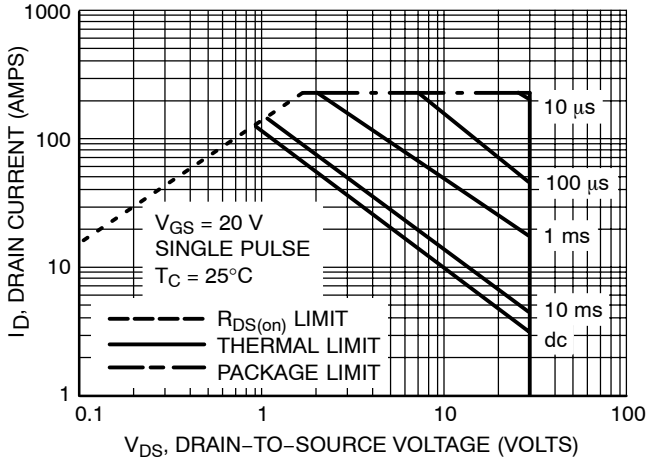


Figure 11. Maximum Rated Forward Biased Safe Operating Area

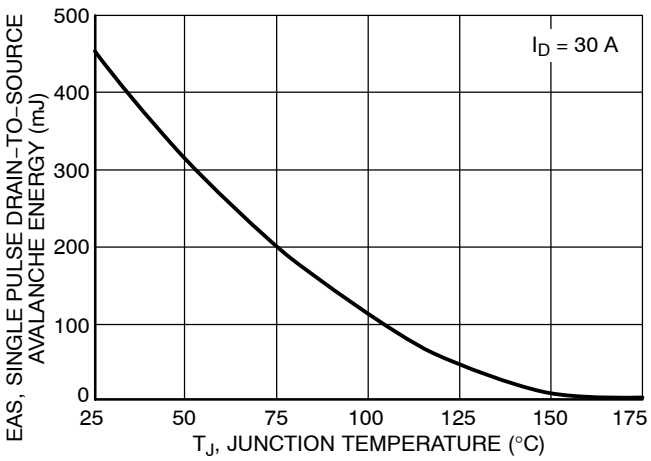


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

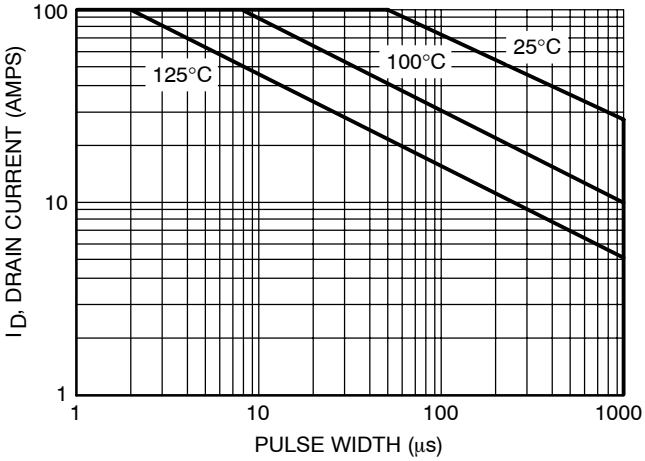


Figure 13. Avalanche Characteristics

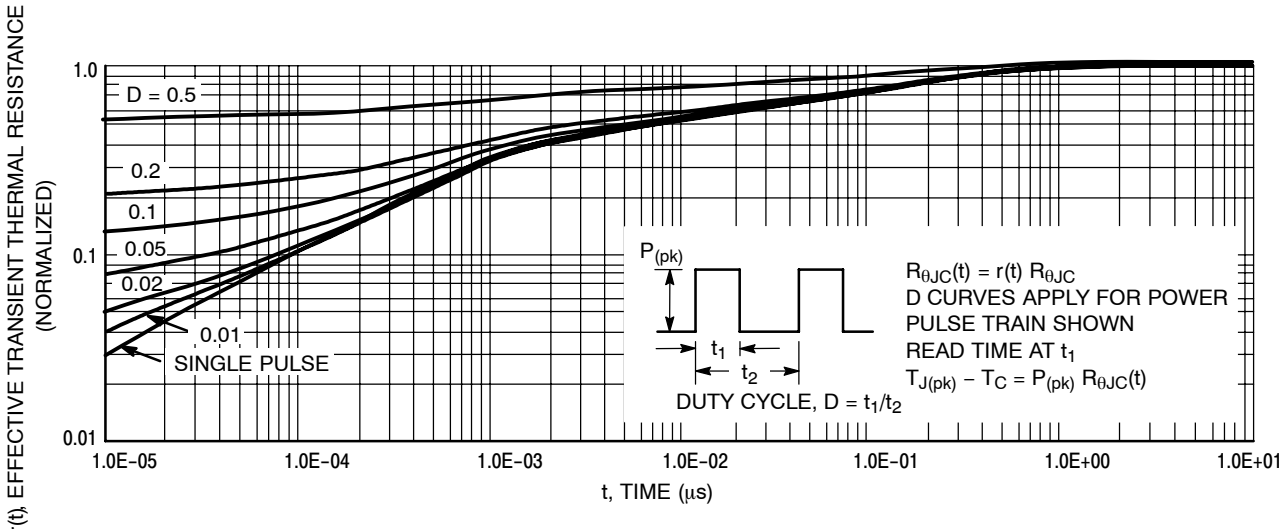


Figure 14. Thermal Response

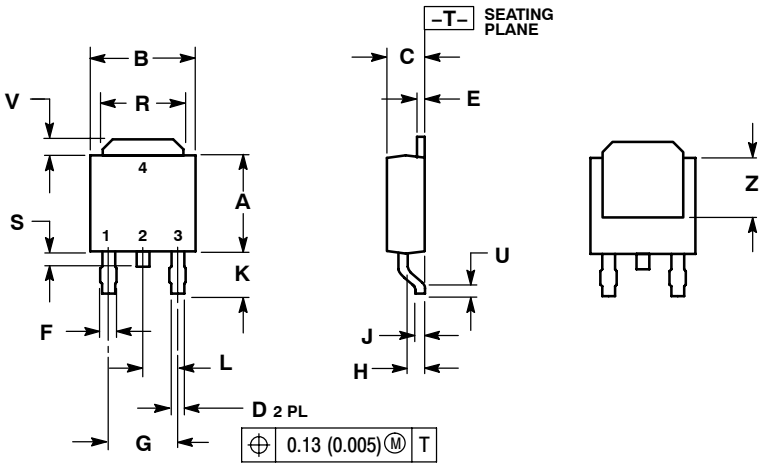
ORDERING INFORMATION

Order Number	Package	Shipping†
NTD4804NAT4G	DPAK (Pb−Free)	2500 Tape & Reel
NTD4804NA−1G	IPAK (Pb−Free)	75 Units/Rail
NTD4804NA−35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb−Free)	75 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

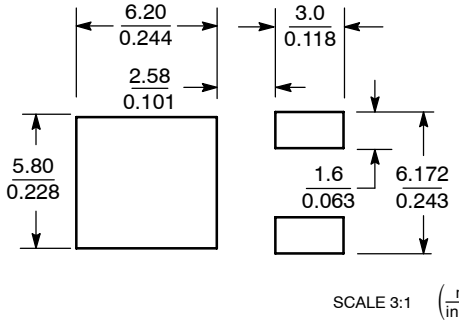
DPAK
CASE 369C−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

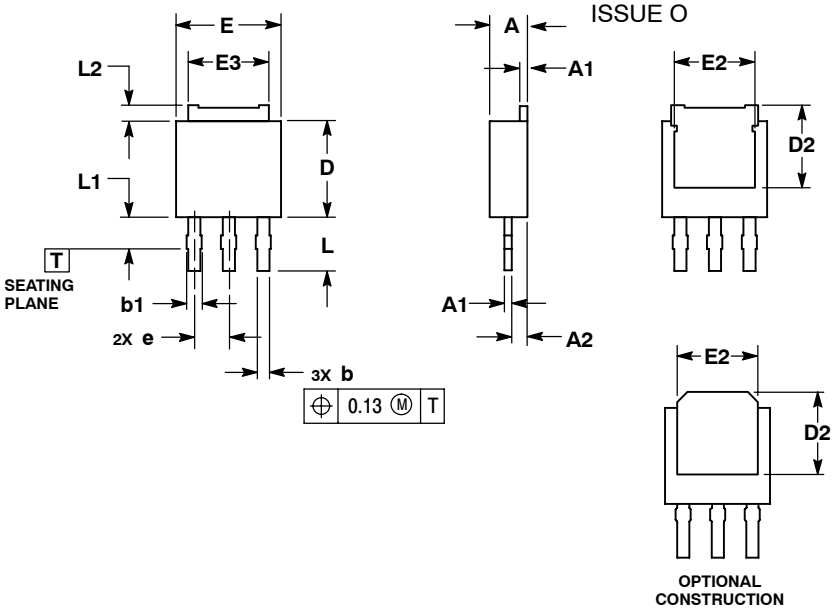
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

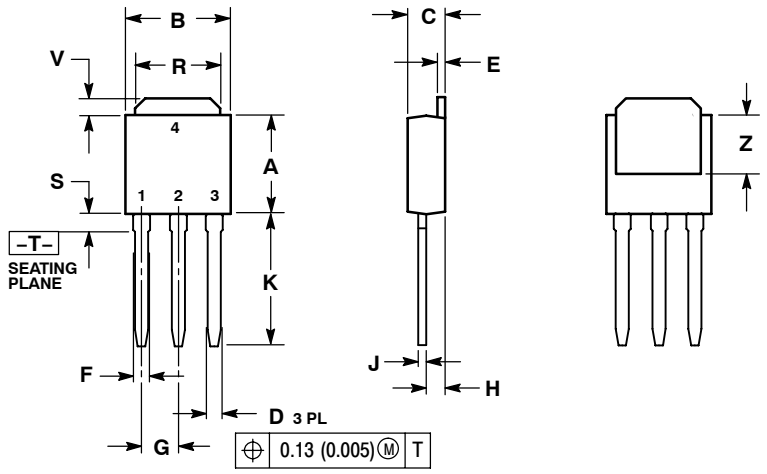
3.5 MM IPAK, STRAIGHT LEAD
CASE 369AD−01
ISSUE O



NOTES:
1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

	MILLIMETERS	
DIM	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	−−−
E	6.35	6.73
E2	4.70	−−−
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	−−−	2.10
L2	0.89	1.27

DPAK
CASE 369D−01
ISSUE B



NOTES:
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E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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