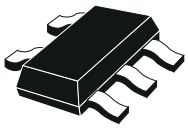
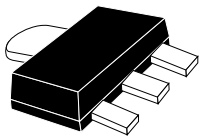
LD2981

Ultra low-drop voltage regulators with inhibit

Datasheet - production data



SOT23-5L



SOT-89

Features

- Ultra low dropout voltage (0.17 V typ. at 100 mA load, 7 mV typ. at 1 mA load)
- Very low quiescent current (80 µA typ. at no load in on mode; max 1 µA in off mode)
- Guaranteed output current up to 100 mA
- Logic-controlled electronic shutdown
- Output voltage of 2.5; 3.0; 3.3; 5.0 V
- Internal current and thermal limit
- ± 0.75% tolerance output voltage available (A version)
- Output low noise voltage 160 µVRMS
- Temperature range: -40 to 125 °C
- Small package SOT23-5L and SOT-89
- Fast dynamic response to line and load changes

Description

The LD2981 is a 100 mA fixed-output voltage regulator. The low-drop voltage and the ultra low quiescent current make them suitable for low noise, low power applications and in battery powered systems.

The quiescent current in sleep mode is less than 1 µA when INHIBIT pin is pulled low. Shutdown logic control function is available on pin n° 3 (TTL compatible). This means that when the device is used as local regulator, it is possible to put a part of the board in standby, decreasing the total power consumption. The LD2981 is designed to work with low ESR ceramic capacitor. Typical applications are in cellular phone, palmtop/laptop computer, personal digital assistant (PDA), personal stereo, camcorder and camera.

This is information on a product in full production.

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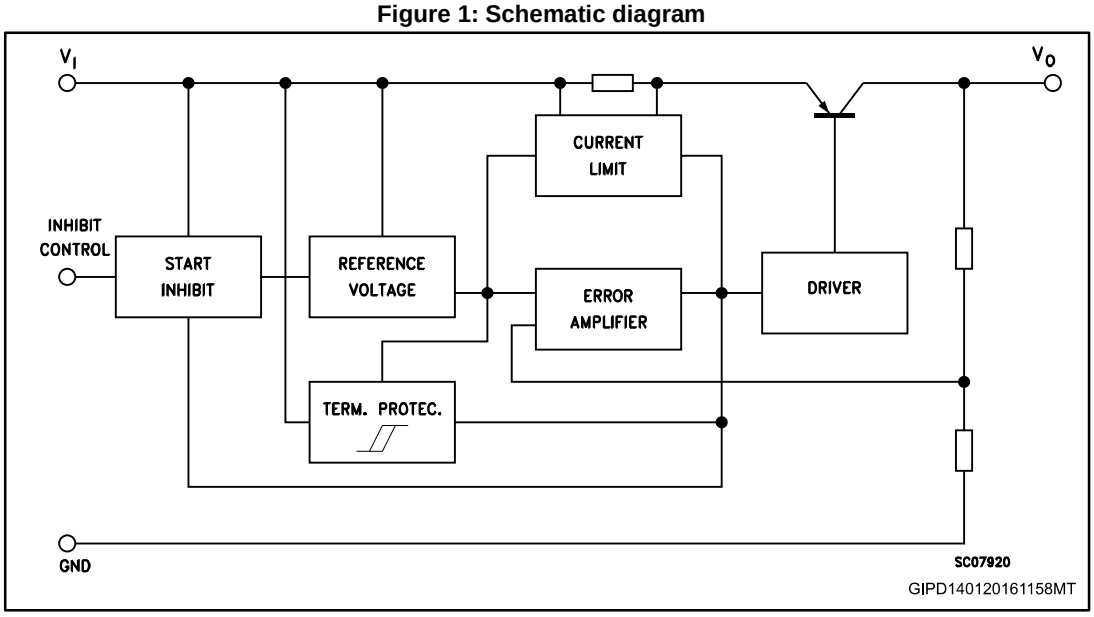
Figure 1: Schematic diagram



2 Pin configuration

Figure 2: Pin connections (top view)

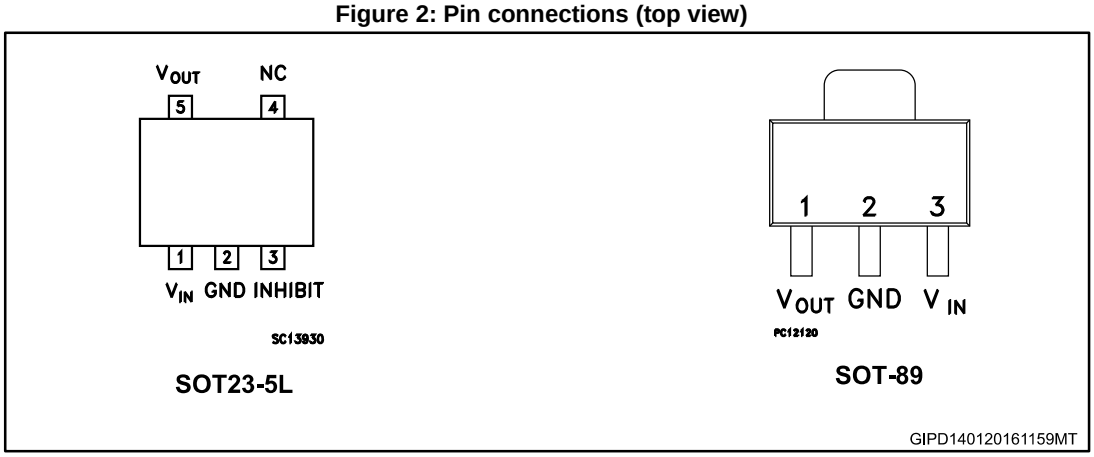


Table 1: Pin description

Pin n° SOT23-5L	Pin n° SOT-89	Symbol	Name and function
1	3	V_{IN}	Input port
2	2	GND	Ground pin
3		INHIBIT	Control switch ON/OFF. Inhibit is not internally pulled-up; it cannot be left floating. Disable the device when connected to GND or to a positive voltage less than 0.18 V
4		NC	Not connected
5	1	V_{OUT}	Output port

Table 2: Thermal data

Symbol	Parameter	SOT23-5L	SOT-89	Unit
R_{thJC}	Thermal resistance junction-case	81	15	°C/W
R_{thJA}	Thermal resistance junction-ambient	255	110	°C/W

3 Maximum ratings

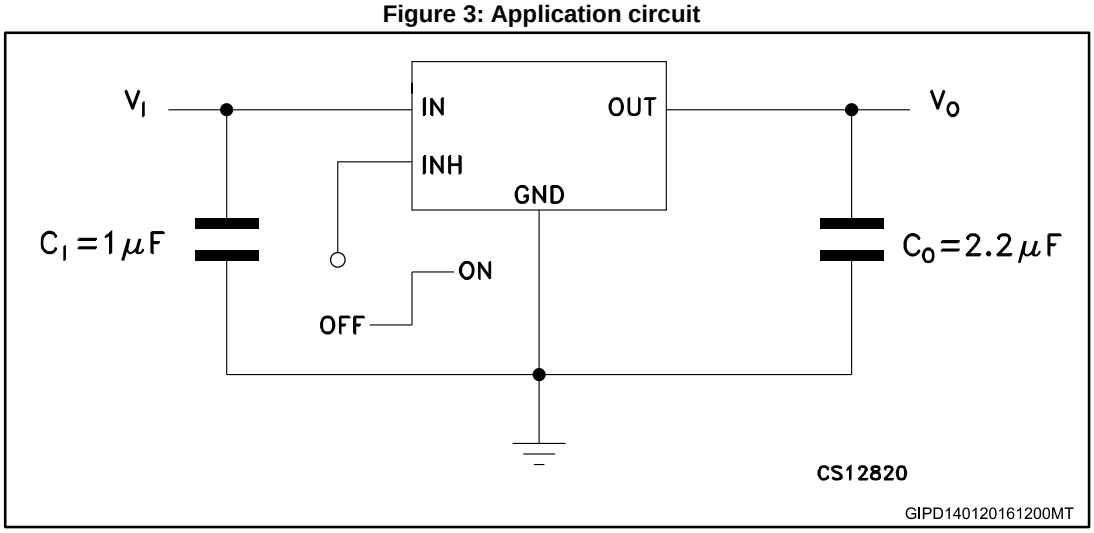
Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	DC input voltage	-0.3 to 16	V
V_{INH}	INHIBIT input voltage	-0.3 to 16	V
I_O	Output current	Internally limited	
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-55 to 150	°C
T_{OP}	Operating junction temperature range	-40 to 125	°C

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

4 Typical application

Figure 3: Application circuit



Inhibit pin is not internally pulled-up then it must not be left floating. Disable the device when connected to GND or to a positive voltage less than 0.18 V.

5 Electrical characteristics

(T_J = 25 °C, V_I = $V_{O(NOM)}$ + 1 V, C_I = 1 µF, C_O = 2.2 µF, I_O = 1 mA, V_{INH} = 2 V, unless otherwise specified).

Table 4: Electrical characteristics for LD2981AB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OP}	Operating input voltage		2.5		16	V
V_O	Output voltage	I_O = 1 mA	2.977	3	3.023	V
		I_O = 1 to 100 mA	2.97		3.03	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	2.925		3.075	
V_O	Output voltage	I_O = 1 mA	3.275	3.3	3.325	V
		I_O = 1 to 100 mA	3.267		3.333	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	3.217		3.383	
V_O	Output voltage	I_O = 1 mA	4.962	5	5.038	V
		I_O = 1 to 100 mA	4.95		5.05	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	4.875		5.125	
ΔV_O	Line regulation	$V_{O(NOM)}$ + 1 < V_{IN} < 16 V, I_O = 1 mA		0.003	0.014	%/V
		T_J = -40 to 125 °C			0.032	
I_Q	Quiescent current ON MODE	I_O = 0		80	100	µA
		I_O = 0, T_J = -40 to 125 °C			150	
		I_O = 1 mA		100	150	
		I_O = 1 mA, T_J = -40 to 125 °C			200	
		I_O = 25 mA		250	400	
		I_O = 25 mA, T_J = -40 to 125 °C			800	
		I_O = 100 mA		1000	1300	
		I_O = 100 mA, T_J = -40 to 125 °C			2600	
	OFF MODE	V_{INH} < 0.3 V			0.8	
		V_{INH} < 0.15 V, T_J = -40 to 125 °C			2	
V_{DROP}	Dropout voltage (1)	I_O = 0		1	3	mV
		I_O = 0, T_J = -40 to 125 °C			5	
		I_O = 1 mA		7	10	
		I_O = 1 mA, T_J = -40 to 125 °C			15	
		I_O = 25 mA		70	100	
		I_O = 25 mA, T_J = -40 to 125 °C			150	
		I_O = 100 mA		180	250	
		I_O = 100 mA, T_J = -40 to 125 °C			375	
I_{SC}	Short circuit current	R_L = 0		150		mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SVR	Supply voltage rejection	C_O = 10 µF, f = 1 KHz		63		dB
V_{INH}	Inhibit input logic low	LOW = Output OFF, T_J = -40 to 125 °C			0.18	V
V_{INL}	Inhibit input logic high	HIGH = Output ON, T_J = -40 to 125 °C	1.6			V
I_{INH}	Inhibit input current	V_{INH} = 0 V, T_J = -40 to 125 °C		0	-1	µA
		V_{INH} = 5 V, T_J = -40 to 125 °C		5	15	
e_N	Output noise voltage	B_W = 300 Hz to 50 KHz, C_O = 10 µF		160		μV_{RMS}
T_{SHDN}	Thermal shutdown			170		°C

Notes:

(1) For V_O < 2.5 V dropout voltage can be calculated according to the minimum input voltage in full temperature range.

(T_J = 25 °C, V_I = $V_{O(NOM)}$ +1 V, C_I = 1 µF, C_O = 2.2 µF, I_O = 1 mA, V_{INH} = 2 V, unless otherwise specified)

Table 5: Electrical characteristics for LD2981C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OP}	Operating input voltage		2.5		16	V
V_O	Output voltage	I_O = 1 mA	2.468	2.5	2.531	V
		I_O = 1 to 100 mA	2.45		2.55	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	2.412		2.587	
V_O	Output voltage	I_O = 1 mA	2.962	3	3.037	V
		I_O = 1 to 100 mA	2.94		3.06	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	2.895		3.105	
V_O	Output voltage	I_O = 1 mA	3.258	3.3	3.341	V
		I_O = 1 to 100 mA	3.234		3.366	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	3.184		3.415	
V_O	Output voltage	I_O = 1 mA	4.937	5	5.062	V
		I_O = 1 to 100 mA	4.9		5.1	
		I_O = 1 to 100 mA, T_J = -40 to 125 °C	4.825		5.175	
ΔV_O	Line regulation	$V_{O(NOM)}$ + 1 < V_{IN} < 16 V, I_O = 1 mA		0.003	0.014	%/V
		T_J = -40 to 125 °C			0.032	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent current ON MODE	I_O = 0		80	100	µA
		I_O = 0, T_J = -40 to 125 °C			150	
		I_O = 1 mA		100	150	
		I_O = 1 mA, T_J = -40 to 125 °C			200	
		I_O = 25 mA		250	400	
		I_O = 25 mA, T_J = -40 to 125 °C			800	
		I_O = 100 mA		1000	1300	
		I_O = 100 mA, T_J = -40 to 125 °C			2600	
	OFF MODE	V_{INH} < 0.3 V			0.8	
		V_{INH} < 0.15 V, T_J = -40 to 125 °C			2	
V_{DROP}	Dropout voltage (1)	I_O = 0		1	3	mV
		I_O = 0, T_J = -40 to 125 °C			5	
		I_O = 1 mA		7	10	
		I_O = 1 mA, T_J = -40 to 125 °C			15	
		I_O = 25 mA		70	100	
		I_O = 25 mA, T_J = -40 to 125 °C			150	
		I_O = 100 mA		180	250	
		I_O = 100 mA, T_J = -40 to 125 °C			375	
I_{SC}	Short circuit current	R_L = 0		150		mA
SVR	Supply voltage rejection	C_O = 10 µF, f = 1 KHz		63		dB
V_{INH}	Inhibit input logic low	LOW = Output OFF, T_J = -40 to 125 °C			0.18	V
V_{INL}	Inhibit input logic high	HIGH = Output ON, T_J = -40 to 125 °C	1.6			V
I_{INH}	Inhibit input current	V_{INH} = 0 V, T_J = -40 to 125 °C		0	-1	µF
		V_{INH} = 5 V, T_J = -40 to 125 °C		5	15	
e_N	Output noise voltage	B_W = 300 Hz to 50 KHz, C_O = 10 µF		160		μV_{RMS}
T_{SHDN}	Thermal shutdown			170		°C

Notes:

(1) For V_O < 2.5 V dropout voltage can be calculated according to the minimum input voltage in full temperature range.

6 Typical performance characteristics

(T_J = 25 °C, V_I = $V_{O(NOM)}$ +1 V, C_I = 1 µF, C_O = 2.2 µF, V_{INH} = 2 V, unless otherwise specified).

Figure 4: Output voltage vs temperature

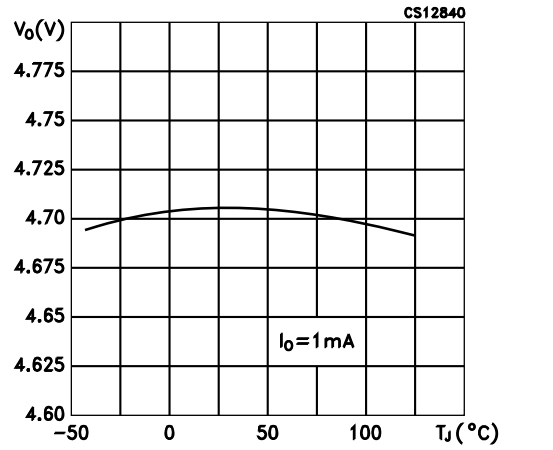


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Figure 5: Dropout voltage vs temperature

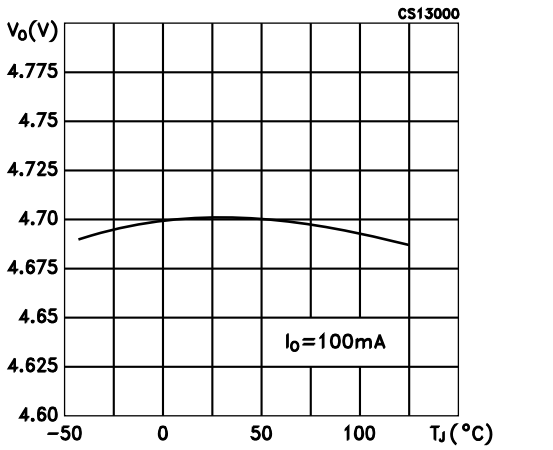

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Figure 6: Line regulation vs temperature

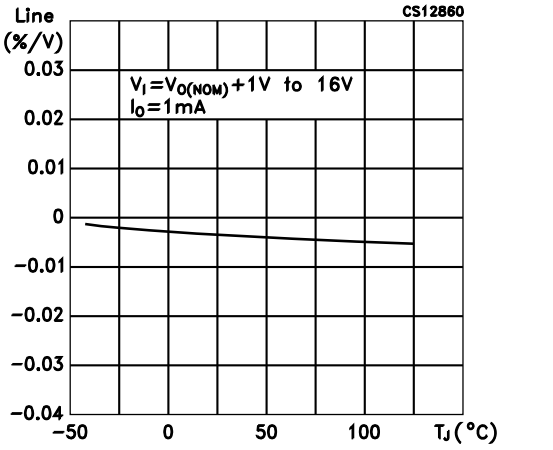

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Figure 7: Load regulation vs temperature

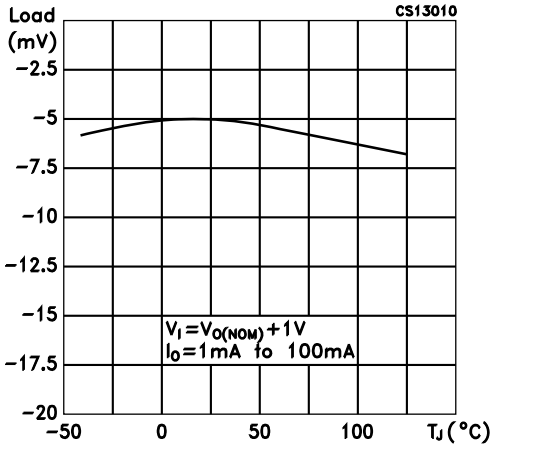

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Figure 8: Dropout voltage vs temperature

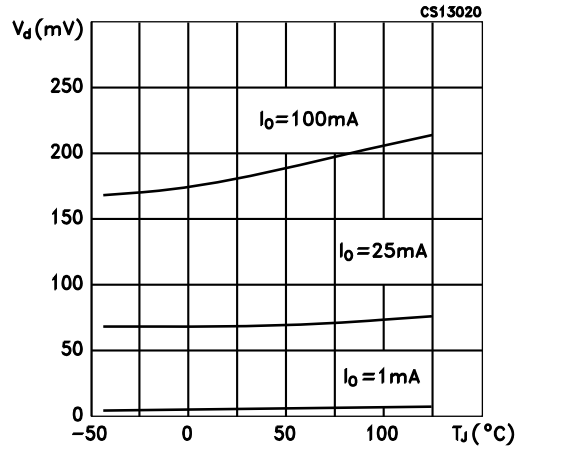

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Figure 9: Quiescent current vs temperature

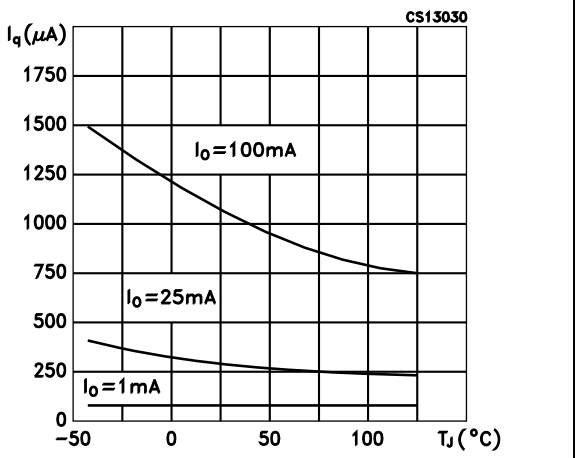

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Figure 10: Quiescent current vs output current

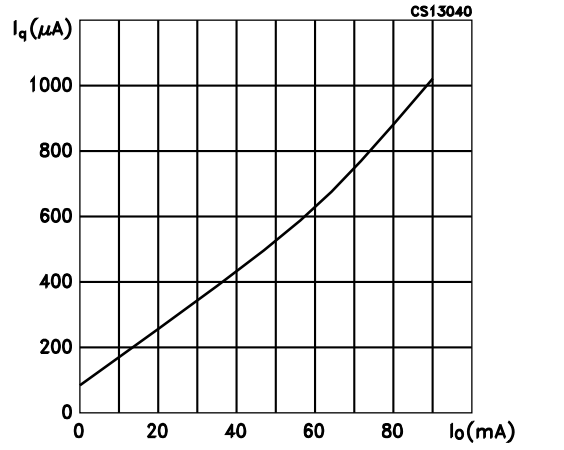

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Figure 11: Off mode quiescent current vs temperature

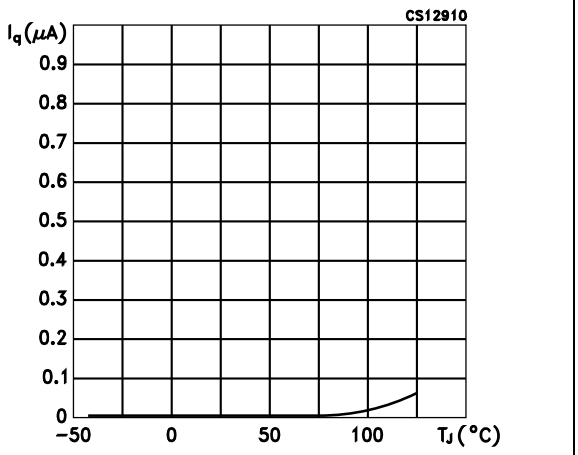

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Figure 12: Quiescent current vs input voltage

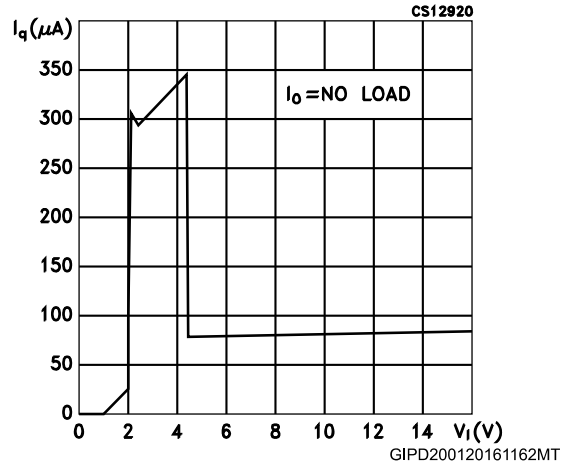

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Figure 13: Dropout voltage vs output current

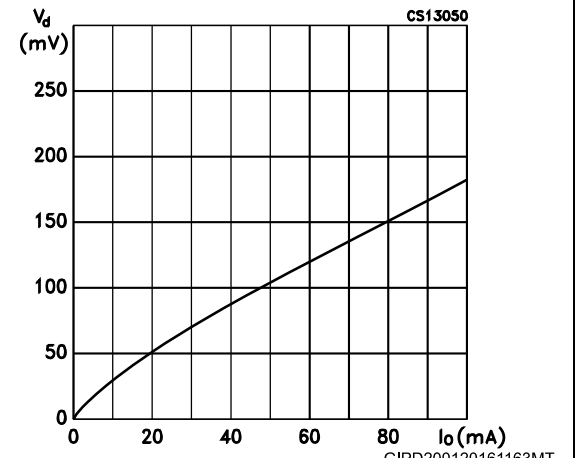

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Figure 14: Inhibit input current vs temperature

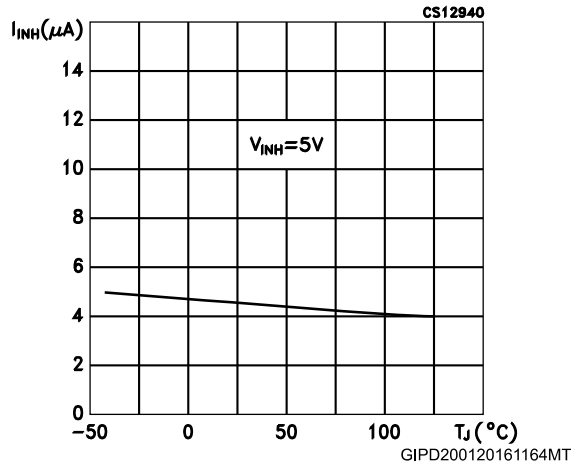

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Figure 15: Inhibit voltage vs temperature

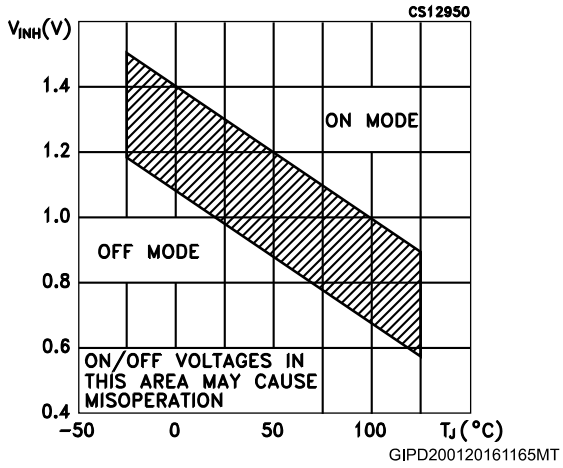

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Figure 16: Supply voltage rejection vs frequency

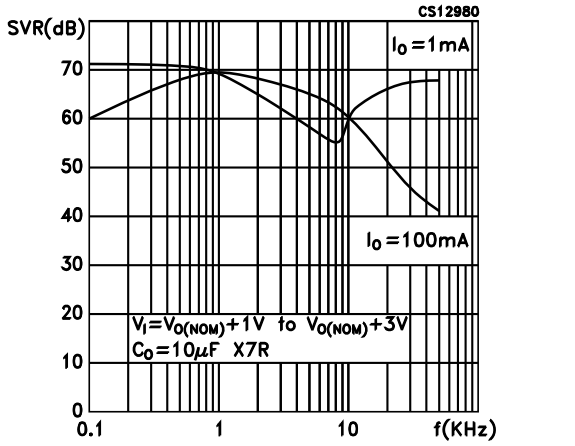

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Figure 17: Noise voltage vs frequency

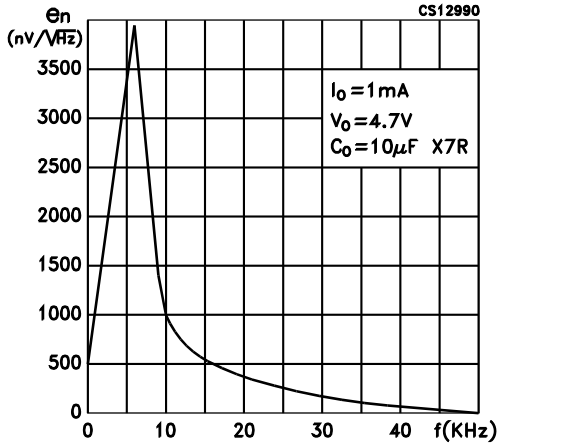

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Figure 18: Best case: highest output version

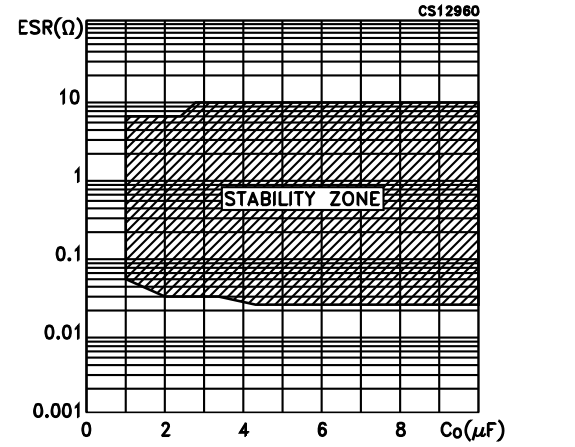

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Figure 19: Worst case: lowest output version

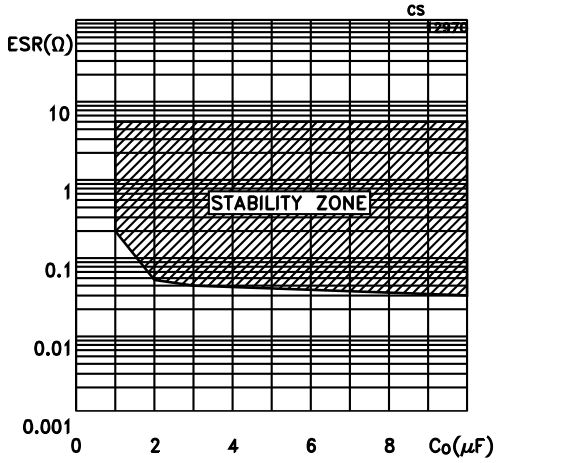

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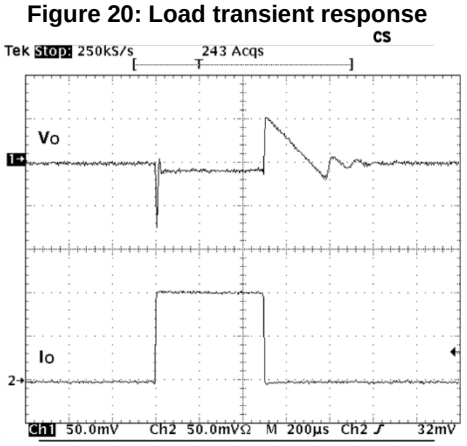
Figure 20: Load transient response



V_O = 4.7V, I_O = 1 to 100mA, C_O = 4.7µF (X7R)

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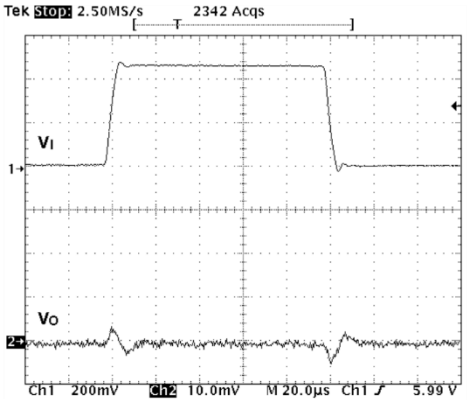
Figure 21: Line transient response



V_I = [$V_{O(NOM)}$ +1V], V_O = 4.7V, I_O = 100mA, C_O = 4.7µF (X7R)

GIPD200120161171MT

7 Application notes

7.1 External capacitors

Like any low-dropout regulator, the LD2981 requires external capacitors for regulator stability. This capacitor must be selected to meet the requirements of minimum capacitance and equivalent series resistance. We suggest to solder input and output capacitors as close as possible to the relative pins.

7.2 Input capacitor

An input capacitor whose value is 1 µF is required with the LD2981 (amount of capacitance can be increased without limit). This capacitor must be located a distance of not more than 0.5" from the input pin of the device and returned to a clean analog ground. Any good quality ceramic, tantalum or film capacitors can be used for this capacitor.

7.3 Output capacitor

The LD2981 is designed specifically to work with ceramic output capacitors. It may also be possible to use Tantalum capacitors, but these are not as attractive for reasons of size and cost. By the way, the output capacitor must meet both the requirement for minimum amount of capacitance and ESR (equivalent series resistance) value. The *Figure 18: "Best case: highest output version"* and *Figure 19: "Worst case: lowest output version"* show the allowable ESR range as a function of the output capacitance. These curves represent the stability region over the full temperature and IO range. Due to the different loop gain, the stability improves for higher output versions and so the suggested minimum output capacitor value, if low ESR ceramic type is used, is 1 µF for output voltages equal or major than 3.8 V, 2.2 µF for output voltages from 2.85 to 3.3 V, and 3.3 µF for the other versions. However, if an output capacitor lower than the suggested one is used, it's possible to make stable the regulator adding a resistor in series to the capacitor (see *Figure 18: "Best case: highest output version"* and *Figure 19: "Worst case: lowest output version"* to choose the right value according to the used version and keeping in account that the ESR of ceramic capacitors has been measured @ 100 kHz).

7.4 Important

The output capacitor must maintain its ESR in the stable region over the full operating temperature to assure stability. Also, capacitor tolerance and variation with temperature must be considered to assure the minimum amount of capacitance is provided at all times. This capacitor should be located not more than 0.5" from the output pin of the device and returned to a clean analog ground.

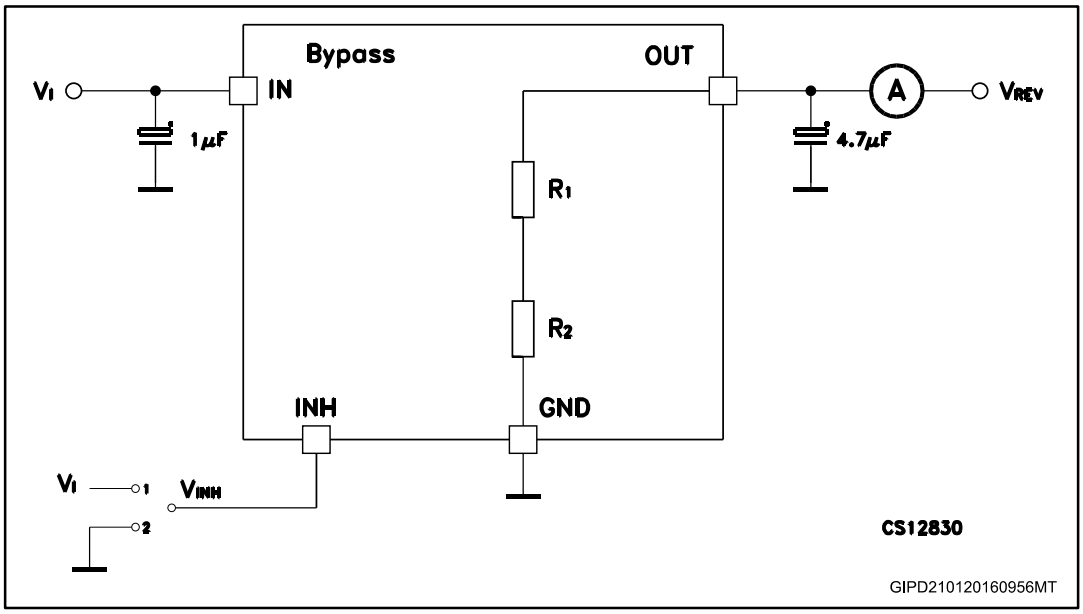
7.5 Inhibit input operation

The inhibit pin can be used to turn OFF the regulator when pulled low, so drastically reducing the current consumption down to less than 1 µA. When the inhibit feature is not used, this pin must be tied to VI to keep the regulator output ON at all times. To assure proper operation, the signal source used to drive the inhibit pin must be able to swing above and below the specified thresholds listed in the electrical characteristics section under V_{IH} V_{IL}. Any slew rate can be used to drive the inhibit.

7.6 Reverse current

The power transistor used in the LD2981 has not an inherent diode connected between the regulator input and output. If the output is forced above the input, no current will flow from the output to the input across the series pass transistor. When a V_{REV} voltage is applied on the output, the reverse current measured, according to the test circuit in *Figure 22: "Reverse current test circuit"*, flows to the GND across the two feedback resistors. This current typical value is 160 µA. R_1 and R_2 resistors are implanted type; typical values are, respectively, 42.6 kΩ and 51.150 kΩ.

Figure 22: Reverse current test circuit



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 SOT-89 package information

Figure 23: SOT-89 package outline

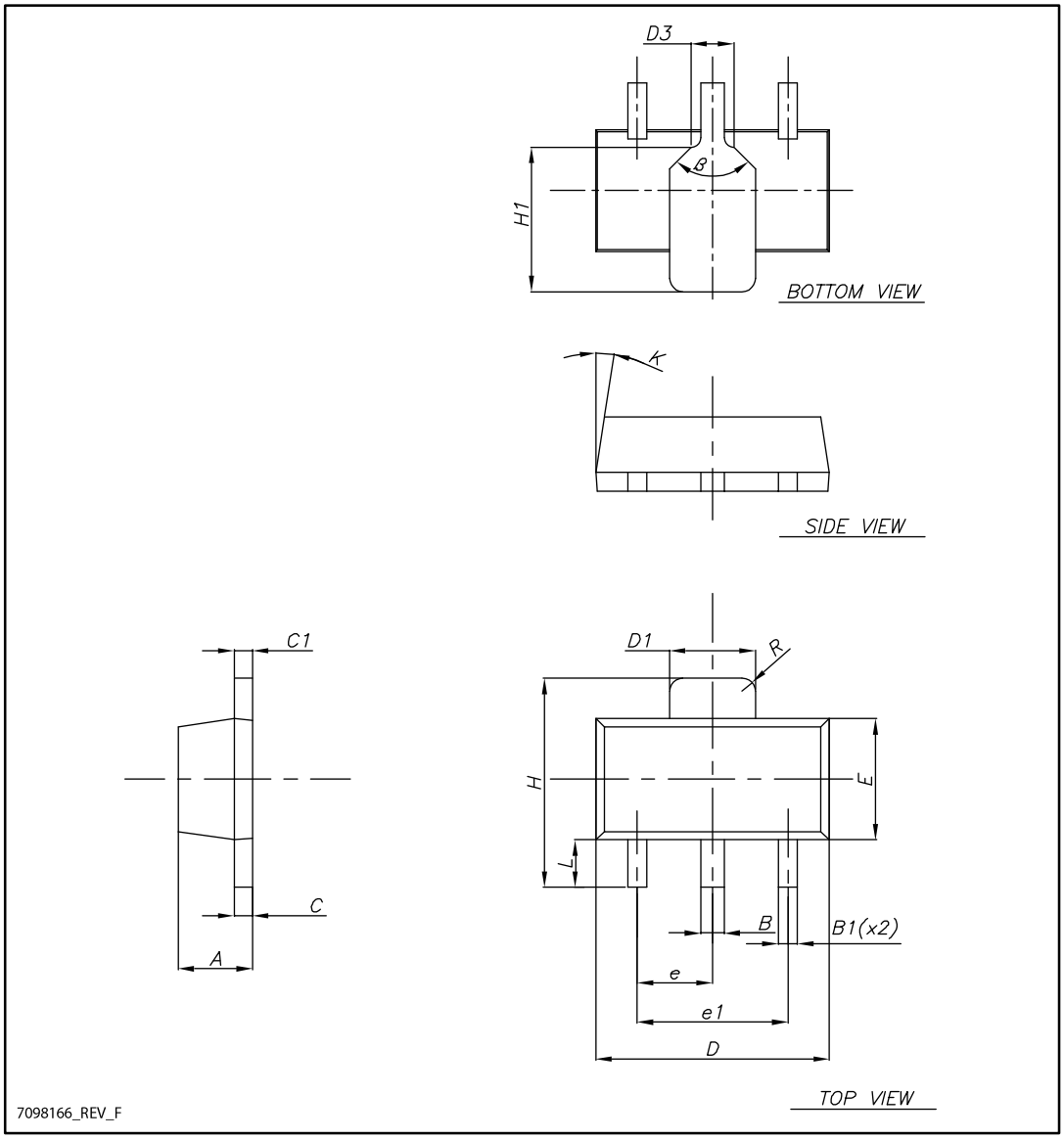
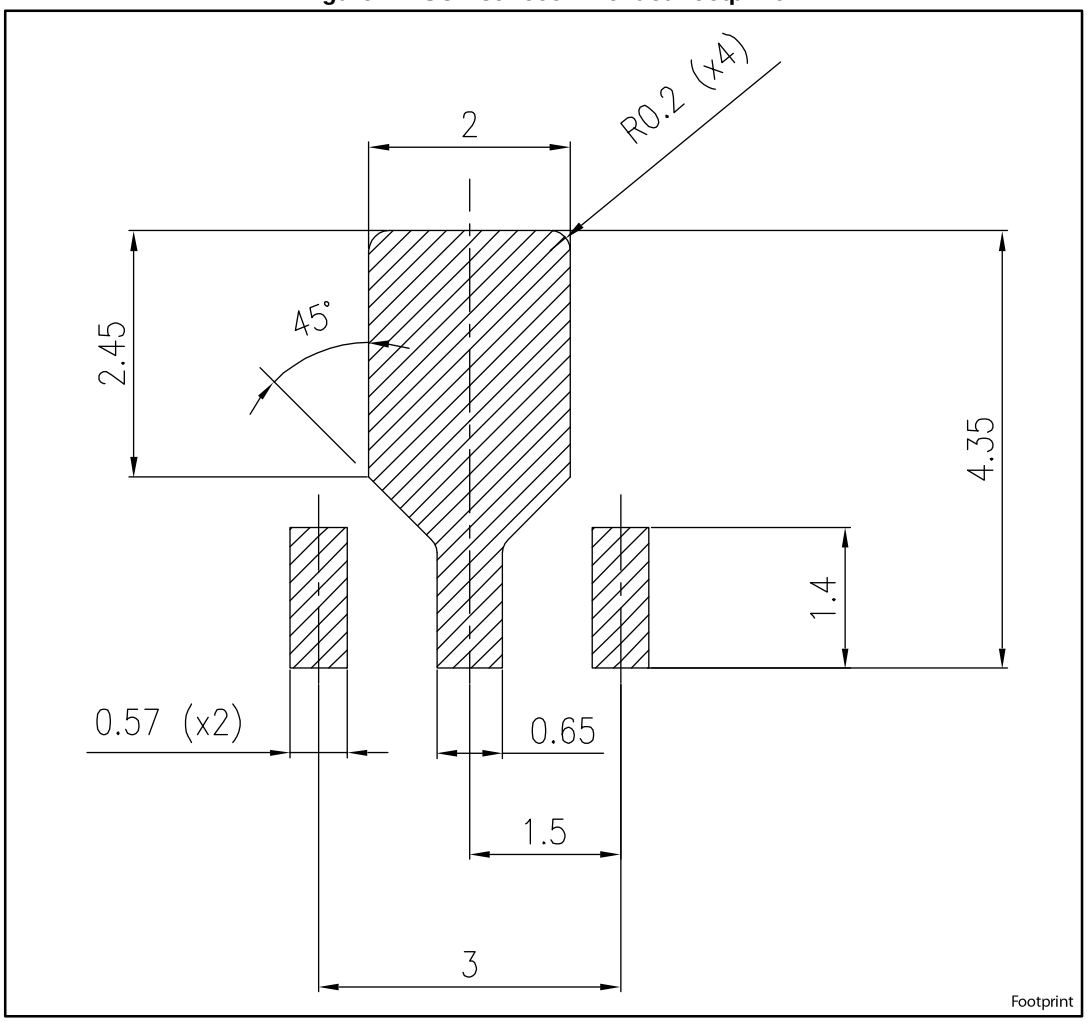


Table 6: SOT-89 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.40		1.60
B	0.44		0.56
B1	0.36		0.48
C	0.35		0.44
C1	0.35		0.44
D	4.40		4.60
D1	1.62		1.83
D3		0.90	
E	2.29		2.60
e	1.42		1.57
e1	2.92		3.07
H	3.94		4.25
H1	2.70		3.10
K	1°		8°
L	0.89		120
R		0.25	
β		90°	

Figure 24: SOT-89 recommended footprint



8.2 SOT-89 packing information

Figure 25: SOT-89 carrier tape outline

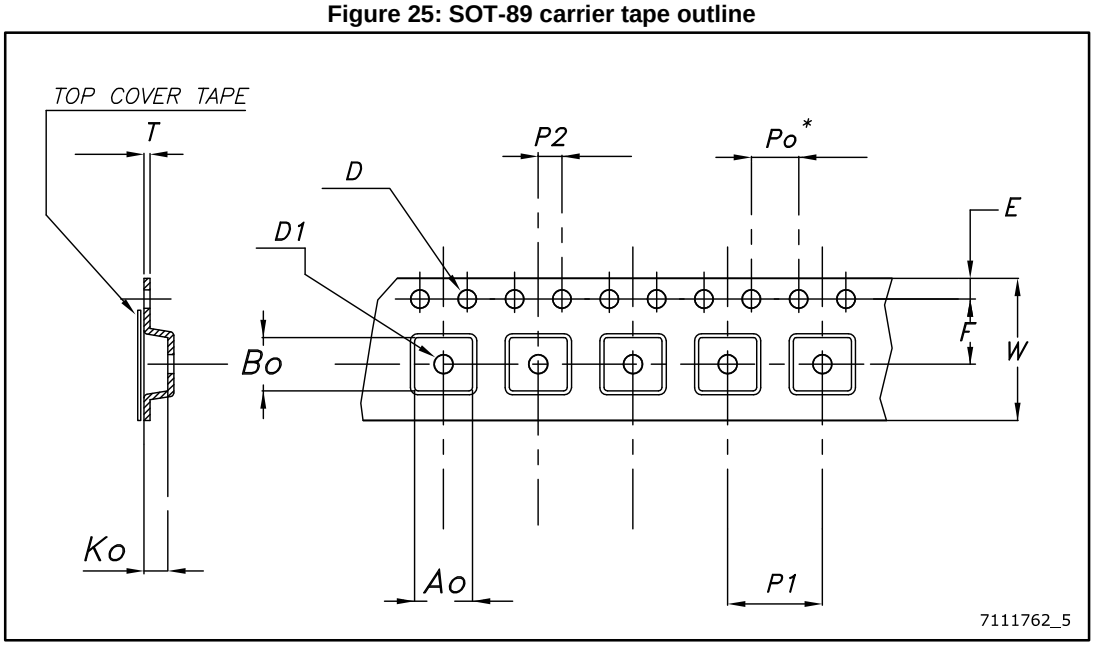


Table 7: SOT-89 carrier tape mechanical data

Dim.	mm	
	Value	Tolerance
Ao	4.91	± 0.10
Bo	4.52	± 0.10
Ko	1.90	± 0.10
F	5.50	± 0.10
E	1.75	± 0.10
W	12	± 0.30
P2	2	± 0.10
Po	4	± 0.10
P1	8	± 0.10
T	0.30	± 0.10
D	Ø 1.55	± 0.05
D1	Ø 1.60	± 0.10

8.3 SOT23-5L package information

Figure 26: SOT23-5L package outline

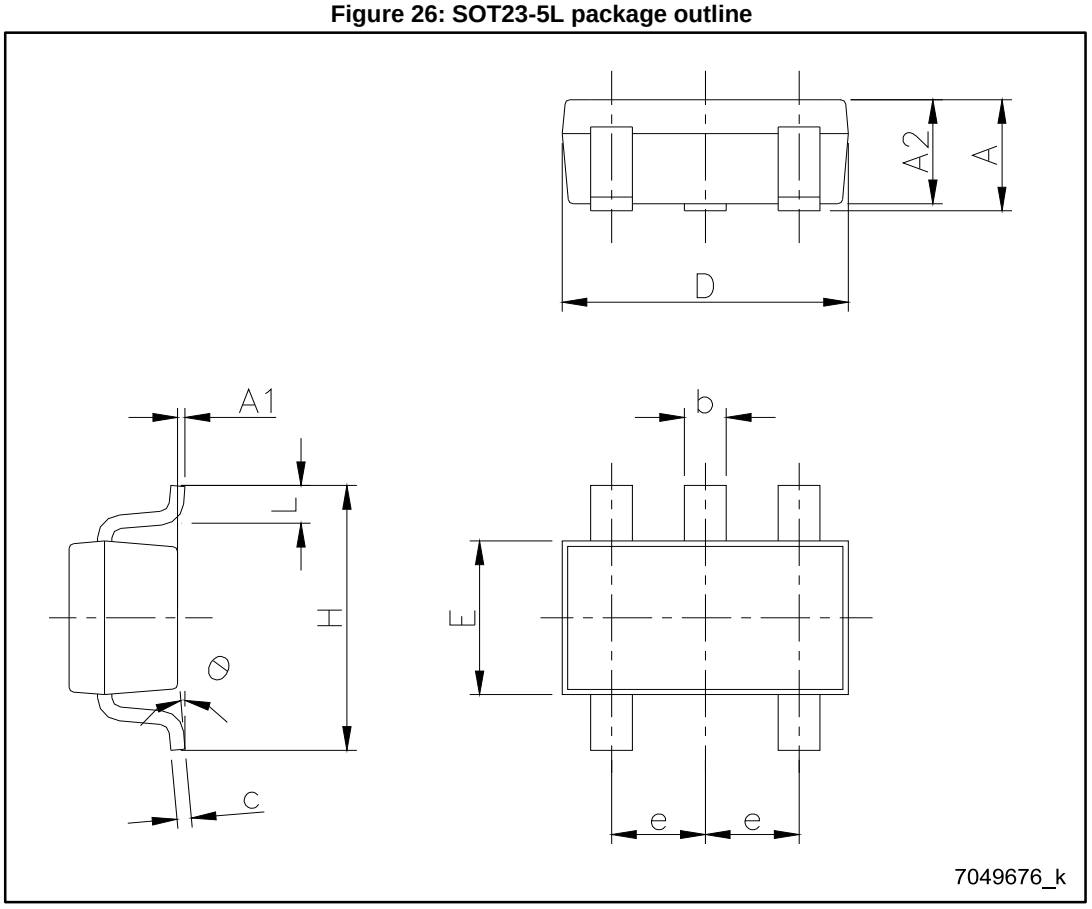
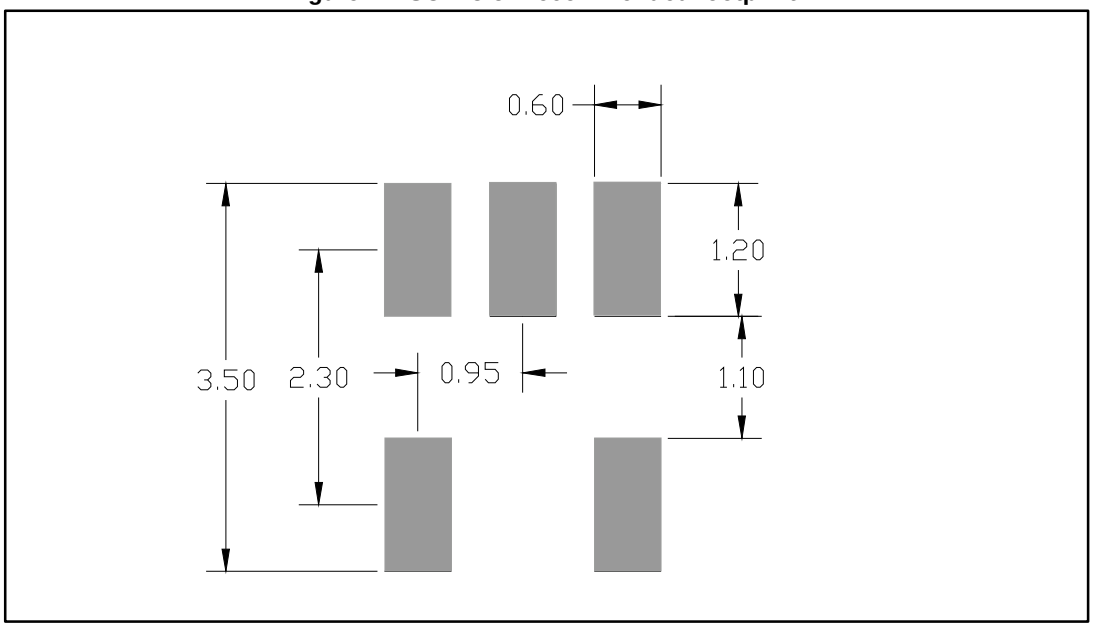


Table 8: SOT23-5L package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.90		1.45
A1	0		0.15
A2	0.90		1.30
b	0.30		0.50
c	0.09		0.20
D		2.95	
E		1.60	
e		0.95	
H		2.80	
L	0.30		0.60
θ	0°		8°

Figure 27: SOT23-5L recommended footprint



Dimensions are in mm

8.4 SOT23-5L packing information

Figure 28: SOT23-5L tape and reel outline

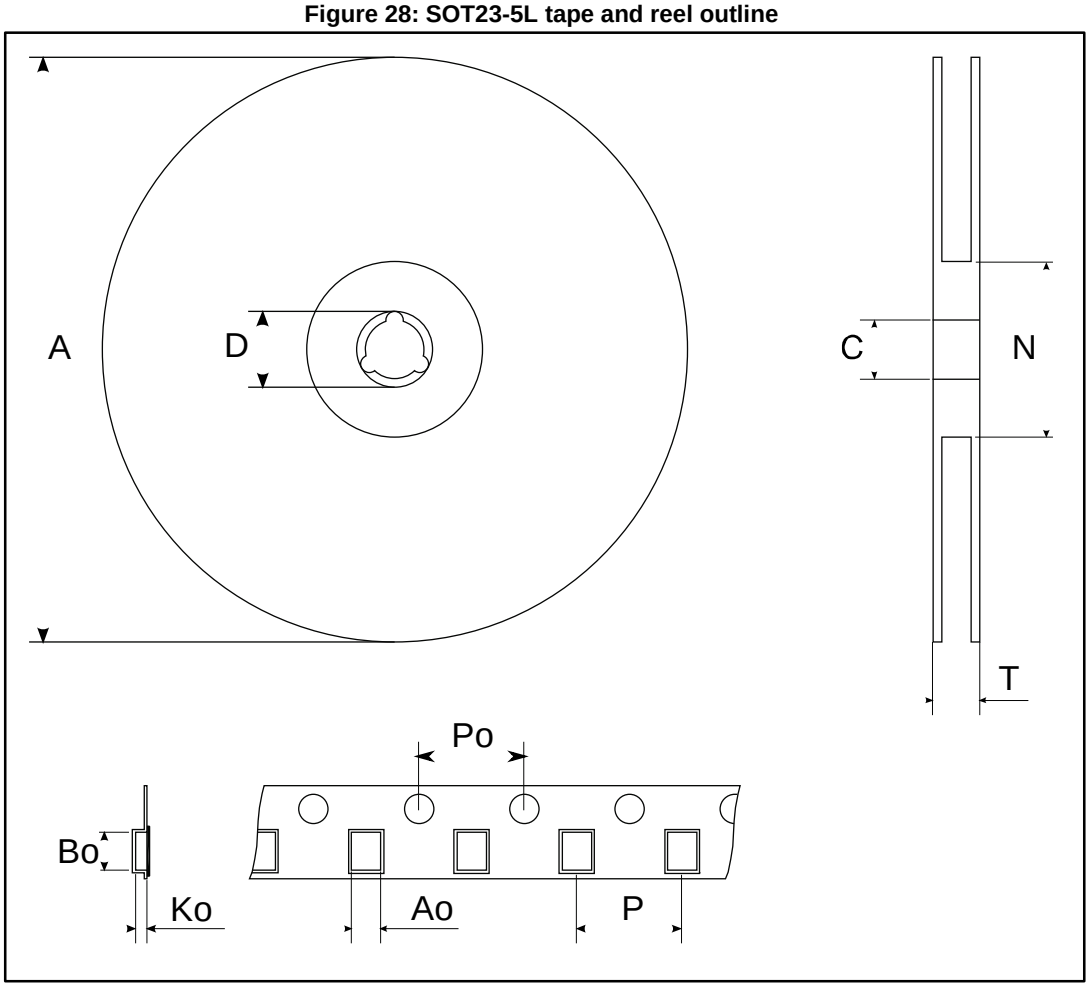


Table 9: SOT23-5L tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C	12.8	13.0	13.2
D	20.2		
N	60		
T			14.4
Ao	3.13	3.23	3.33
Bo	3.07	3.17	3.27
Ko	1.27	1.37	1.47
Po	3.9	4.0	4.1
P	3.9	4.0	4.1

9 Ordering information

Table 10: Order codes

AB version		C version		Output voltage
SOT23-5L	**SOT-89**	**SOT23-5L**	**SOT-89**	
		LD2981CM25TR		2.5 V
LD2981ABM30TR		LD2981CM30TR		3.0 V
LD2981ABM33TR	LD2981ABU33TR	LD2981CM33TR	LD2981CU33TR	3.3 V
LD2981ABM50TR	LD2981ABU50TR	LD2981CM33TR	LD2981CU50TR	5.0 V

10 Revision history

Table 11: Document revision history

Date	Revision	Changes
25-Jul-2006	12	Order codes updated.
14-Feb-2008	13	Added: Table 1 on page 1.
14-Jul-2008	14	Modified: Table 1 on page 1 and Table 10 on page 23.
25-Nov-2013	15	Document name changed from LD2981ABxx and LD2981Cxx to LD2981. Updated Table 4 and Table 5. Updated Section 8: Package information and Section 8.4: SOT-89 packing information. Minor text changes in title, in features and description in cover page.
16-Mar-2015	16	Updated Section 8: Package information. Minor text changes.
01-Apr-2016	17	Updated *Section 8: "Package information"*. Minor text changes.

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