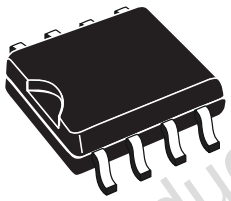
ST2042

Enhanced power switch

Not recommended for new design

Features

- 80 mΩ high-side MOSFET switch
- 500 mA continuous current per channel
- Thermal and short-circuit protection with overcurrent logic output
- Operating range from 2.7 V to 5.5 V
- CMOS- and TTL-compatible enable inputs
- 10 ms OC_N fault-blanking
- 2.5 ms typical rise time
- Undervoltage lock out
- 10 µA maximum standby supply current
- Ambient temperature range, -40 °C to 85 °C
- Fault-blanking



SO-8

Table 1. Device summary

Order code	Package	Packaging
ST2042BD[1]	SO-8	Tube (50 parts per tube, 40 tube per box)
ST2042BDR[1]	SO-8	Tape and reel (2500 parts per reel)

1. Not recommended for new design (refer to STMPS2242MTR). Contact ST sales office for availability.

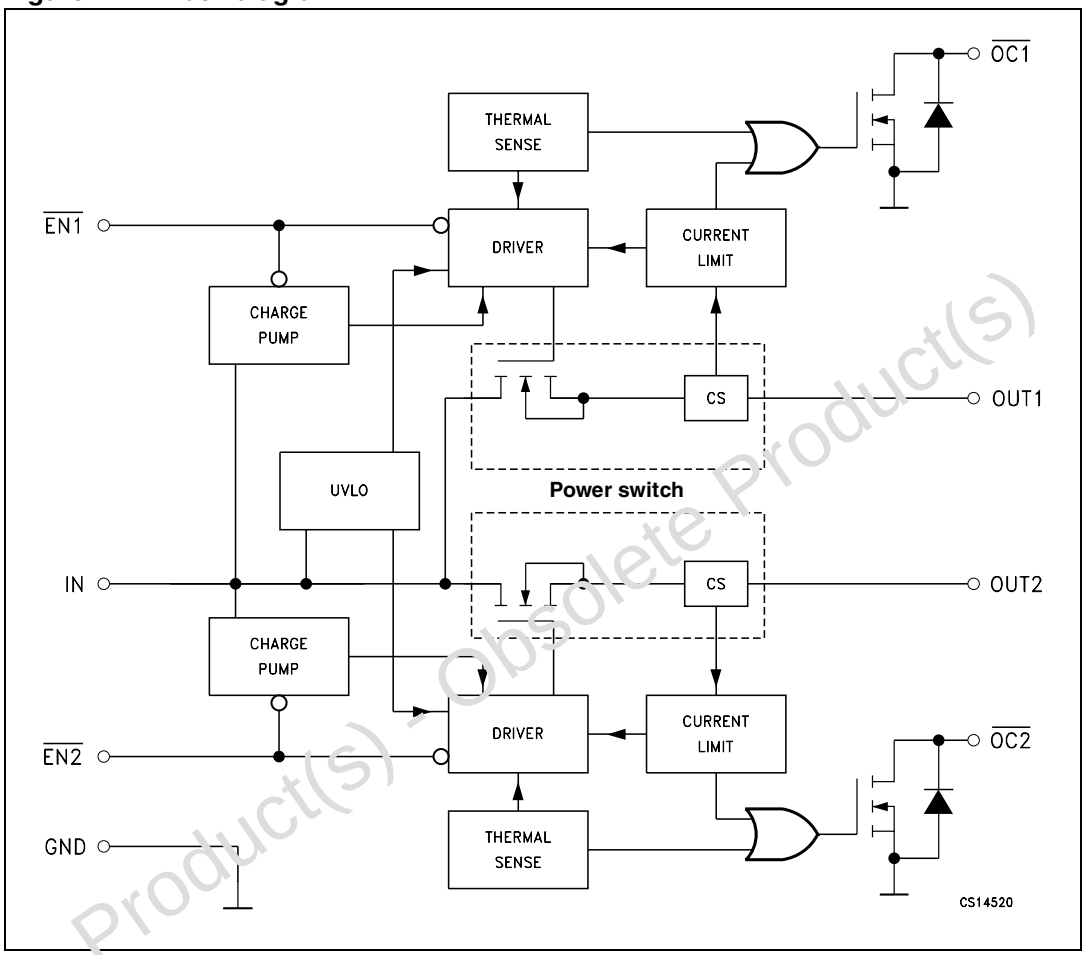
Contents

1 Description

The ST2042 power distribution switches is intended for application where heavy capacitive loads and short-circuits are likely to be encountered. These devices incorporate 80 mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple powers switches in a single package. Each switch is controlled by an independent logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching.
The charge pump requires no external components and allows operation from supplies as low as 2.7 V. When the output load exceeds the current-limit threshold or a short is present, these devices limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OCx) logic output low.
A 10 ms deglitching circuit provides fault-blanking feature, preventing the OC_N pin to be asserted during hot-insertion or short spikes of overcurrent conditions. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present. These power-distribution switches are designed to current limit at 0.9 A.

2 Block diagram

Figure 1. Block diagram



3 Pin connections

Figure 2. Pin connections (top view)

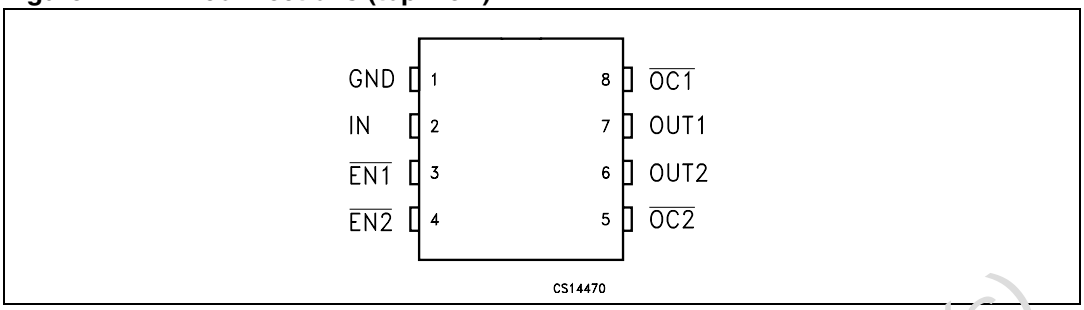


Table 2. Pin functions

Pin	Symbol	Description
1	GND	Ground
2	IN	Input voltage
3	EN1	Enable input. Logic low turns on power switch IN-OUT1.
4	EN2	Enable input. Logic low turns on power switch IN-OUT2.
5	OC2	Overcurrent. Logic output active low IN-OUT2.
6	OUT2	Power switch output
7	OUT1	Power switch output
8	OC1	Overcurrent. Logic output active low IN-OUT2

4 Electrical ratings

4.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_I	Input voltage range(1)	-0.3 - 6	V
V_O	Output voltage range(1)	-0.3 - (V_I + 0.3)	V
V_{IENX}	EN Input voltage range	-0.3 to 6	V
I_O	Continuous output current	Internally limited	
ESD	Electrostatic discharge	2	kV
T_J	Junction operating temperature	-40 to 125	°C

1. All voltages are referred to GND.

4.2 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_I	Input voltage range(1)	2.7		5.5	V
V_O	Output voltage range(1)	0		5.5	V
I_O	Continuous output current (per switch)	0		500	mA

1. All voltages are referred to GND.

5 Electrical characteristics

V_I = 5.5 V, I_O = rated current, $V_{\overline{IEN}}$ = 0 V, T_J = 25 °C, unless otherwise specified (See *Note 1 on page 8*).

Table 5. Power switch electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source ON-state resistance	V_I = 5 V	I_O = 0.5 A		80	100	mΩ
		V_I = 5 V	I_O = 0.5 A, T_J = 85 °C		90	120	
		V_I = 5 V	I_O = 0.5 A, T_J =125 °C		100	135	
		V_I = 3.3 V	I_O = 0.5 A		90	125	
		V_I = 3.3 V	I_O = 0.5 A, T_J = 85 °C		110	145	
		V_I = 3.3 V	I_O = 0.5 A, T_J = 125 °C		120	160	
t_r	Output rise time	V_I = 5.5 V	R_L = 10, C_L = 1 µF		2.5		ms
		V_I = 2.7 V			3		
t_f	Output fall time	V_I = 5.5 V			0.3		ms
		V_I = 2.7 V			0.2		

Table 6. Enable Input $\overline{ENx}$ characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage	V_I = 2.7 to 5.5 V	2			V
V_{IL}	Low level input voltage	V_I = 4.5 to 5.5 V			0.8	V
		V_I = 2.7 to 4.5 V			0.4	
I_I	Input current	V_{IENX} = 0 V or V_I	-0.5		0.5	µA
t_{on}	Turn-on time	R_L= 10 Ω, C_L= 100 µF			20	ms
t_{off}	Turn-off time	R_L= 10 Ω, C_L= 100 µF			40	ms

Table 7. Current limit characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OS}	Short-circuit output current	V_I = 5 V, OUT connected to GND, device enabled into short circuit	0.7	1	1.3	A

Table 8. Supply current characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SOL}	Current low level output	$V_{IENX} = V_I$, no load,		0.025	1	µA
		$V_{IENX} = V_I$, no load, T_J = -40 to 125 °C			10	
I_{SOH}	Current low high output	V_{IENX} = 0, no load,		70	90	µA
		V_{IENX} = 0, no load, T_J = -40 to 125 °C			100	
I_L	Output leakage current	$V_{IENX} = V_I$, output connected to GND, T_J = -40 to 125 °C			10	µA

Table 9. Undervoltage characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage		2		2.5	V
V_{HYS}	Hysteresis			500		mV

Table 10. Overcurrent (OC) characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SINK}	Sink current	V_O = 5 V	10			mA
V_O	Output low voltage	I_O = 5 mA			0.5	V
I_{OFF}	OFF-state current	V_O = 5 V, V_O = 3.3 V			1	µA
T_{FB}	Fault-blanking period	V_I = 5.5 V, T_J = 25 °C (See *Note 2* and *Note 3*)	2	10		ms

Note: 1 Pulse testing techniques maintain junction temperature close to ambient temperature: thermal effect must be takes into account separately.

2 Specified by design, not production tested.

3 Guaranteed by design.

Figure 3. Test circuit

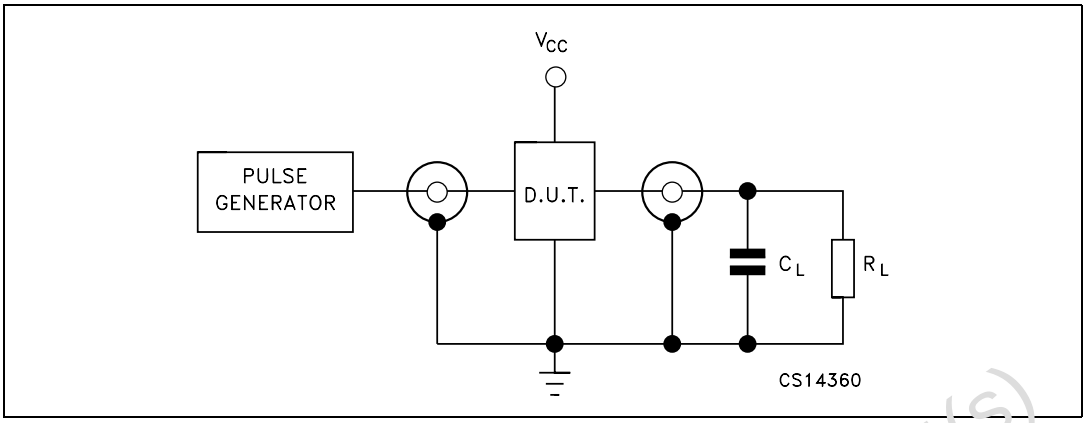
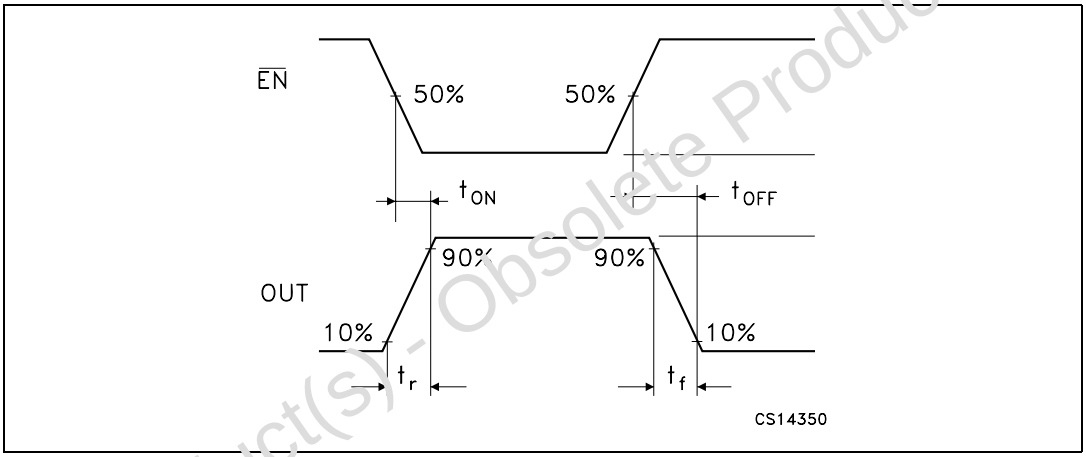


Figure 4. Waveform - propagation delays (f = 1 MHz; 50% duty cycle)



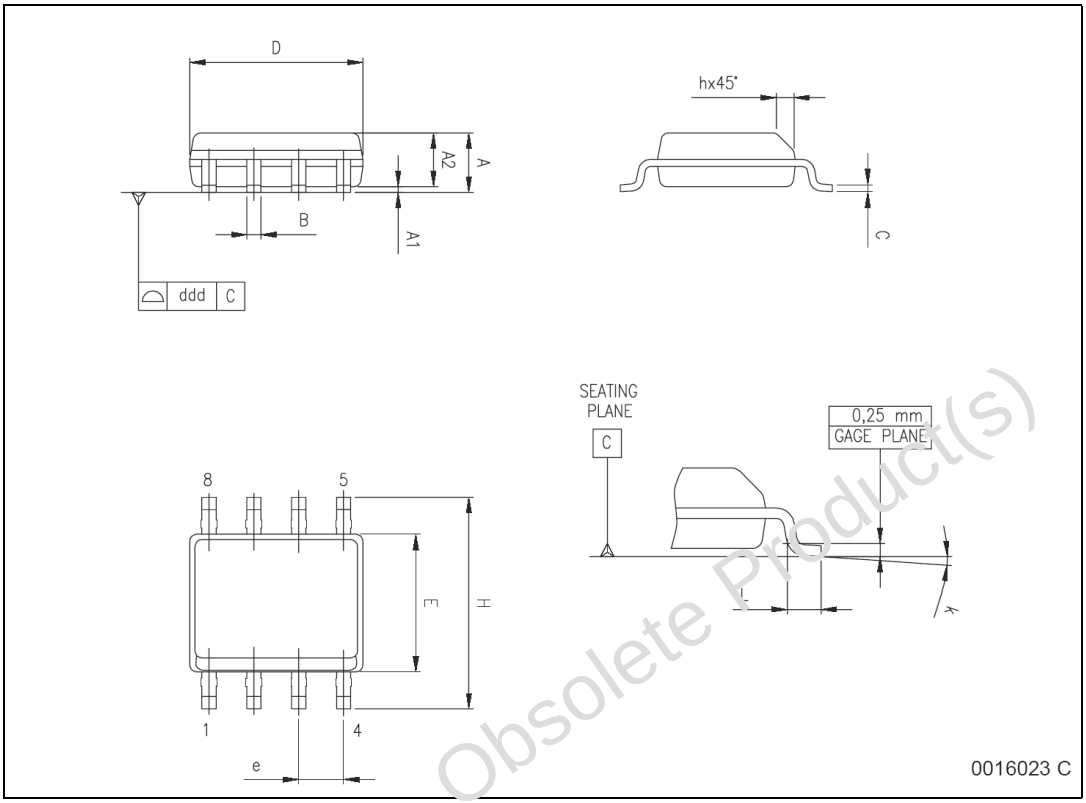
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 11. SO-8 mechanical data

Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.10			0.004

Figure 5. Package dimensions



7 Revision history

Table 12. Revision history

Date	Revision	Changes
13-Jul-2005	4	Add bullet on pag. 1, add paragraph in the description on pag. 1 and add row T_{FB} on Table 10.
29-May-2007	5	Updated features in cover page, document reformatted.
24-Nov-2010	6	Document reformatted, added “Not Recommended for New Design” and *Note 1* below *Table 1*, corrected typo in *Features*, *Description*, *Figure 1*, *Table 2* to *Table 8*, *Table 10*, title of *Figure 4*, updated *Table 1*, *Section 4.1*, *Section 5* and ECOPACK® text in *Section 6*.

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