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FDG6308P

P-Channel 1.8V Specified PowerTrench® MOSFET

General Description

This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

- · Battery management
- Load switch

Features

• -0.6 A, -20 V. $R_{DS(ON)} = 0.40$ Ω @ $V_{GS} = -4.5$ V $R_{DS(ON)} = 0.55$ Ω @ $V_{GS} = -2.5$ V $R_{DS(ON)} = 0.80$ Ω @ $V_{GS} = -1.8$ V

· Low gate charge

S 1 or 4

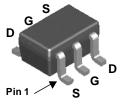
D 3 or 6

- High performance trench technology for extremely low R_{DS(ON)}
- Compact industry standard SC70-6 surface mount package

6 or 3 D

5 or 2 G

4 or 1 S



SC70-6

The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		± 8	V
I _D	Drain Current - Continuous	(Note 1)	-0.6	А
	- Pulsed		-1.8	
P _D	Power Dissipation for Single Operation	(Note 1)	0.3	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

R_{BJA} Thermal Resistance, Junction-to-Ambient (Note 1) 415 °C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.08	FDG6308P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics			•		
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	-20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		-15		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μА
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = 8 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	-0.4	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$, Referenced to 25°C		2		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$\begin{split} &V_{GS} = -4.5 \text{ V}, \ I_D = -0.6 \text{ A} \\ &V_{GS} = -2.5 \text{ V}, \ I_D = -0.5 \text{ A} \\ &V_{GS} = -1.8 \text{ V}, \ I_D = -0.4 \text{ A} \\ &V_{GS} = -4.5 \text{ V}, \ I_D = -0.6 \text{ A}, \ T_J = 125 ^{\circ}\text{C} \end{split}$		0.27 0.36 0.55 0.35	0.40 0.55 0.80 0.56	Ω
I _{D(on)}	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, \ V_{DS} = -5 \text{ V}$	-2			Α
g FS	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -0.6 \text{ A}$		2.1		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$		153		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		25		pF
C _{rss}	Reverse Transfer Capacitance			9		pF
Switchin	g Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, I_{D} = 1 \text{ A},$		5	10	ns
t _r	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		15	27	ns
t _{d(off)}	Turn-Off Delay Time			7	14	ns
t _f	Turn-Off Fall Time			1.6	3.2	ns
Q _g	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_{D} = -0.6 \text{ A},$		1.8	2.5	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$		0.3		nC
Q_{gd}	Gate-Drain Charge			0.4		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				-0.25	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, \qquad I_S = -0.25 \text{ A}(\text{Note 2})$		-0.77	-1.2	V

Notes

^{1.} $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA} = 415^{\circ}$ C/W when mounted on a minimum pad .

^{2.} Pulse Test: Pulse Width < $300\mu s$, Duty Cycle < 2.0%

Typical Characteristics

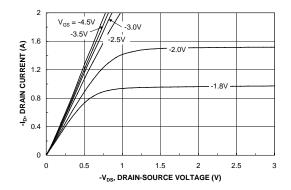


Figure 1. On-Region Characteristics.

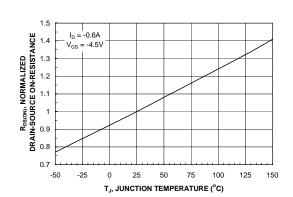


Figure 3. On-Resistance Variation with Temperature.

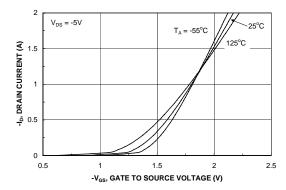


Figure 5. Transfer Characteristics.

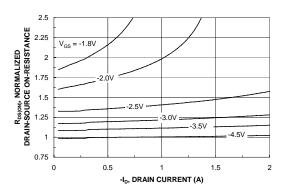


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

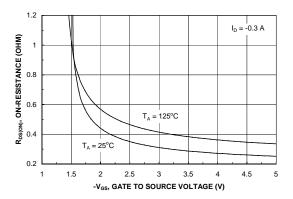


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

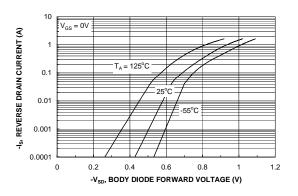
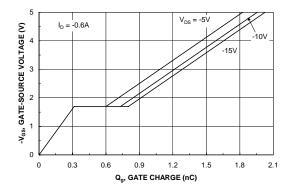


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

FDG6308P Rev C (W)

Typical Characteristics



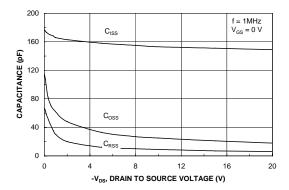


Figure 7. Gate Charge Characteristics.

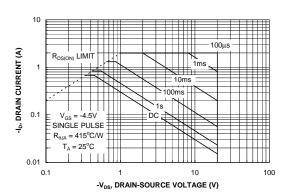


Figure 8. Capacitance Characteristics.

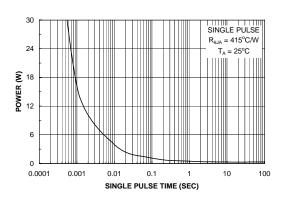


Figure 9. Maximum Safe Operating Area.



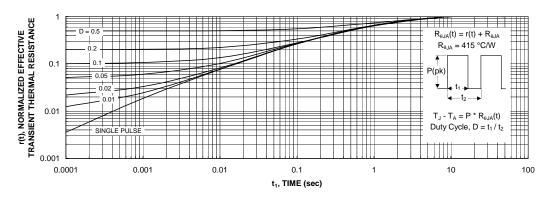


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1. Transient thermal response will change depending on the circuit board design.

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