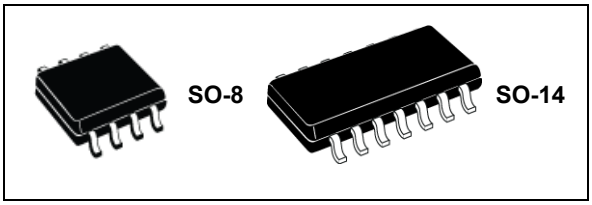
L6498

High voltage high and low-side 2 A gate driver

Datasheet - production data



Features

- Transient withstand voltage 600 V
- dV/dt immunity ± 50 V/ns in full temperature range
- Driver current capability:
  - 2 A source typ. at 25 °C
  - 2.5 A sink typ. at 25 °C
- Short propagation delay: 85 ns
- Switching times 25 ns rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Interlocking function
- UVLO on both high-side and low-side sections
- Compact and simplified layout
- Bill of material reduction
- Flexible, easy and fast design

Applications

- Motor driver for home appliances, factory automation, industrial drives and fans
- HID ballasts
- Power supply units
- DC-DC converters
- Induction heating
- Wireless chargers
- Industrial inverters
- UPS
- Welding

Description

The L6498 is a high voltage device manufactured with the BCD6 “OFF-LINE” technology. It is a single chip half-bridge gate driver for the N-channel power MOSFET or IGBT.

The high-side (floating) section is designed to stand a DC voltage rail up to 500 V, with 600 V transient withstand voltage. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing control units such as microcontrollers or DSP.

Both device outputs can sink 2.5 A and source 2 A, making the L6498 particularly suited for medium and high capacity power MOSFETs\IGBTs.

The outputs cannot be simultaneously driven high thanks to an integrated interlocking function.

The independent UVLO protection circuits present on both the lower and upper driving sections prevent the power switches from being operated in low efficiency or dangerous conditions.

The integrated bootstrap diode as well as all of the integrated features of this driver make the application PCB design simpler and more compact, and help to reduce the overall bill of material.

Contents

1 Block diagrams

Figure 1. Block diagram SO-8

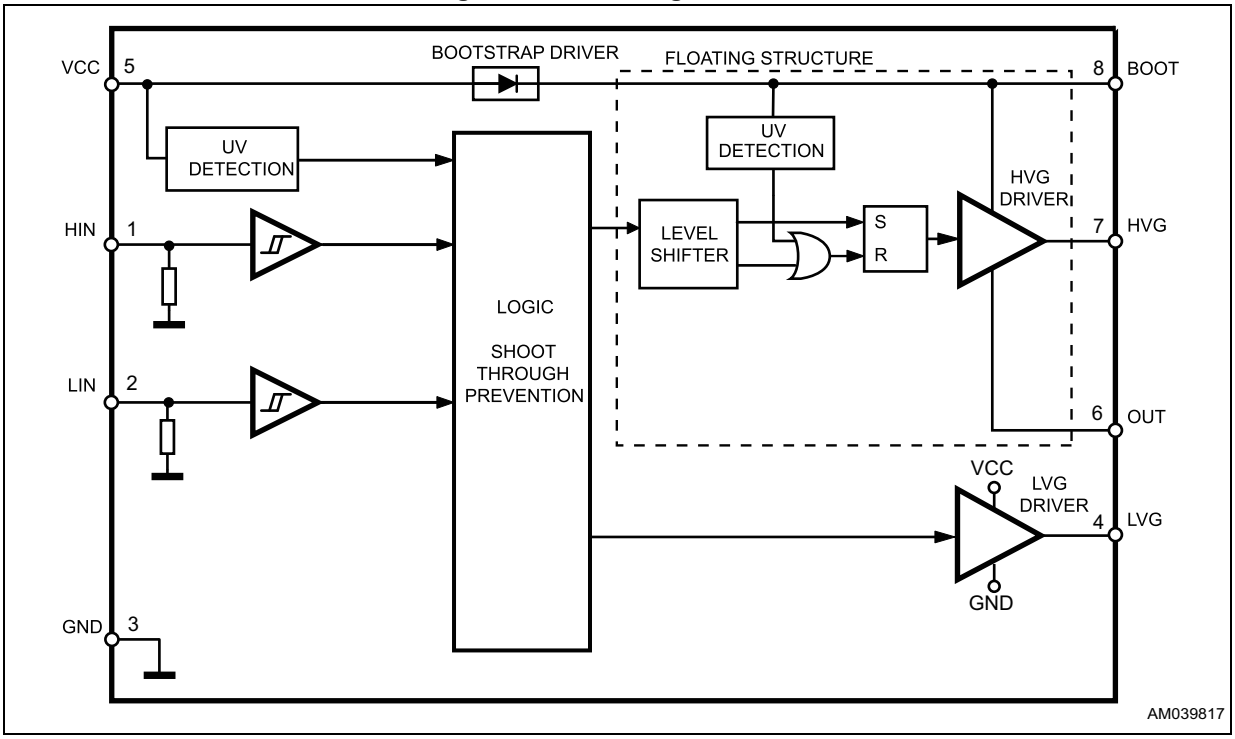
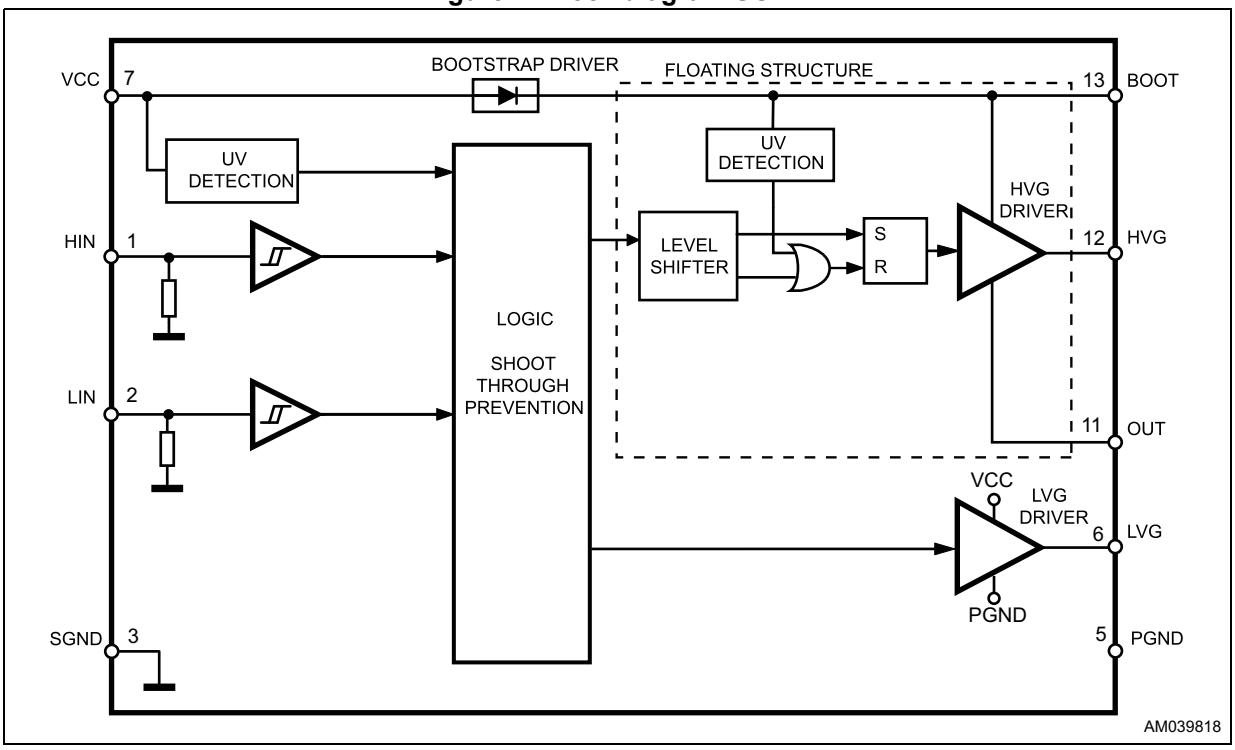


Figure 2. Block diagram SO-14



2 Pin description and connection diagram

Figure 3. Pin connection SO-8 (top view)

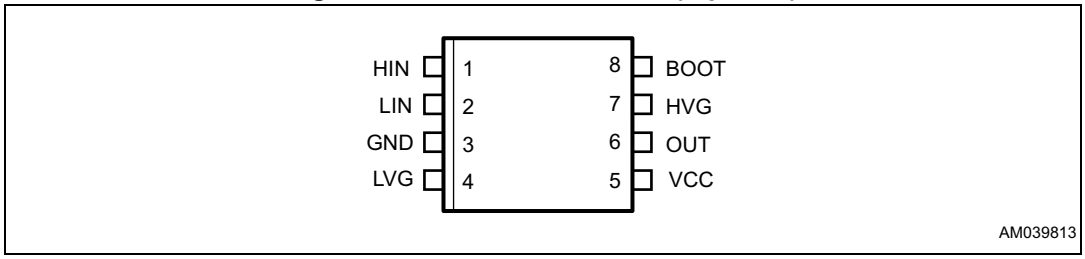


Figure 4. Pin connection SO-14 (top view)

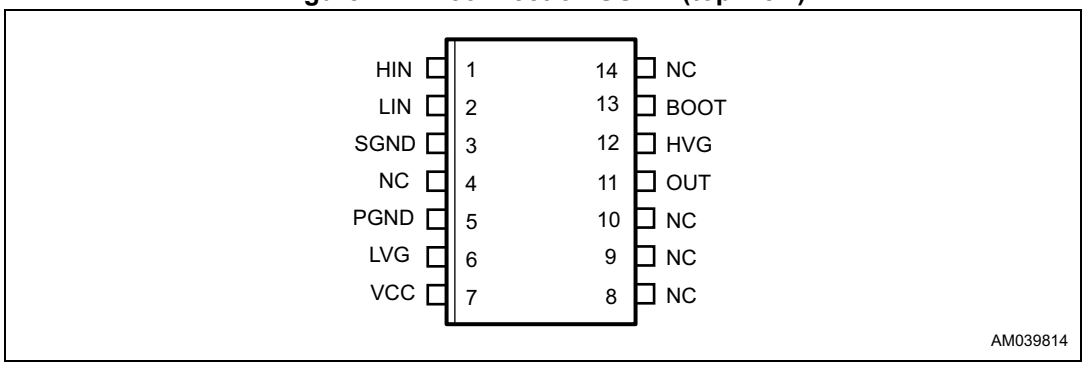


Table 1. Pin description

Pin no.		Pin name	Type	Function
SO-8	SO-14			
1	1	HIN	I	High-side driver logic input (active high)
2	2	LIN	I	Low-side driver logic input (active high)
3	-	GND	P	Device ground
4	6	LVG(1)	O	Low-side driver output
5	7	VCC	P	Lower section supply voltage
6	11	OUT	P	High-side (floating) common voltage
7	12	HVG(1)	O	High-side driver output
8	13	BOOT	P	Bootstrapped supply voltage
-	3	SGND	P	Signal ground
-	5	PGND	P	Power ground
-	4, 8, 9, 10, 14	NC	-	Not connected

1. The circuit guarantees less than 1 V on the LVG and HVG pins (at I_{sink} = 10 mA), with V_{CC} > 3 V. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings(1)

Symbol	Parameter	Value		Unit
		Min.	Max.	
V_{CC}	Supply voltage	-0.3	21	V
V_{PGND}	Low-side driver ground	V_{CC} - 21	V_{CC} + 0.3	V
V_{OUT}	Output voltage	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{BOOT}	Boot DC voltage	-0.3	500	V
	Boot transient withstand voltage (T_{pulse} < 1 ms)	-	620	V
V_{hvg}	High-side gate output voltage	V_{OUT} - 0.3	V_{BOOT} + 0.3	V
V_{lvg}	Low-side gate output voltage	(P)GND - 0.3	V_{CC} + 0.3	V
V_i	Logic input pins voltage	-0.3	15	V
dV_{OUT}/dt	Allowed output slew rate	-	50	V/ns
P_{TOT}	Total power dissipation (T_A = 25 °C) SO-14	-	1	W
T_J	Junction temperature	-	150	°C
T_{stg}	Storage temperature	-50	150	°C
ESD	Human body model	2		kV

1. Each voltage referred to GND\SGND unless otherwise specified.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	SO-8	185	°C/W
		SO-14	120	

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
V_{CC}	VCC	Supply voltage	-	10	20	V
V_{PS}(1)	SGND - PGND	Low-side driver ground	-	-5	+5	V
V_{BO}(2)	BOOT - OUT	Floating supply voltage	-	9.3	20	V
V_{OUT}	OUT	DC output voltage	-	- 9(3)	480	V
		OUT transient withstand voltage	T_{pulse} < 1 ms	-	600	V
f_{SW}	-	Maximum switching frequency	HVG, LVG load C_L = 1 nF	-	800	kHz
T_J	-	Junction temperature	-	-40	125	°C
T_A	-	Ambient temperature(4)	-	-40	125	°C

1. $V_{PS} = V_{PGND}$ - SGND.
2. $V_{BO} = V_{BOOT} - V_{OUT}$.
3. LVG off. V_{CC} = 12.5 V. Logic is operational if V_{BOOT} > 5 V.
4. Maximum ambient temperature is actually limited by T_J.

4 Electrical characteristics

Table 5. Electrical characteristics (V_{CC} = 15 V; T_J = +25 °C; PGND = SGND

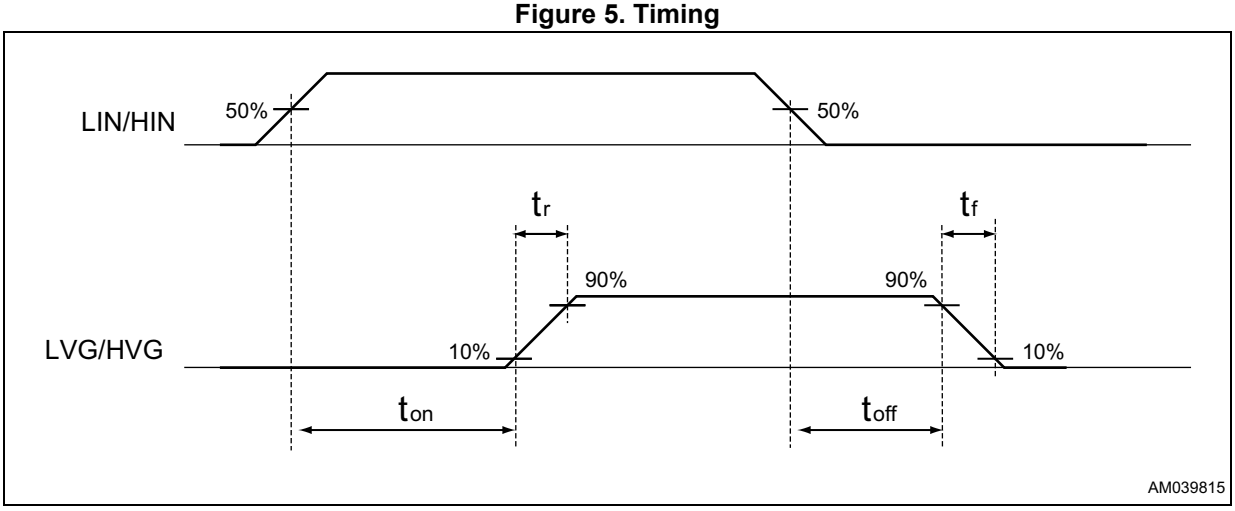
Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Low-side section supply							
V_{CC_hys}	VCC vs. (S)GND	V_{CC} UV hysteresis	-	0.5	0.6	0.72	V
V_{CC_thON}		V_{CC} UV turn ON threshold	-	8.7	9.3	9.8	V
V_{CC_thOFF}		V_{CC} UV turn OFF threshold	-	8.2	8.7	9.2	V
I_{QCCU}		Undervoltage quiescent supply current	V_{CC} = 7 V LIN = GND; HIN = GND	-	160	210	µA
I_{QCC}		Quiescent current	V_{CC} = 15 V LIN = 5 V; HIN = GND	-	340	480	µA
High-side floating section supply(1)							
V_{BO_hys}	BOOT vs. OUT	V_{BO} UV hysteresis	-	0.48	0.6	0.7	V
V_{BO_thON}		V_{BO} UV turn ON threshold	-	8.0	8.6	9.1	V
V_{BO_thOFF}		V_{BO} UV turn OFF threshold	-	7.5	8.0	8.5	V
I_{QBOU}		Undervoltage V_{BO} quiescent current	V_{BO} = 7 V LIN = GND; HIN = 5 V	-	20	30	µA
I_{QBO}		V_{BO} quiescent current	V_{BO} = 15 V LIN = GND; HIN = 5 V	-	90	120	µA
I_{LK}	-	High voltage leakage current	$V_{hvg} = V_{OUT} = V_{BOOT}$ = 600 V	-	-	8	µA
$R_{DS(on)}$	-	Bootstrap diode on resistance(2)	-	-	175	-	Ω
Output driving buffers							
I_{so}	LVG, HVG	High/low-side source short-circuit current	LVG/HVG ON T_J = 25 °C	1.7	2	-	A
			Full temperature range	1.4	-	-	A
I_{si}		High/low-side sink short-circuit current	LVG/HVG ON T_J = 25 °C	2	2.5	-	A
			Full temperature range	1.55	-	-	A
Logic inputs							
V_{il}	LIN, HIN vs. (S)GND	Low level logic threshold voltage	-	0.95	-	1.45	V
V_{ih}		High level logic threshold voltage	-	2	-	2.5	V
I_{HINh}	HIN vs. (S)GND	HIN logic “1” input bias current	HIN = 15 V	120	200	260	µA
I_{HINl}		HIN logic “0” input bias current	HIN = 0 V	-	-	1	µA
I_{LINl}	LIN vs. (S)GND	LIN logic “1” input bias current	LIN = 15 V	120	200	260	µA
I_{LINh}		LIN logic “0” input bias current	LIN = 0 V	-	-	1	µA

Table 5. Electrical characteristics (V_{CC} = 15 V; T_J = +25 °C; PGND = SGND (continued)

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{PD}	LIN, HIN vs. (S)GND	Logic inputs pull-down resistor	-	58	75	125	kΩ
Dynamic characteristics (see *Figure 5*)							
t_{on}	HIN vs. HVG; LIN vs. LVG	High/low-side driver turn-on propagation delay	V_{OUT} = 0 V; V_{BOOT} = V_{CC}; C_L = 1 nF; V_i = 0 to 3.3 V	-	85	120	ns
t_{off}		High/low-side driver turn-off propagation delay		-	85	120	ns
MT	-	Delay matching, HS and LS turn-on/off(3)	-	-	-	30	ns
t_r	LVG, HVG	Rise time	C_L = 1 nF	-	25	-	ns
t_f		Fall time	C_L = 1 nF	-	25	-	ns

1. V_{BO} = V_{BOOT} - V_{OUT}.
2. R_{DSON} is tested in the following way:
   R_{DSON} = [(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})] / [I_1 (V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})]
   where I_1 is BOOT pin current when V_{BOOT} = V_{BOOT1}, I_2 when V_{BOOT} = V_{BOOT2}.
3. MT = max. (|t_{on} (LVG) - t_{off} (LVG)|, |t_{on} (HVG) - t_{off} (HVG)|, |t_{off} (LVG) - t_{on} (HVG)|, |t_{off} (HVG) - t_{on} (LVG)|).

Figure 5. Timing



5 Truth table

Table 6. Truth table

Input		Output	
LIN	**HIN**	**LVG**	**HVG**
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L(1)	L(1)

1. Interlocking function.

6 Typical application diagram

Figure 6. Typical application diagram

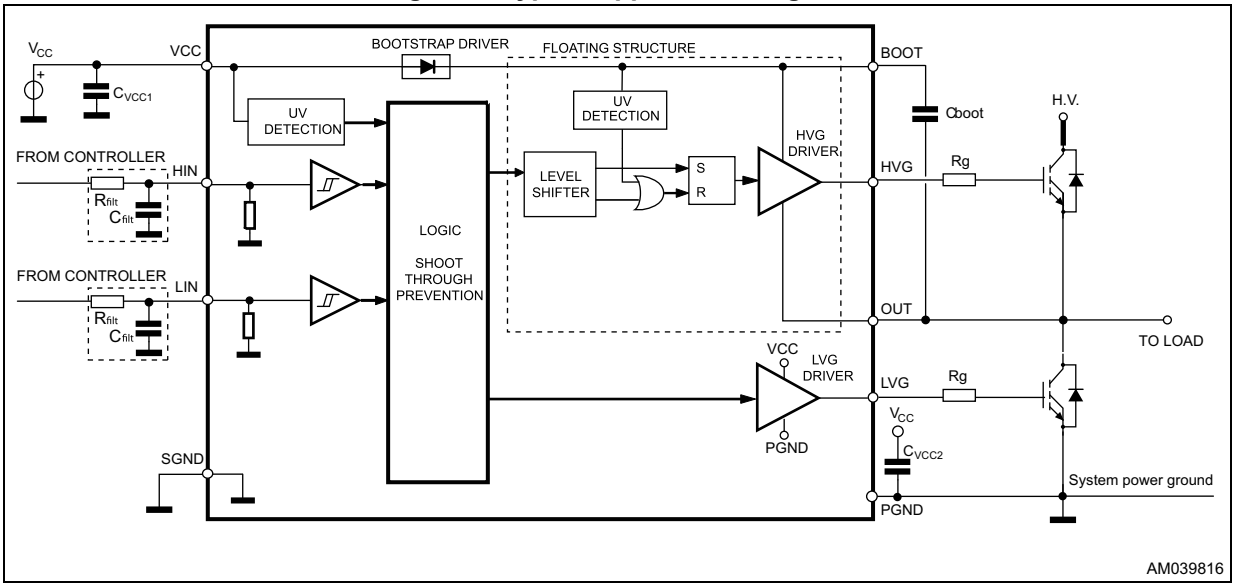


Figure 7. Suggested PCB layout (SO-8)

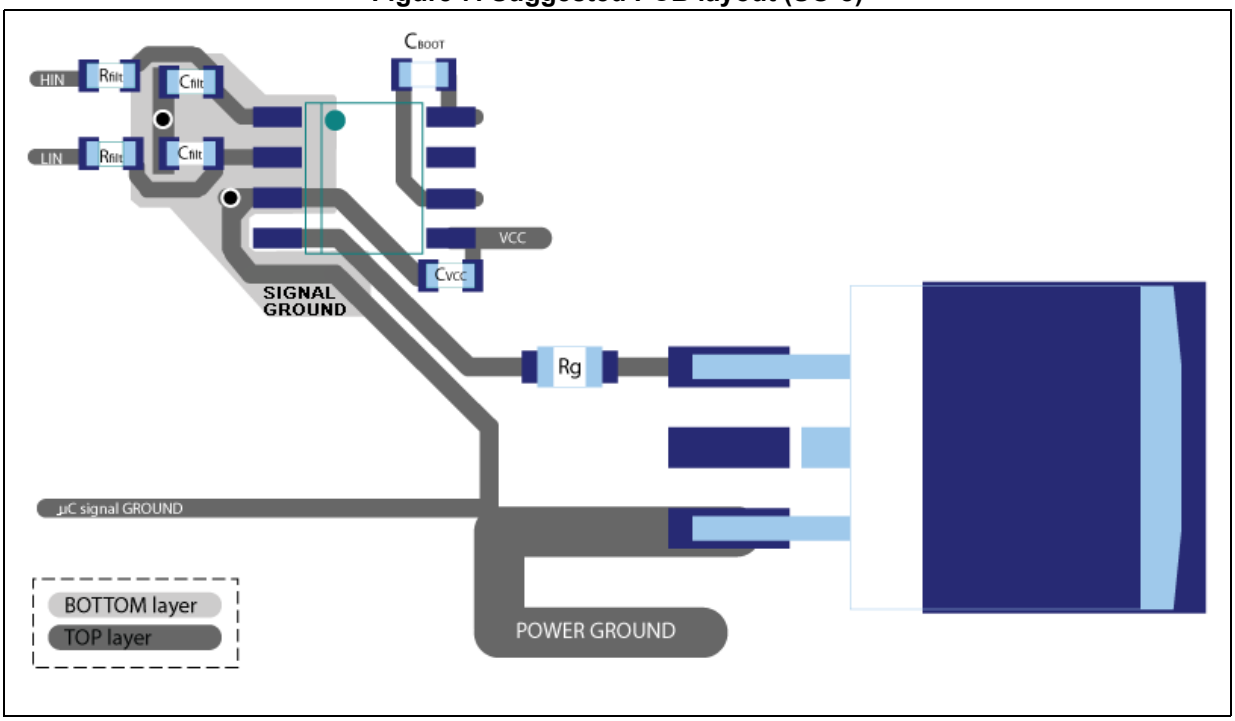
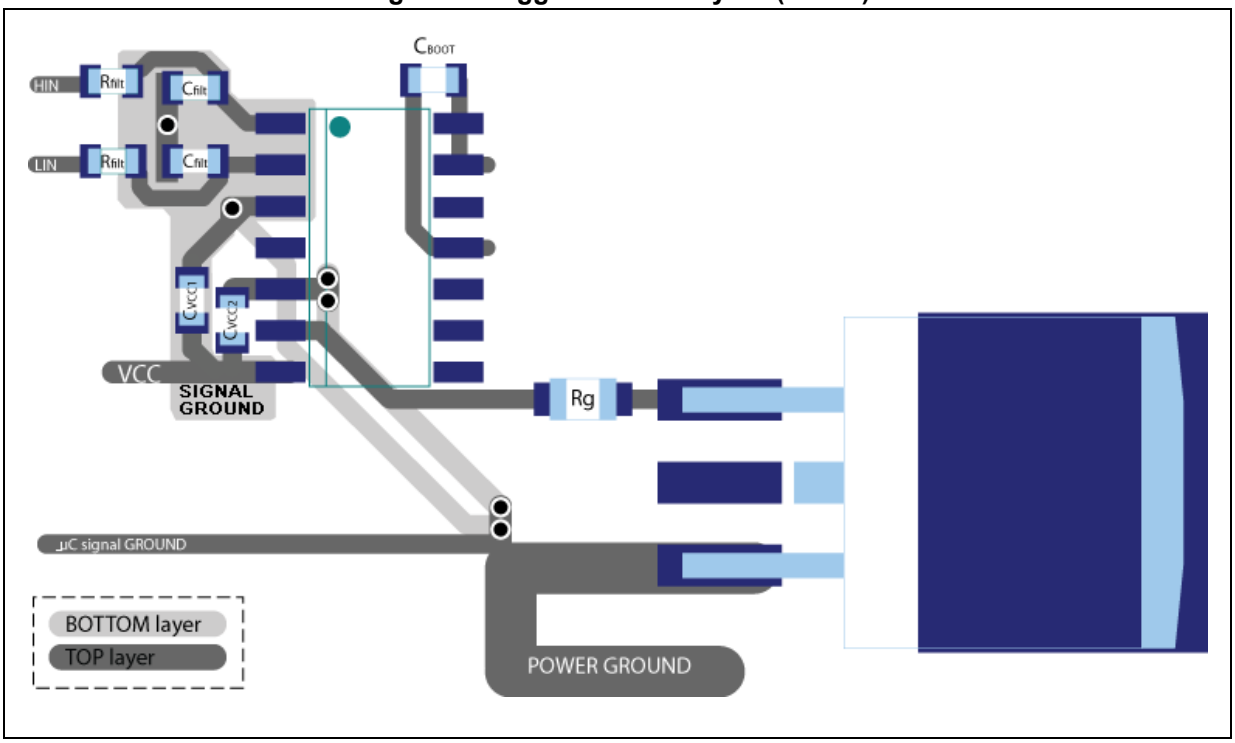


Figure 8. Suggested PCB layout (SO-14)



7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is usually accomplished by a high voltage fast recovery diode (*Figure 9*). In the L6498 an integrated structure replaces the external diode.

C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} >>> C_{EXT}$$

if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop is 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has also to take into account the leakage and quiescent losses.

HVG steady-state consumption is lower than 120 µA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 0.6 µC. This charge on a 1 µF capacitor means a voltage drop of 0.6 V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to SGND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 175 Ω). At low frequency this drop can be neglected. Anyway, the rise of frequency has to take into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{drop} = I_{charge} R_{DS(on)} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{DS(on)}$$

where Q_{gate} is the gate charge of the external power MOS, $R_{DS(on)}$ is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

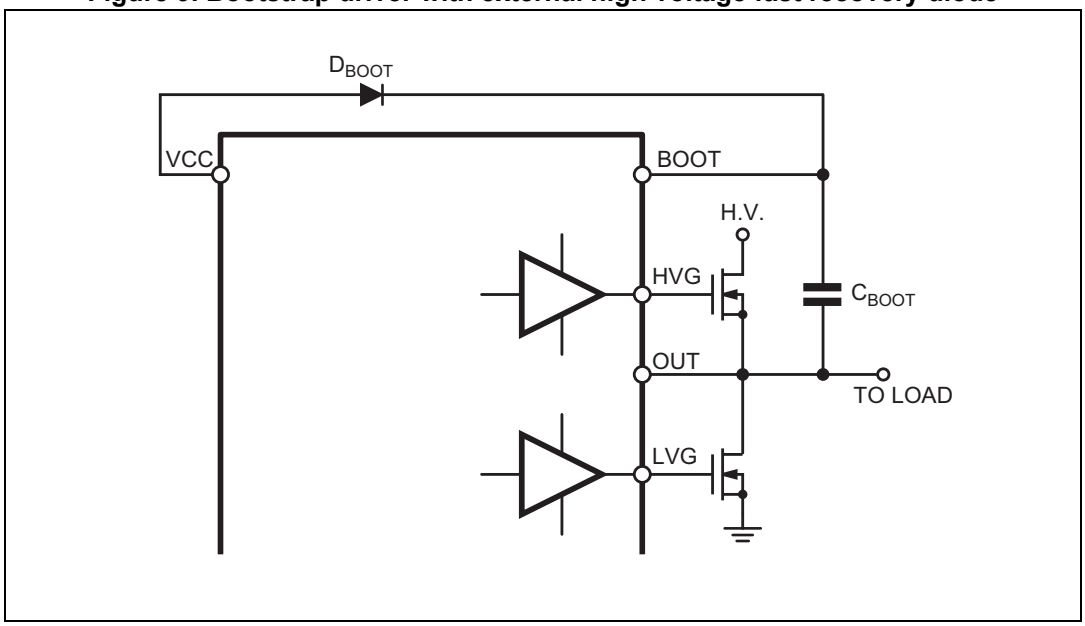
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

Equation 4

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 175\Omega \sim 1V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 9. Bootstrap driver with external high voltage fast recovery diode



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

8.1 SO-8 package information

Figure 10. SO-8 package outline

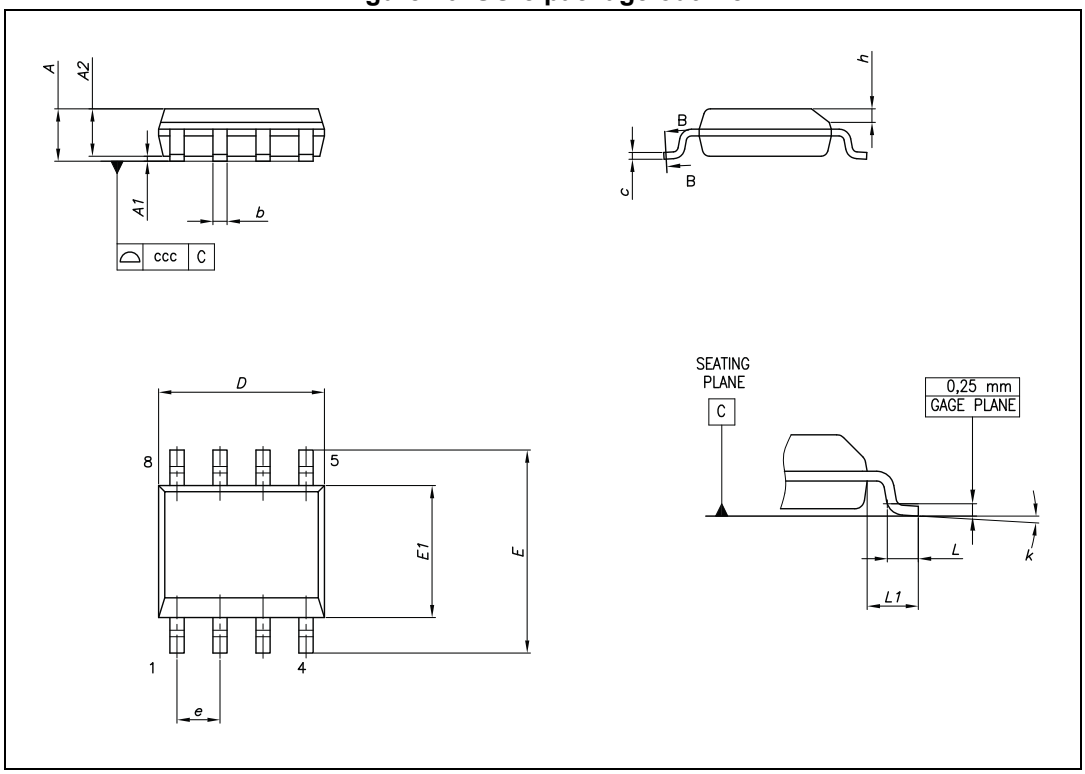
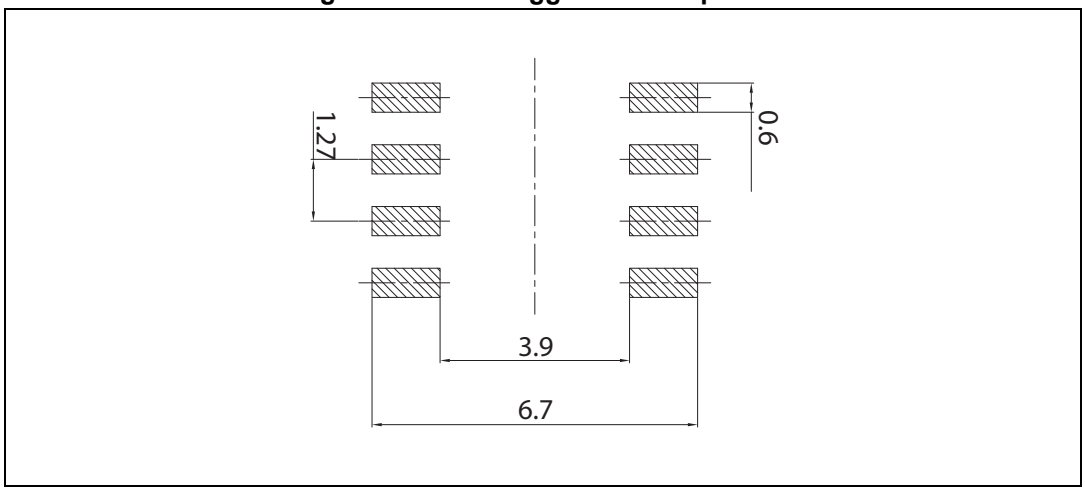


Table 7. SO-8 package mechanical data

Symbol	Dimensions (mm)			Notes
	Min.	Typ.	Max.	
A	-	-	1.75	-
A1	0.10	-	0.25	-
A2	1.25	-	-	-
b	0.28	-	0.48	-
c	0.17	-	0.23	-
D	4.80	4.90	5.00	-
E	5.80	6.00	6.20	-
E1	3.80	3.90	4.00	-
e	-	1.27	-	-
h	0.25	-	0.50	-
L	0.40	-	1.27	-
L1	-	1.04	-	-
k	0	-	8	Degrees
ccc	-	-	0.10	-

Figure 11. SO-8 suggested land pattern



8.2 SO-14 package information

Figure 12. SO-14 package outline

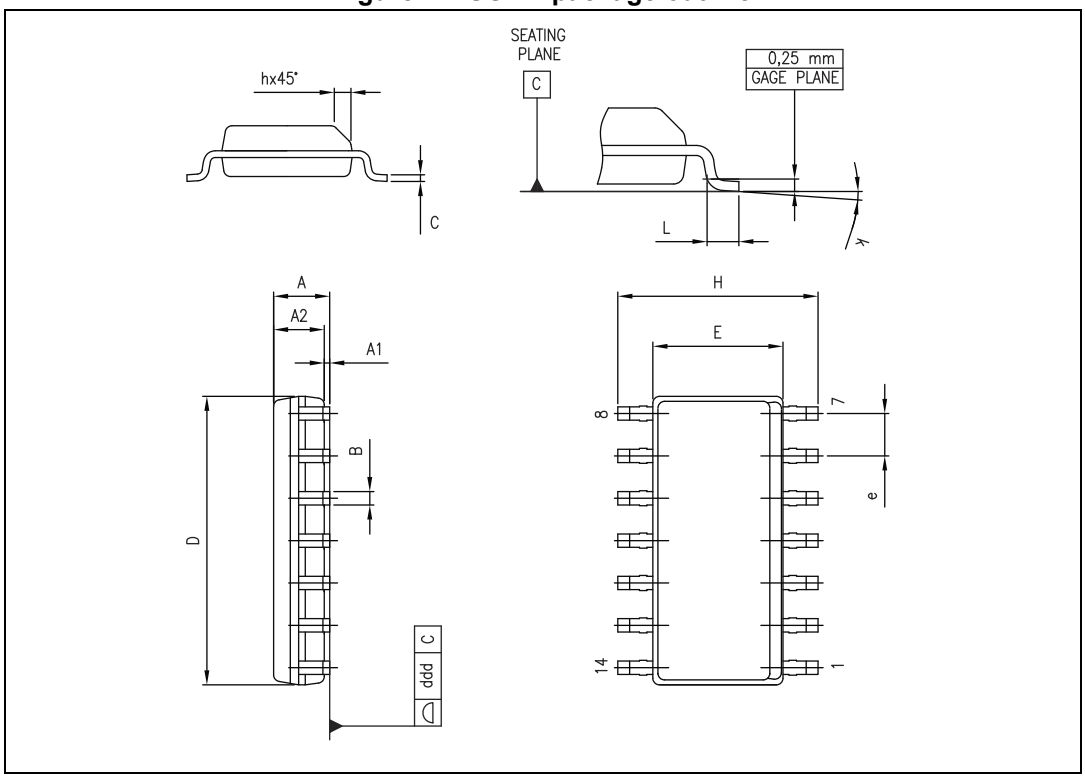
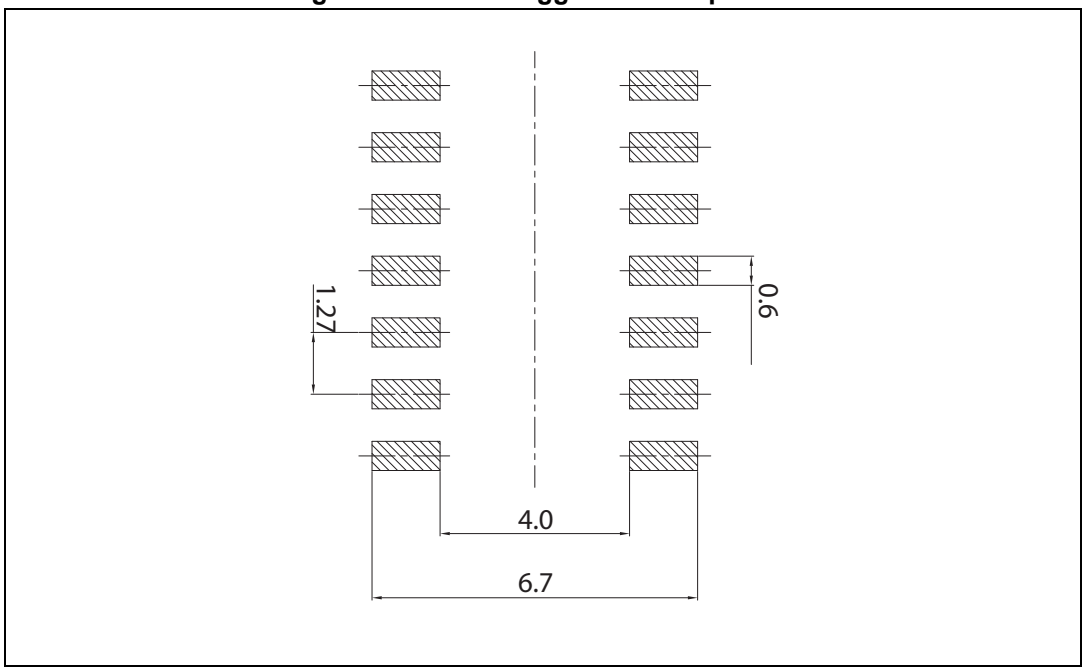


Table 8. SO-14 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.10	-	1.65
B	0.33	-	0.51
C	0.19	-	0.25
D	8.55	-	8.75
E	3.80	-	4.00
e	-	1.27	-
H	5.80	-	6.20
h	0	-	-
25	-	0.50	-
L	0.40	-	1.27
k	0	-	8
ddd	-	-	0.10

Figure 13. SO-14 suggested land pattern



9 Ordering information

Table 9. Device summary

Order code	Package	Packaging
L6498D	SO-8	Tube
L6498DTR	SO-8	Tape and reel
L6498LD	SO-14	Tube
L6498LDTR	SO-14	Tape and reel

10 Revision history

Table 10. Document revision history

Date	Revision	Changes
08-Feb-2017	1	Initial release.
26-Apr-2017	2	Updated *Table 5 on page 7* (replaced “I_{NR_PD}” by “R_{PD}”, added Test condition to “t_{off}”). Updated order codes in *Table 9 on page 19*. Minor modifications throughout document.
13-Sep-2017	3	Updated *Table 4 on page 6* (added T_A symbol and note *4.*).