

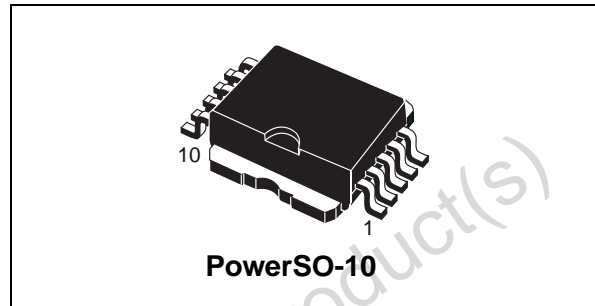
## Double channel high-side driver

### Features

Type	$R_{DS(on)}$	$I_{OUT}$	$V_{CC}$
VND830LSP	60 m $\Omega$ <sup>(1)</sup>	18 A <sup>(1)</sup>	36 V

1. Per each channel.

- CMOS compatible inputs
- Open drain status outputs
- On-state open-load detection
- Off-state open-load detection
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Loss of ground protection
- Very low standby current
- Reverse battery protection



### Description

The VND830LSP is a monolithic device designed using STMicroelectronics™ VIPower™ M0-3 Technology. The VND830LSP is intended for driving any type of multiple load with one side connected to ground.

The Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). Active current limitation combined with thermal shutdown and automatic restart protects the device against overload.

The open-load threshold is aimed at detecting the 5 W / 12 V standard bulb as an open-load fault in the on-state.

The device detects the open-load condition in both the on and off-state. In the off-state the device detects if the output is shorted to  $V_{CC}$ . The device automatically turns off in the case where the ground pin becomes disconnected.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VND830LSP	VND830LSP13TR

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# 1 Block diagram and pin description

Figure 1. Block diagram

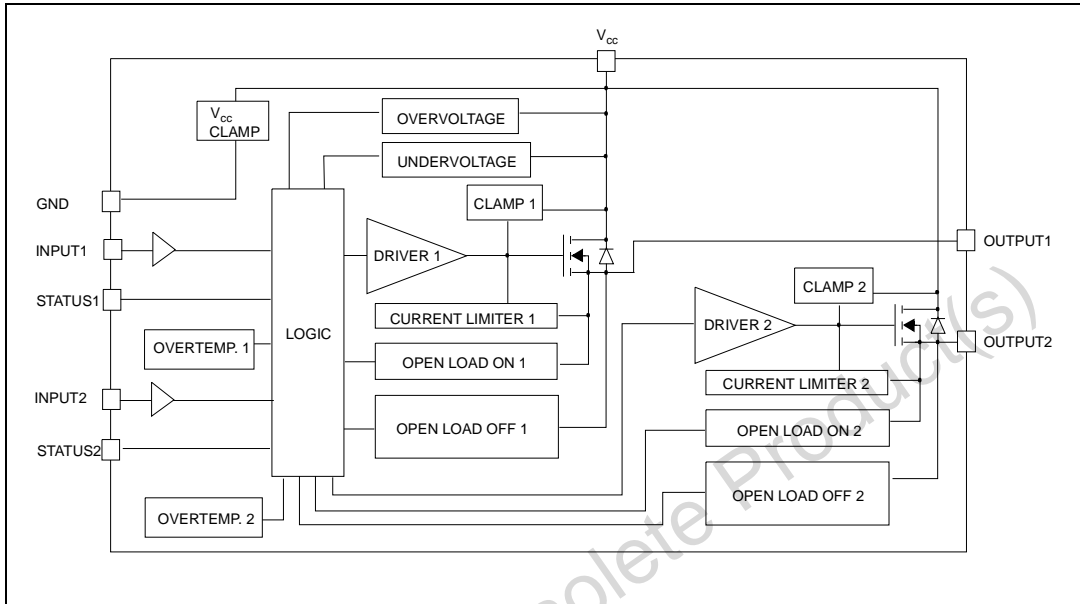


Figure 2. Configuration diagram (top view)

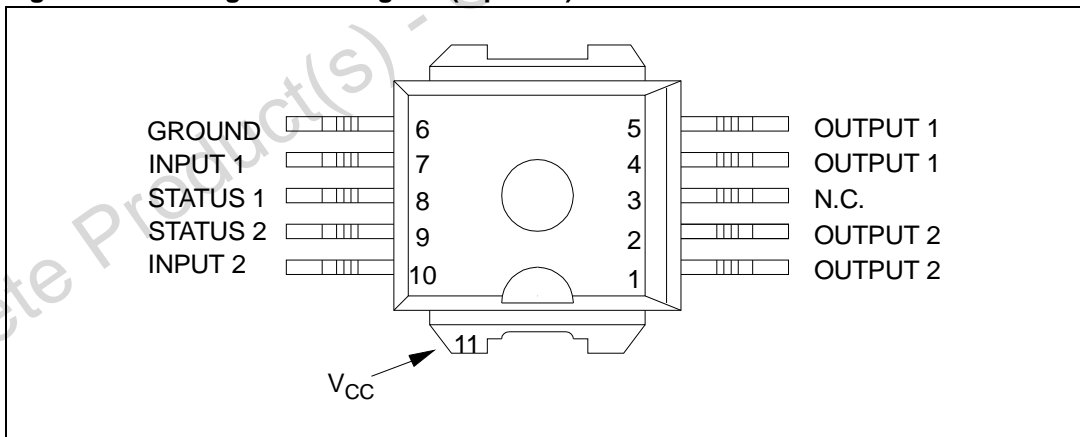


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10KΩ resistor

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	- 0.3	V
$-I_{GND}$	DC reverse ground pin current	- 200	mA
$I_{OUT}$	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	- 6	A
$I_{IN}$	DC input current	+/- 10	mA
$I_{STAT}$	DC Status current	+/- 10	mA
$V_{ESD}$	Electrostatic discharge (human body model: R = 1.5 K $\Omega$ ; C = 100 pF)		
	– INPUT	4000	V
	– STATUS	4000	V
	– OUTPUT	5000	V
	– $V_{CC}$	5000	V
$E_{MAX}$	Maximum switching energy (L = 0.14 mH; R <sub>L</sub> = 0 $\Omega$ ; V <sub>bat</sub> = 13.5 V; T <sub>jstart</sub> = 150 °C; I <sub>L</sub> = 14 A)	52	mJ
$P_{tot}$	Power dissipation (per island) at T <sub>lead</sub> = 25 °C	74	W
$T_j$	Junction operating temperature	Internally limited	°C
$T_c$	Case operating temperature	- 40 to 150	
$T_{stg}$	Storage temperature	- 55 to 150	°C

## 2.2 Thermal data

**Table 4. Thermal data (per island)**

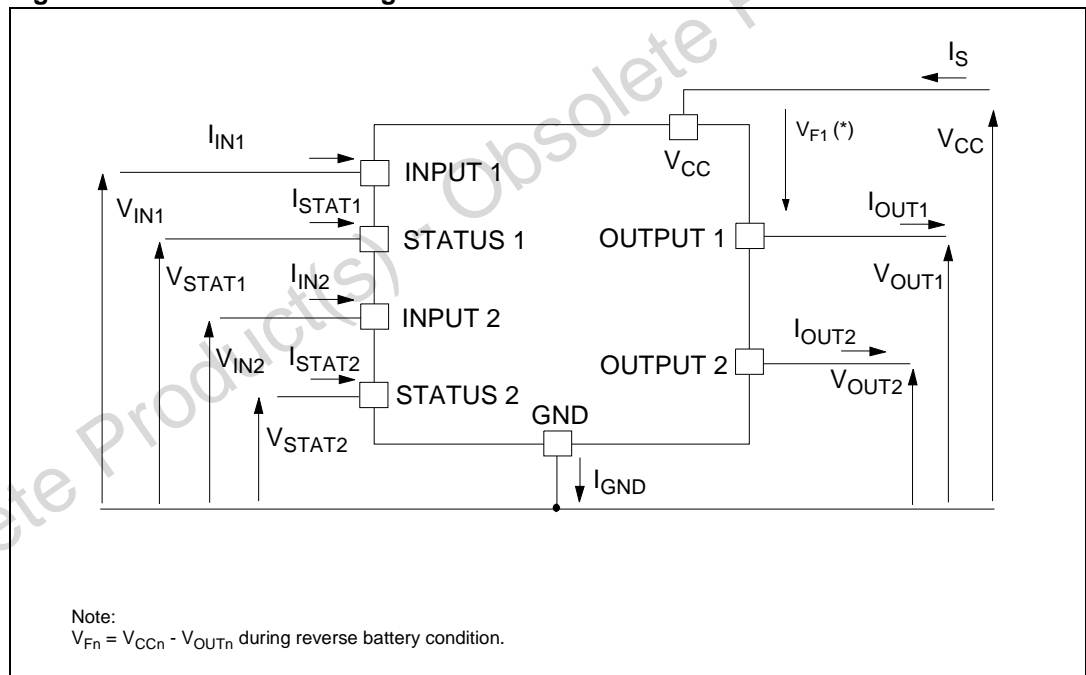
Symbol	Parameter	Value		Unit
$R_{thj-lead}$	Thermal resistance junction-lead	2		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	52 <sup>(1)</sup>	37 <sup>(2)</sup>	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5 cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6 cm<sup>2</sup> of Cu (at least 35 μm thick) connected to all V<sub>CC</sub> pins. Horizontal mounting and no artificial air flow.

## 2.3 Electrical characteristics

Values specified in this section are for 8 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>j</sub> < 150 °C, unless otherwise stated.

**Figure 3. Current and voltage conventions**



**Table 5. Power output**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		5.5	13	36	V
$V_{USD}$	Undervoltage shutdown		3	4	5.5	V
$V_{OV}$	Overvoltage shutdown		36			V
$R_{ON}$	On-state resistance	$I_{OUT} = 2A; T_j = 25^\circ C$ $I_{OUT} = 2A; V_{CC} > 8V$			60 120	m $\Omega$ m $\Omega$
$I_S$	Supply current	Off-state; $V_{CC} = 13 V$ ; $V_{IN} = V_{OUT} = 0 V$		12	40	$\mu A$
		Off-state; $V_{CC} = 13 V$ ; $V_{IN} = V_{OUT} = 0 V$ ; $T_j = 25^\circ C$		12	25	$\mu A$
		On-state; $V_{CC} = 13 V$ ; $V_{IN} = 5 V$ ; $I_{OUT} = 0 A$		5	7	mA
$I_{L(off1)}$	Off-state output current	$V_{IN} = V_{OUT} = 0 V$	0		50	$\mu A$
$I_{L(off2)}$	Off-state output current	$V_{IN} = 0V; V_{OUT} = 3.5 V$	-75		0	$\mu A$
$I_{L(off3)}$	Off-state output current	$V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V$ ; $T_j = 125^\circ C$			5	$\mu A$
$I_{L(off4)}$	Off-state output current	$V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V$ ; $T_j = 25^\circ C$			3	$\mu A$

**Table 6. Protections**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$T_{TSD}$	Shutdown temperature		150	175	200	$^\circ C$
$T_R$	Reset temperature		135			$^\circ C$
$T_{hyst}$	Thermal hysteresis		7	15		$^\circ C$
$t_{SDL}$	Status delay in overload conditions	$T_j > T_{TSD}$			20	$\mu s$
$I_{lim}$	Current limitation	$V_{CC} = 13 V$	18	23	29	A
		$5.5 V < V_{CC} < 36 V$			29	A
$V_{demag}$	Turn-off output clamp voltage	$I_{OUT} = 2 A; L = 6 mH$	$V_{CC} - 41$	$V_{CC} - 48$	$V_{CC} - 55$	V

**Note:** To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.



**Table 7.  $V_{CC}$  - output diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_F$	Forward on voltage	$-I_{OUT} = 1.3 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	—	—	0.6	V

**Table 8. Switching ( $V_{CC} = 13 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5 \text{ } \Omega$ from $V_{IN}$ rising edge to $V_{OUT} = 1.3 \text{ V}$ (see <a href="#">Figure 5</a> )	5	30	60	$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5 \text{ } \Omega$ from $V_{IN}$ falling edge to $V_{OUT} = 11.7 \text{ V}$ (see <a href="#">Figure 5</a> )	10	30	70	$\mu\text{s}$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5 \text{ } \Omega$ from $V_{OUT} = 1.3 \text{ V}$ to $V_{OUT} = 10.4 \text{ V}$ (see <a href="#">Figure 5</a> )	0.15	See <a href="#">Figure 10</a>	1.5	$\text{V}/\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5 \text{ } \Omega$ from $V_{OUT} = 11.7 \text{ V}$ to $V_{OUT} = 1.3 \text{ V}$ (see <a href="#">Figure 5</a> )	0.1	See <a href="#">Figure 12</a>	0.75	$\text{V}/\mu\text{s}$

**Table 9. Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level				1.25	V
$I_{IL}$	Low level input current	$V_{IN} = 1.25 \text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level		3.25			V
$I_{IH}$	High level input current	$V_{IN} = 3.25 \text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1 \text{ mA}$	6	6.8	8	V
		$I_{IN} = -1 \text{ mA}$		-0.7		V

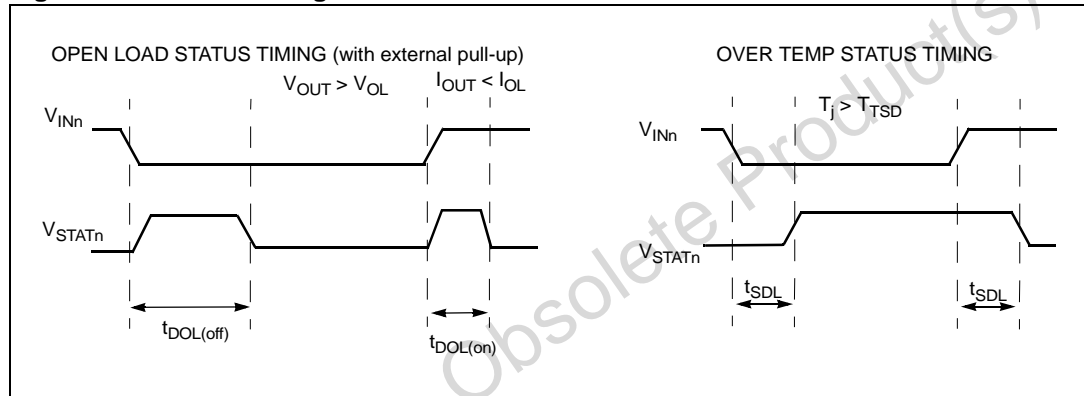
**Table 10. Status pin**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{STAT}$	Status low output voltage	$I_{STAT} = 1.6 \text{ mA}$			0.5	V
$I_{LSTAT}$	Status leakage current	Normal operation; $V_{STAT} = 5\text{V}$			10	$\mu\text{A}$
$C_{STAT}$	Status pin Input capacitance	Normal operation; $V_{STAT} = 5\text{V}$			100	pF
$V_{SCL}$	Status clamp voltage	$I_{STAT} = 1 \text{ mA}$	6	6.8	8	V
		$I_{STAT} = -1 \text{ mA}$		-0.7		V

**Table 11. Open-load detection**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{OL}$	Open-load on-state detection threshold	$V_{IN} = 5\text{ V}$	0.6	0.9	1.2	A
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0\text{ A}$			200	$\mu\text{s}$
$V_{OL}$	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	$\mu\text{s}$

**Figure 4. Status timings**



**Figure 5. Switching time waveforms**

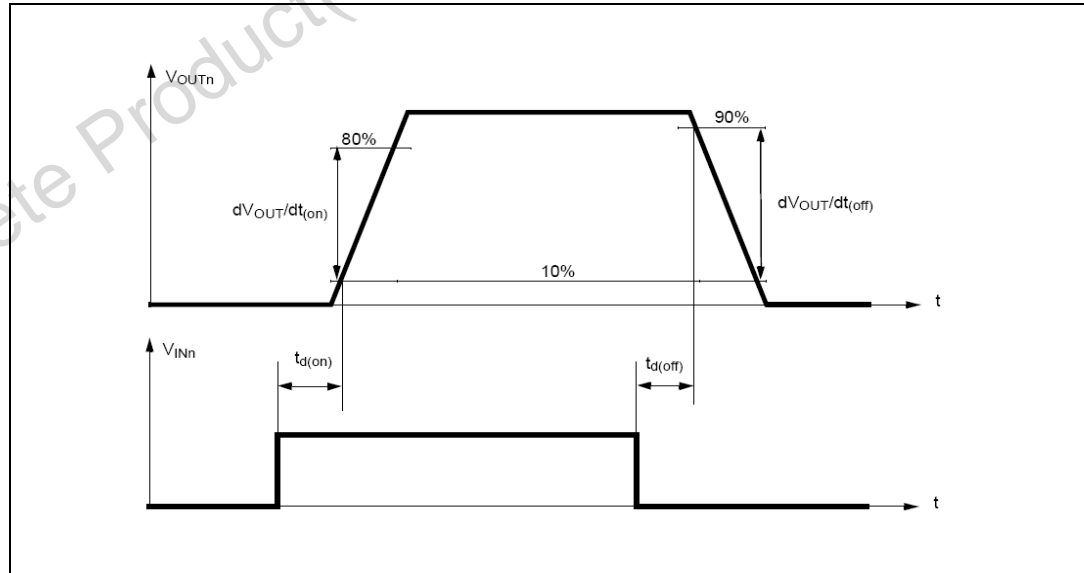


Table 12. Truth table

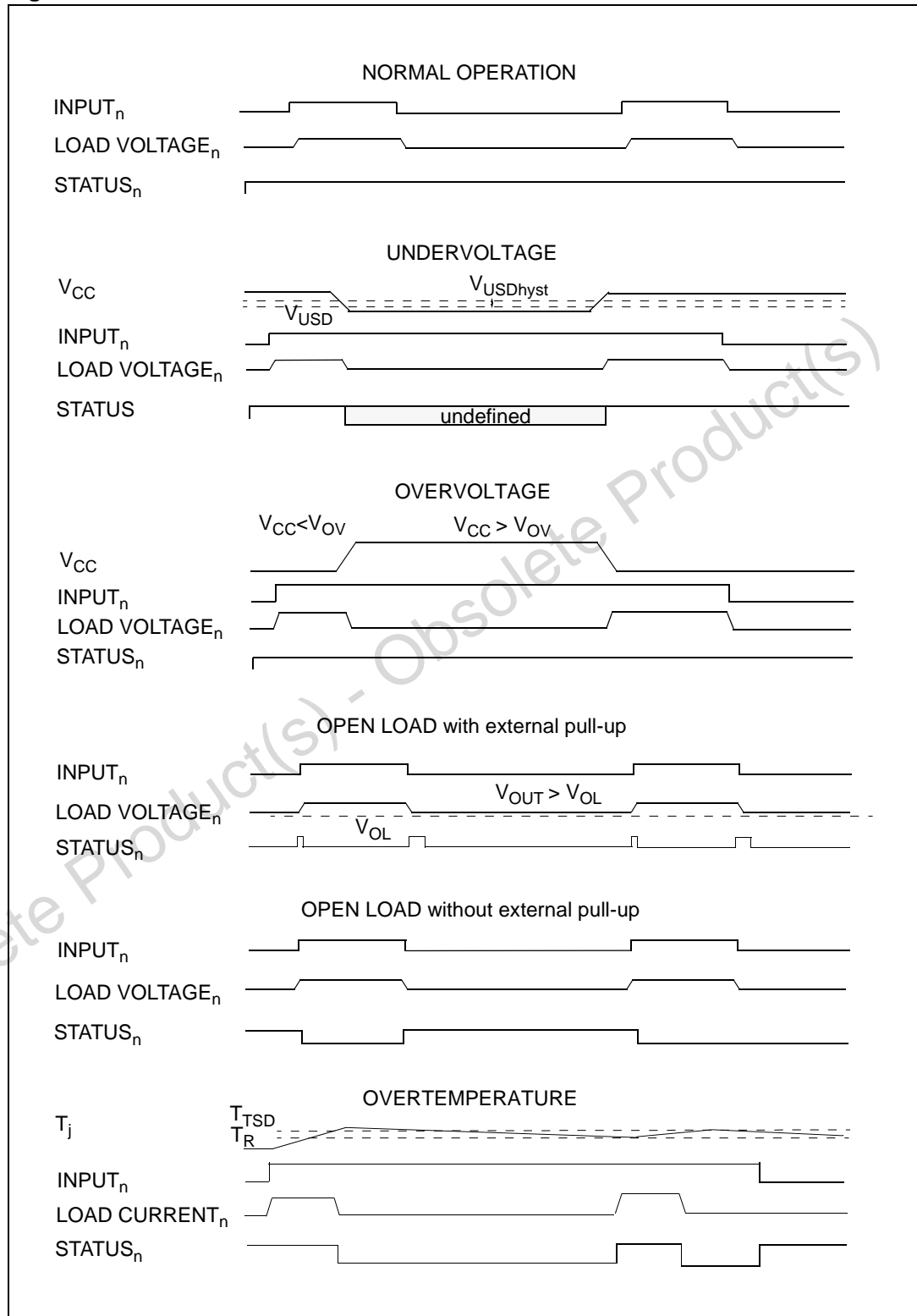
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_j < T_{TSD})$ H
	H	X	$(T_j > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage $> V_{OL}$	L	H	L
	H	H	H
Output current $< I_{OL}$	L	L	H
	H	H	L

Table 13. Electrical transient requirements

ISO T/R 7637/1 Test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	- 25V <sup>(1)</sup>	- 50V <sup>(1)</sup>	- 75V <sup>(1)</sup>	- 100V <sup>(1)</sup>	2ms, 10Ω
2	+ 25V <sup>(1)</sup>	+ 50V <sup>(1)</sup>	+ 75V <sup>(1)</sup>	+ 100V <sup>(1)</sup>	0.2ms, 10Ω
3a	- 25V <sup>(1)</sup>	- 50V <sup>(1)</sup>	- 100V <sup>(1)</sup>	- 150V <sup>(1)</sup>	0.1μs, 50Ω
3b	+ 25V <sup>(1)</sup>	+ 50V <sup>(1)</sup>	+ 75V <sup>(1)</sup>	+ 100V <sup>(1)</sup>	0.1μs, 50Ω
4	- 4V <sup>(1)</sup>	- 5V <sup>(1)</sup>	- 6V <sup>(1)</sup>	- 7V <sup>(1)</sup>	100ms, 0.01Ω
5	+ 26.5V <sup>(1)</sup>	+ 46.5V <sup>(2)</sup>	+ 66.5V <sup>(2)</sup>	+ 86.5V <sup>(2)</sup>	400ms, 2Ω

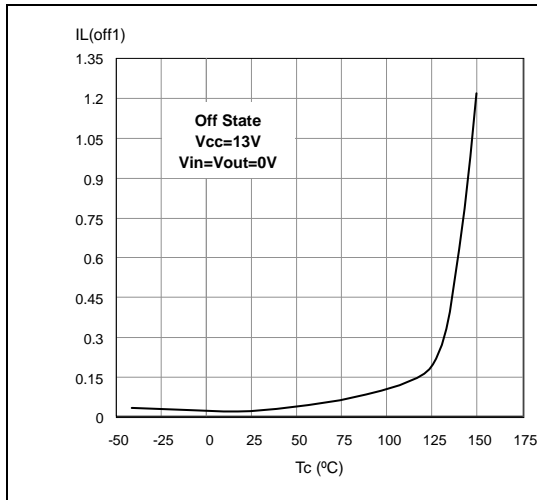
1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

Figure 6. Waveforms

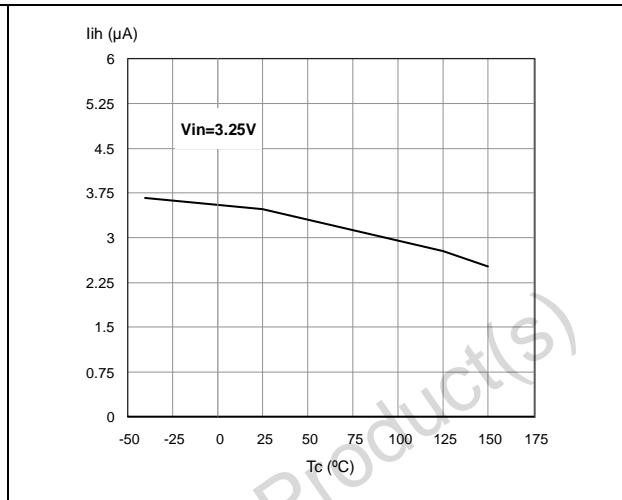


## 2.4 Electrical characteristics curves

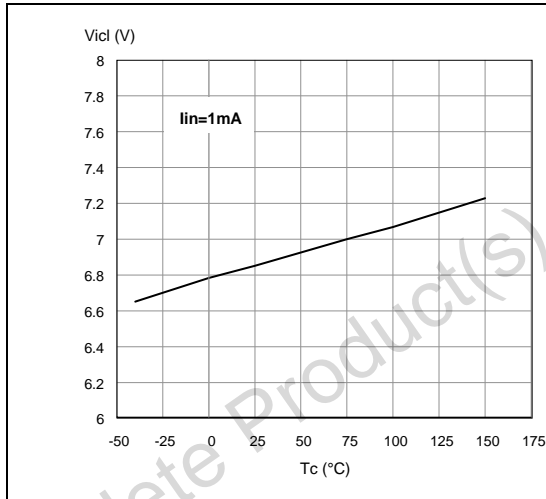
**Figure 7. Off-state output current**



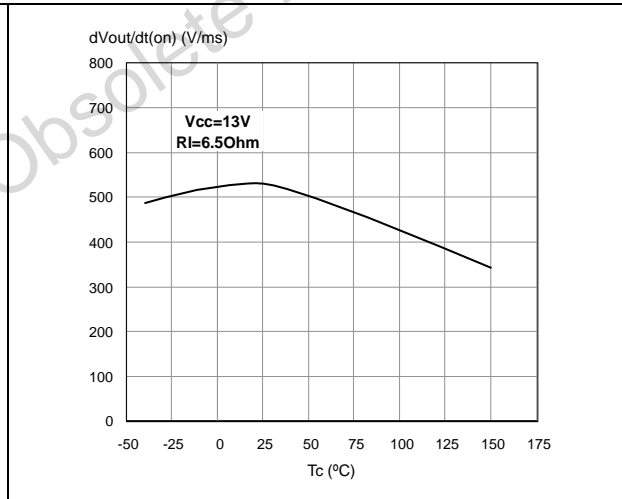
**Figure 8. High level input current**



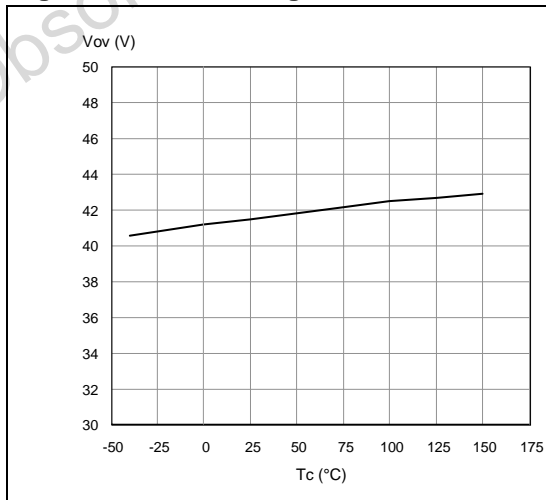
**Figure 9. Input clamp voltage**



**Figure 10. Turn-on voltage slope**



**Figure 11. Overvoltage shutdown**



**Figure 12. Turn-off voltage slope**

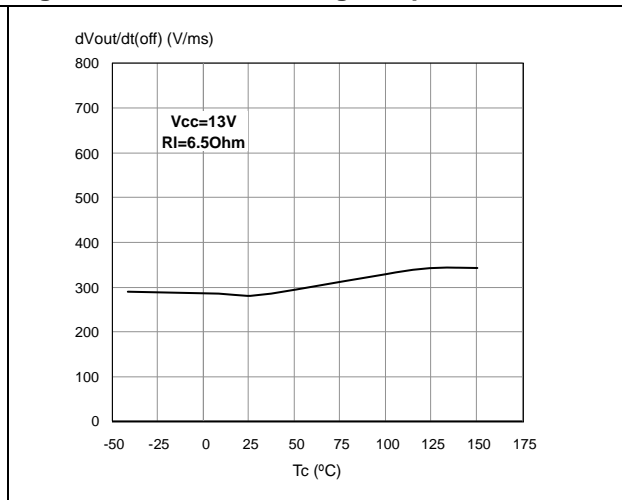


Figure 13.  $I_{LIM}$  vs  $T_{case}$

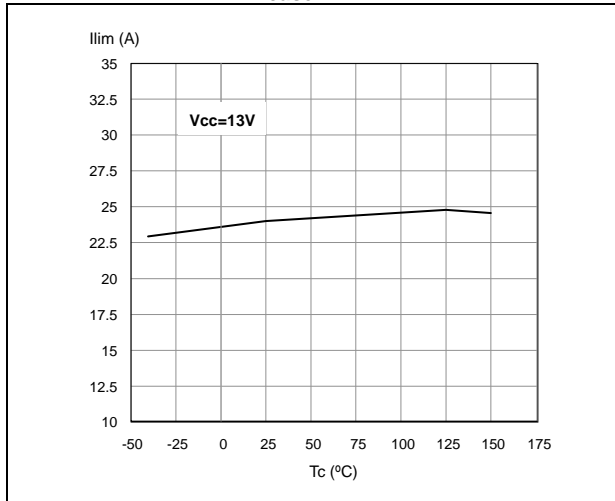


Figure 14. On-state resistance vs  $V_{CC}$

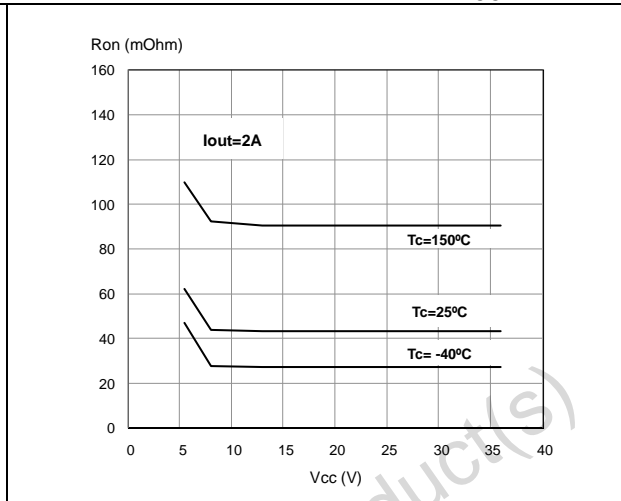


Figure 15. Input high level

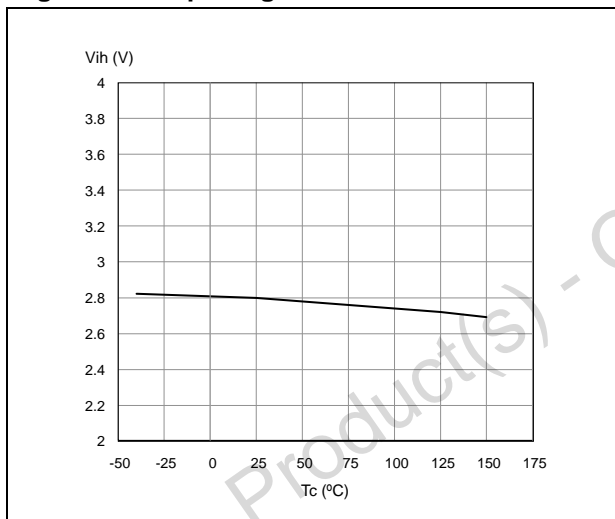


Figure 16. Input hysteresis voltage

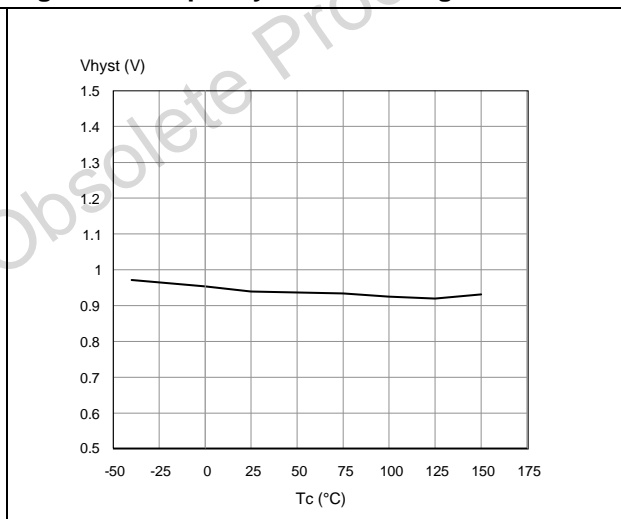


Figure 17. On-state resistance vs  $T_{case}$

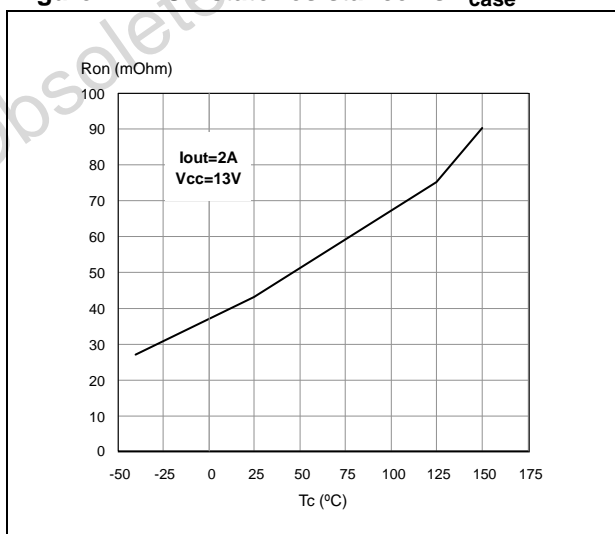


Figure 18. Input low level

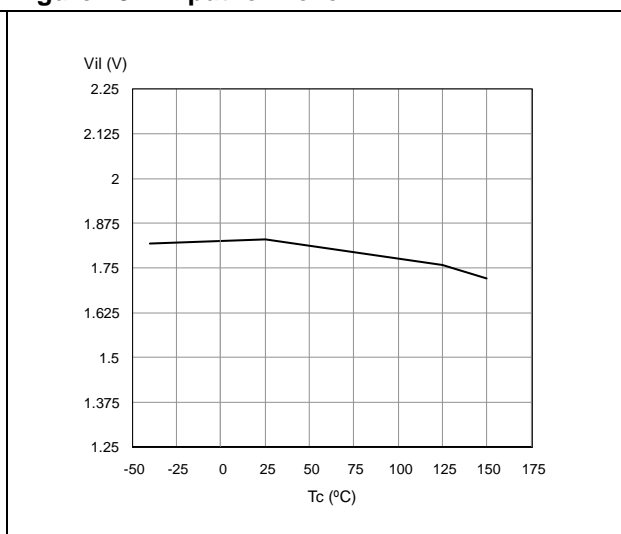


Figure 19. Status leakage current

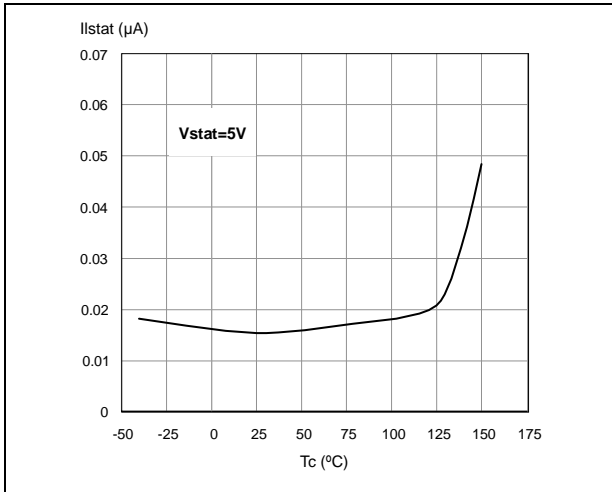


Figure 20. Status low output voltage

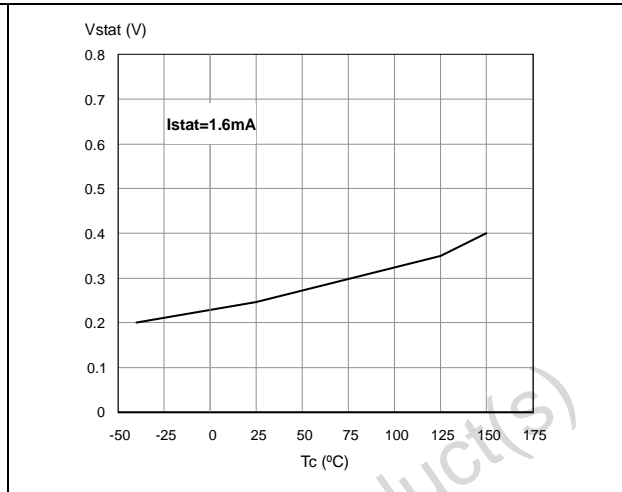


Figure 21. Status clamp voltage

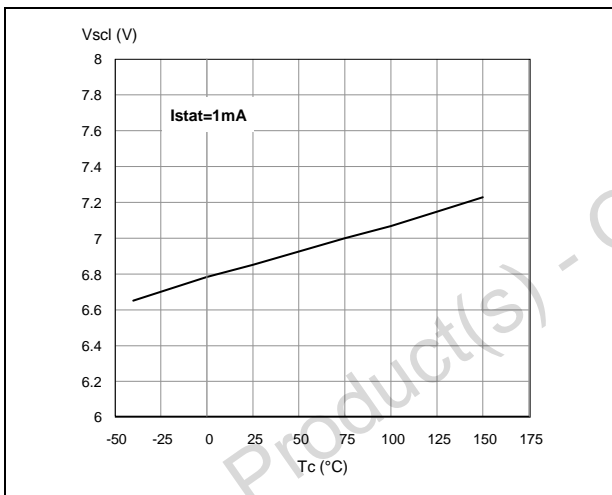


Figure 22. Open-load on-state detection threshold

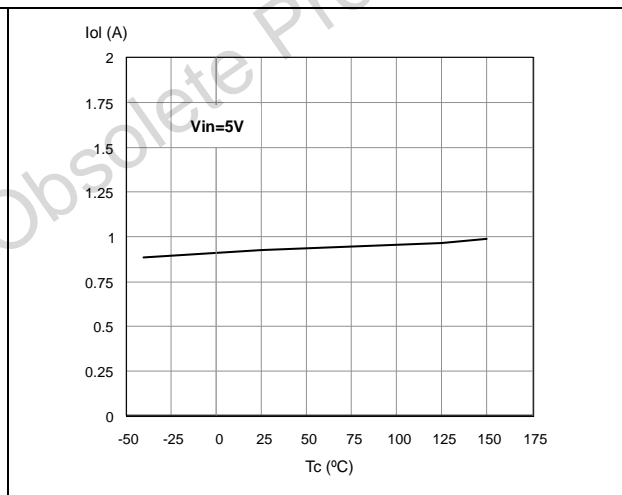
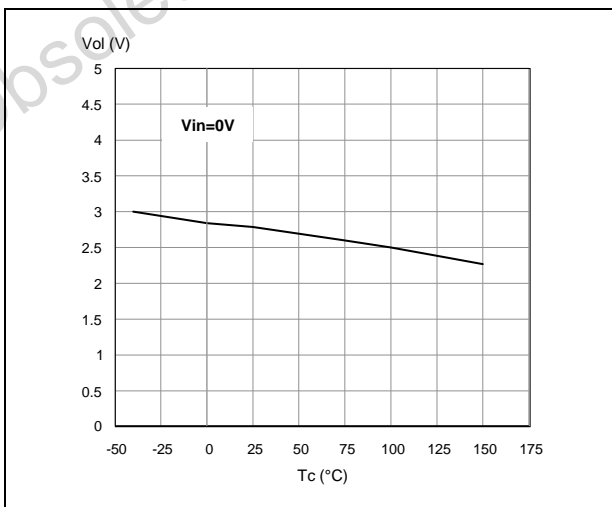
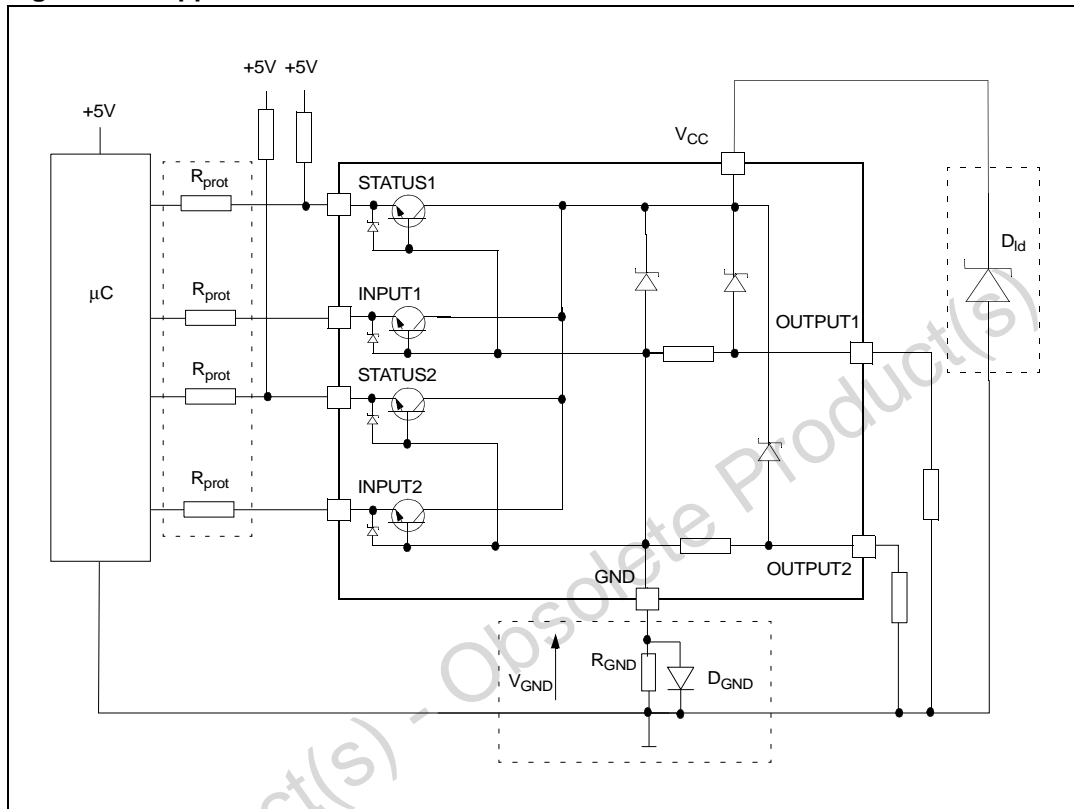


Figure 23. Open-load off-state voltage detection threshold



### 3 Application information

Figure 24. Application schematic



#### 3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

##### 3.1.1 Solution 1: a resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following show how to dimension the R<sub>GND</sub> resistor:

1.  $R_{GND} \leq 600 \text{ mV} / 2 (I_{S(on)max})$
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where - I<sub>GND</sub> is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R<sub>GND</sub> (when V<sub>CC</sub> < 0 during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where I<sub>S(on)max</sub> becomes the sum of the maximum on-state currents of the different devices.



Please note that, if the microprocessor ground is not shared by the device ground, then the  $R_{GND}$  produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same  $R_{GND}$ .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND} = 1 \text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produces a shift ( $\approx 600 \text{ mV}$ ) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift not varies if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

## 3.2 Load dump protection

$D_{ld}$  is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  maximum DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than those shown in the ISO T/R 7637/1 table.

## 3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the microcontroller I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

### Example

For the following conditions:

$$V_{CCpeak} = -100 \text{ V}$$

$$I_{latchup} \geq 20 \text{ mA}$$

$$V_{OH\mu C} \geq 4.5 \text{ V}$$

$$5 \text{ k}\Omega \leq R_{prot} \leq 65 \text{ k}\Omega.$$

Recommended values are:

$$R_{prot} = 10 \text{ k}\Omega$$

### 3.4 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor ( $R_{PU}$ ) connected between OUTPUT pin and a positive supply voltage ( $V_{PU}$ ) like the +5 V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

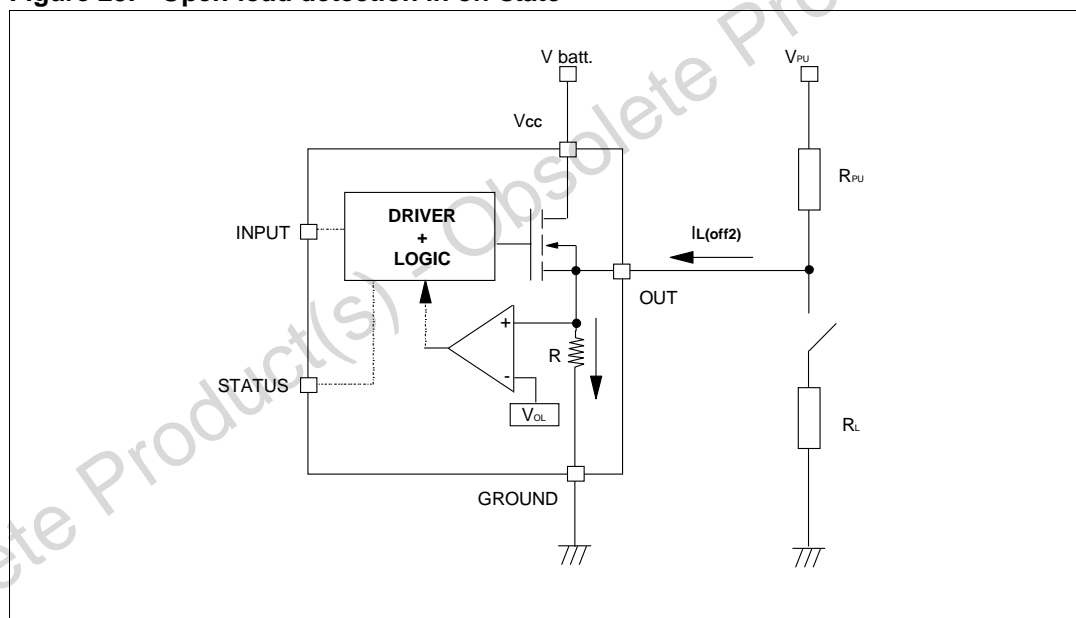
1) no false open-load indication when load is connected: in this case we have to avoid  $V_{OUT}$  to be higher than  $V_{OLmin}$ ; this results in the following condition

$$V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{OLmin}.$$

2) no misdetection when load is disconnected: in this case the  $V_{OUT}$  has to be higher than  $V_{OLmax}$ ; this results in the following condition  $R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}$ .

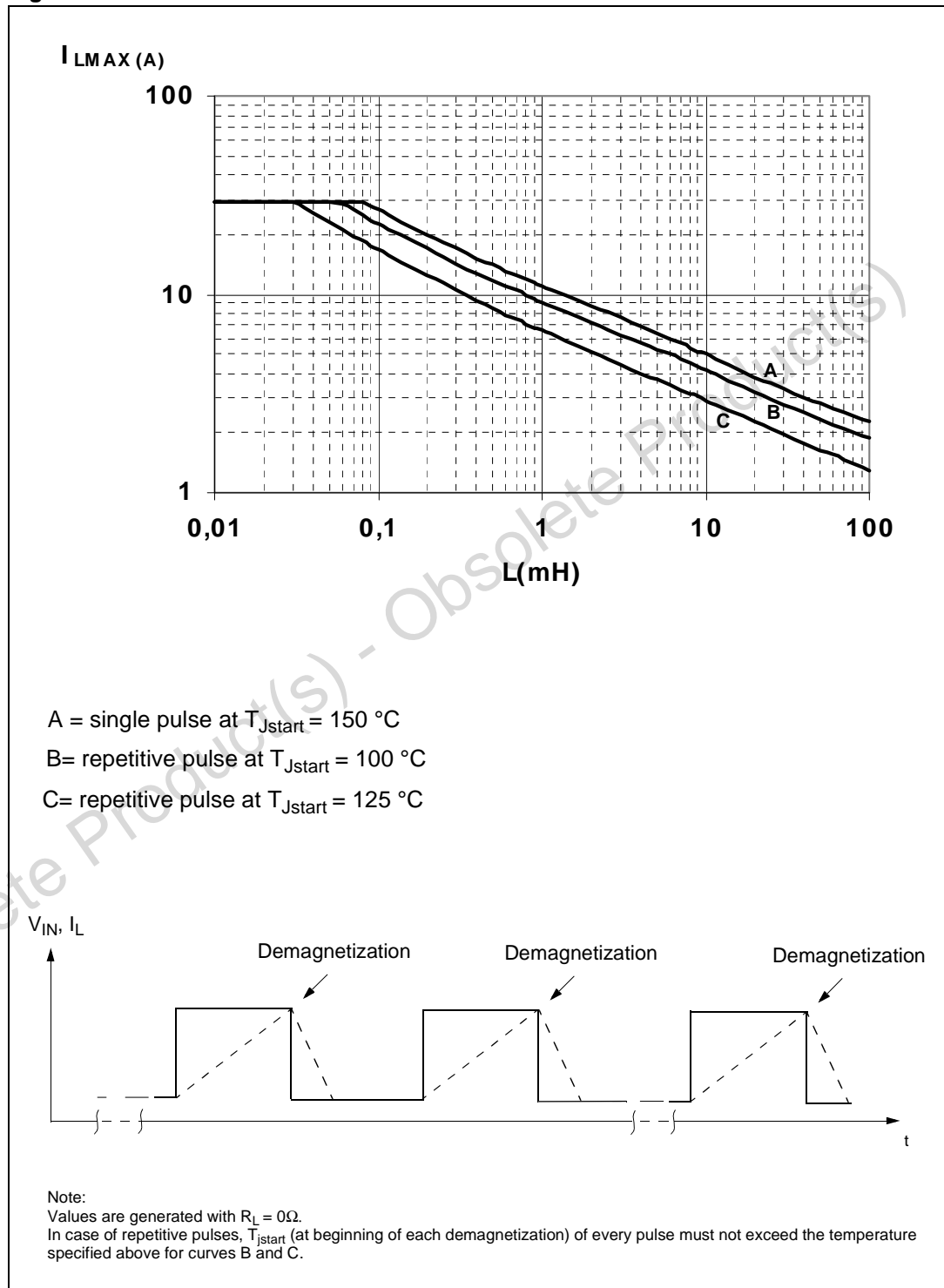
Because  $I_{s(OFF)}$  may significantly increase if  $V_{out}$  is pulled high (up to several mA), the pull-up resistor  $R_{PU}$  should be connected to a supply that is switched OFF when the module is in standby.

Figure 25. Open-load detection in off-state



### 3.5 Maximum demagnetization energy ( $V_{CC} = 13.5\text{ V}$ )

Figure 26. Maximum turn-off current versus load inductance



## 4 Package and PCB thermal data

### 4.1 PowerSO-10 thermal data

Figure 27. PowerSO-10 PC board

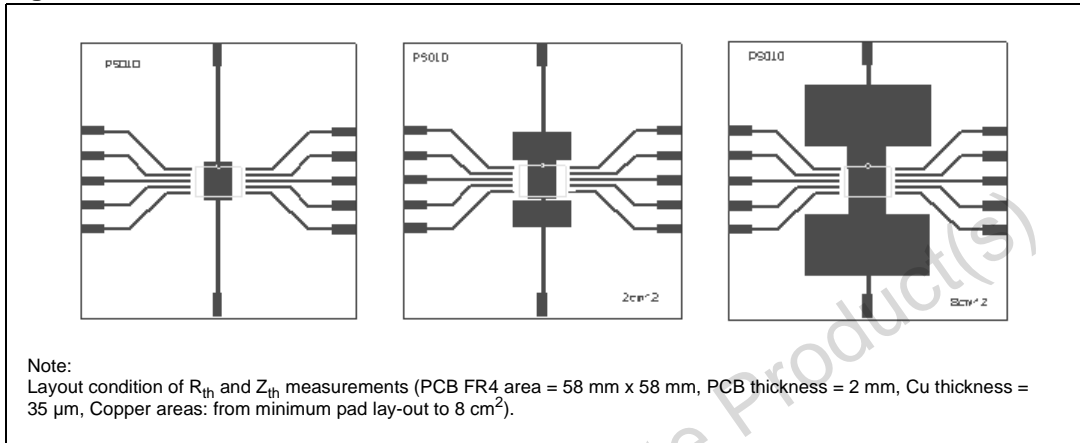


Figure 28.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

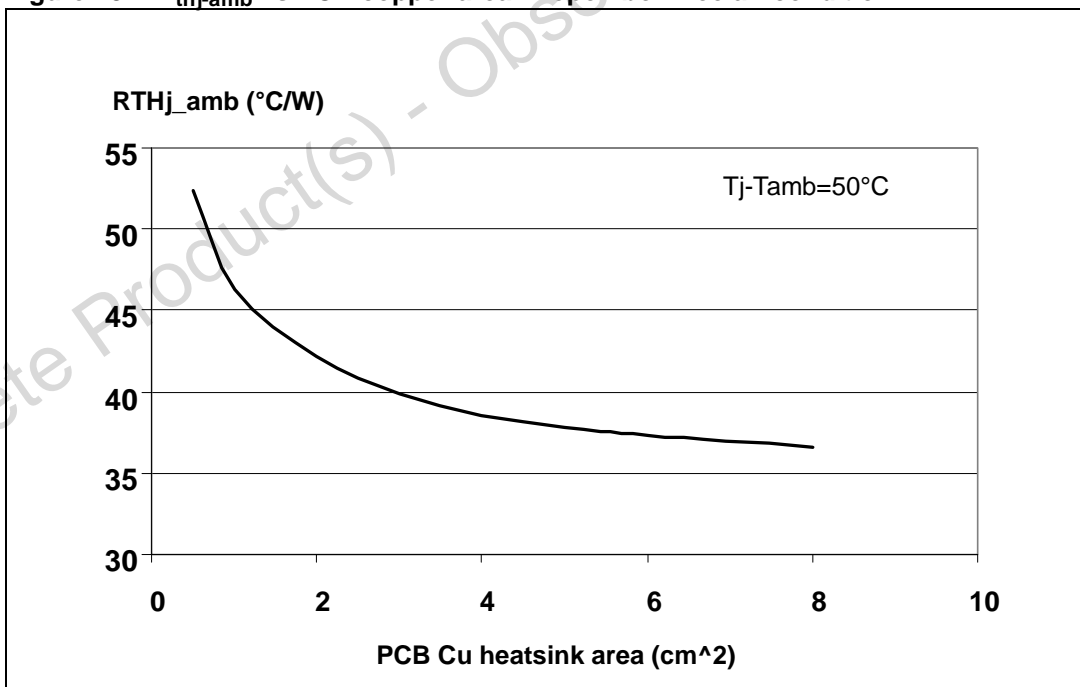
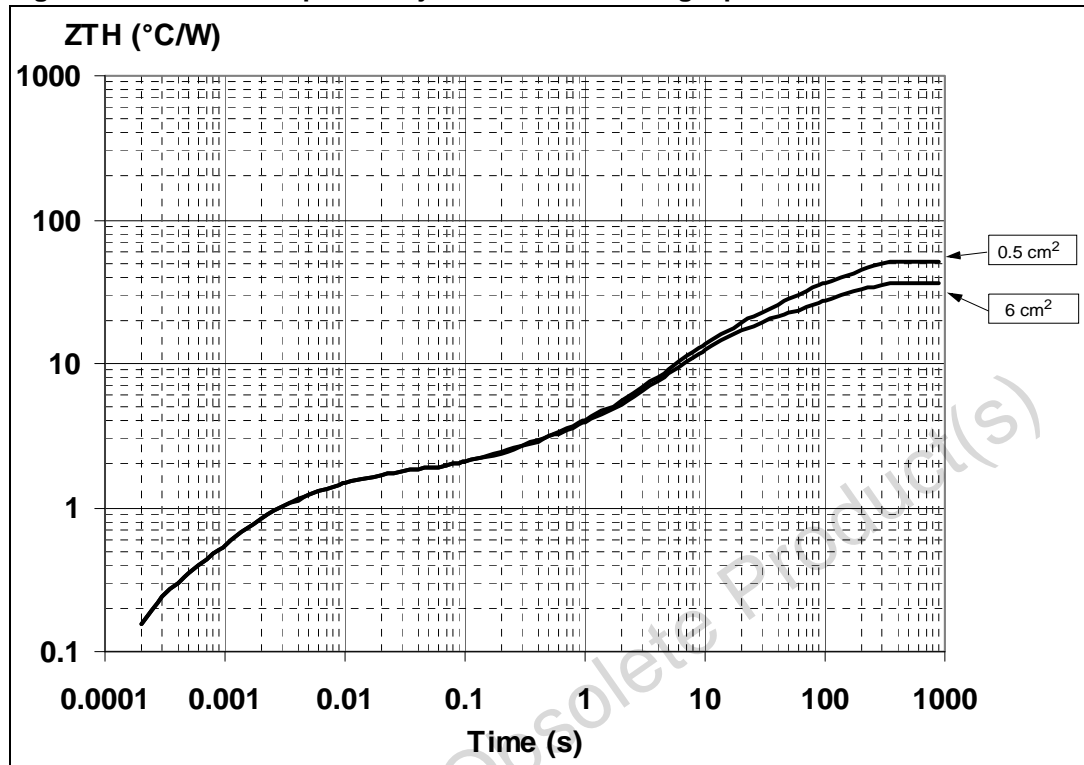


Figure 29. Thermal impedance junction ambient single pulse



Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 30. Thermal fitting model of a double channel HSD in PowerSO-10

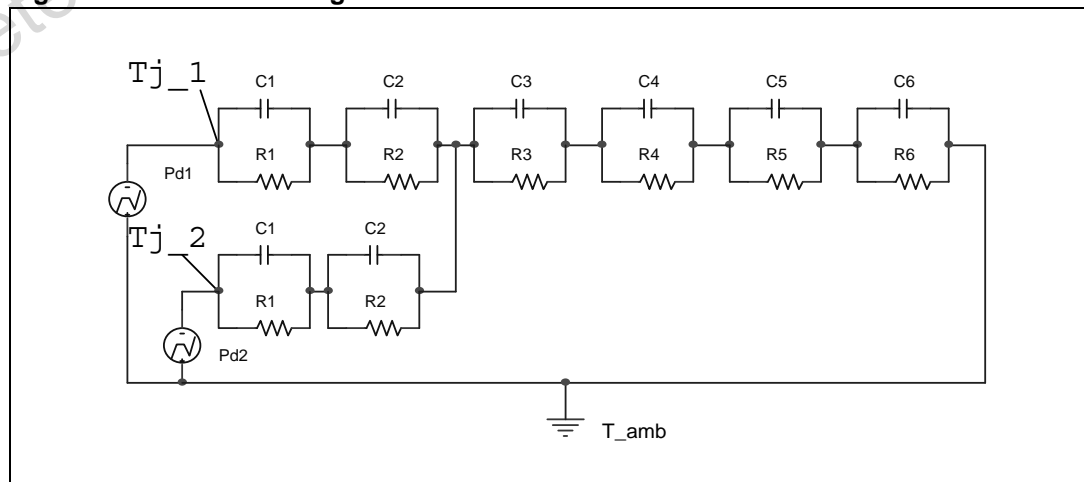


Table 14. Thermal parameters

Area / island (cm <sup>2</sup> )	Footprint	6
R1 (°C/W)	0.15	
R2 (°C/W)	0.8	
R3 (°C/W)	0.7	
R4 (°C/W)	0.8	
R5 (°C/W)	12	
R6 (°C/W)	37	22
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	2.1E-03	
C3 (W.s/°C)	0.013	
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.75	
C6 (W.s/°C)	3	5

## 5 Package and packing information

### 5.1 ECOPACK<sup>®</sup> packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 5.2 PowerSO-10 mechanical data

Figure 31. PowerSO-10 package dimensions

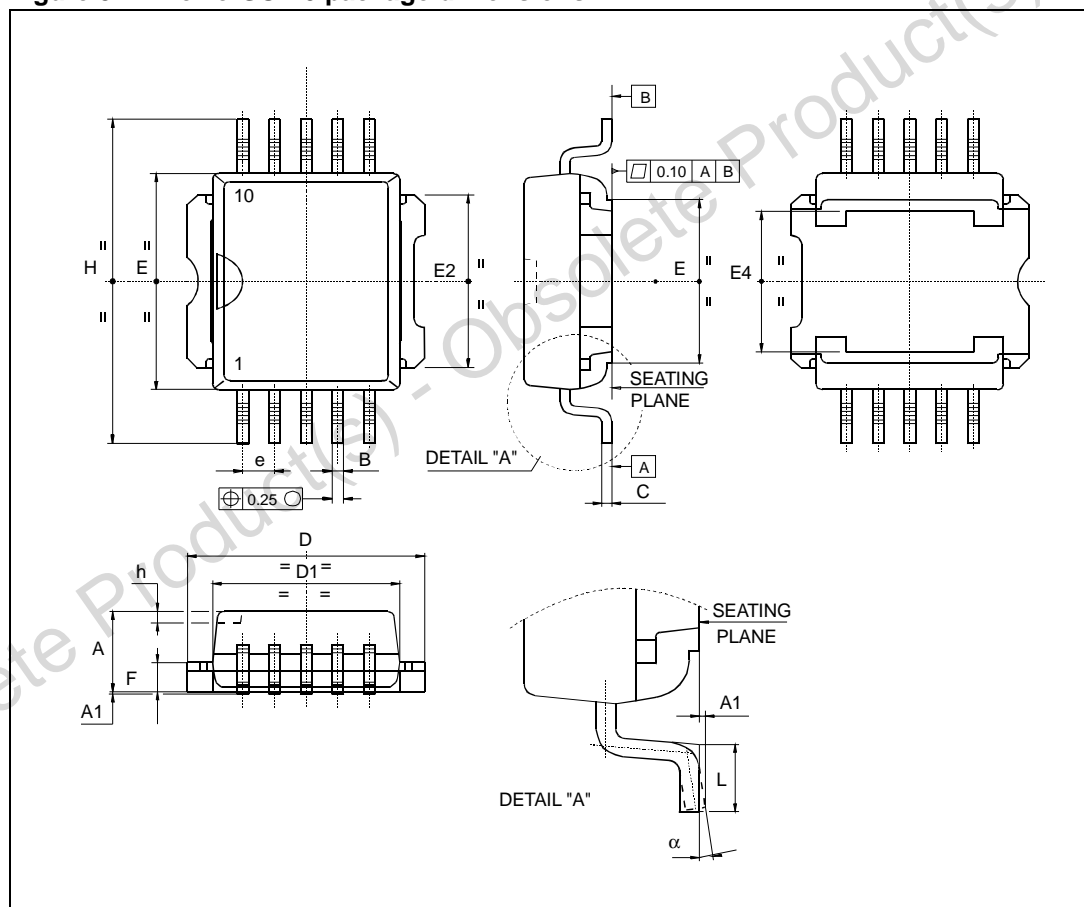


Table 15. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	3.35		3.65
A <sup>(1)</sup>	3.4		3.6
A1	0		0.10
B	0.40		0.60
B <sup>(1)</sup>	0.37		0.53
C	0.35		0.55
C <sup>(1)</sup>	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 <sup>(1)</sup>	7.30		7.50
E4	5.90		6.10
E4 <sup>(1)</sup>	5.90		6.30
e		1.27	
F	1.25		1.35
F <sup>(1)</sup>	1.20		1.40
H	13.80		14.40
H <sup>(1)</sup>	13.85		14.35
h		0.50	
L	1.20		1.80
L <sup>(1)</sup>	0.80		1.10
$\alpha$	0°		8°
$\alpha$ <sup>(1)</sup>	2°		8°

1. Muar only POA P013P.



### 5.3 PowerSO-10 packing information

Figure 32. PowerSO-10 suggested pad layout      Figure 33. PowerSO-10 tube shipment (no suffix)

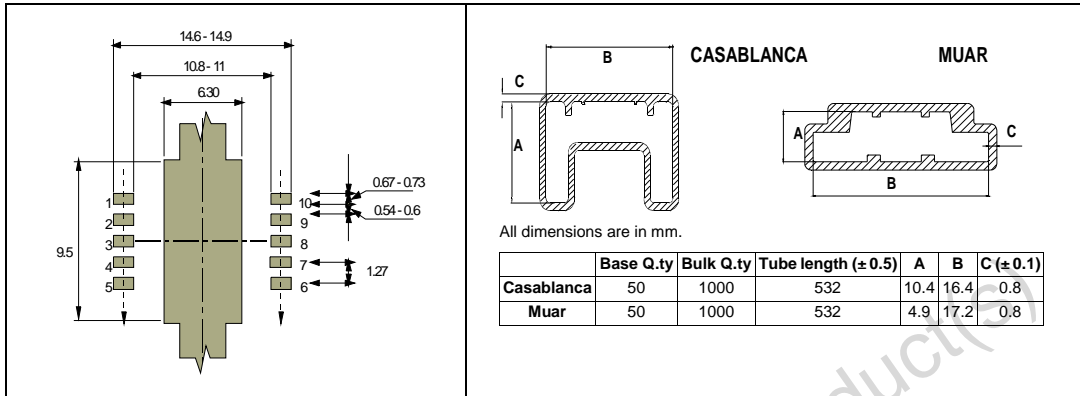
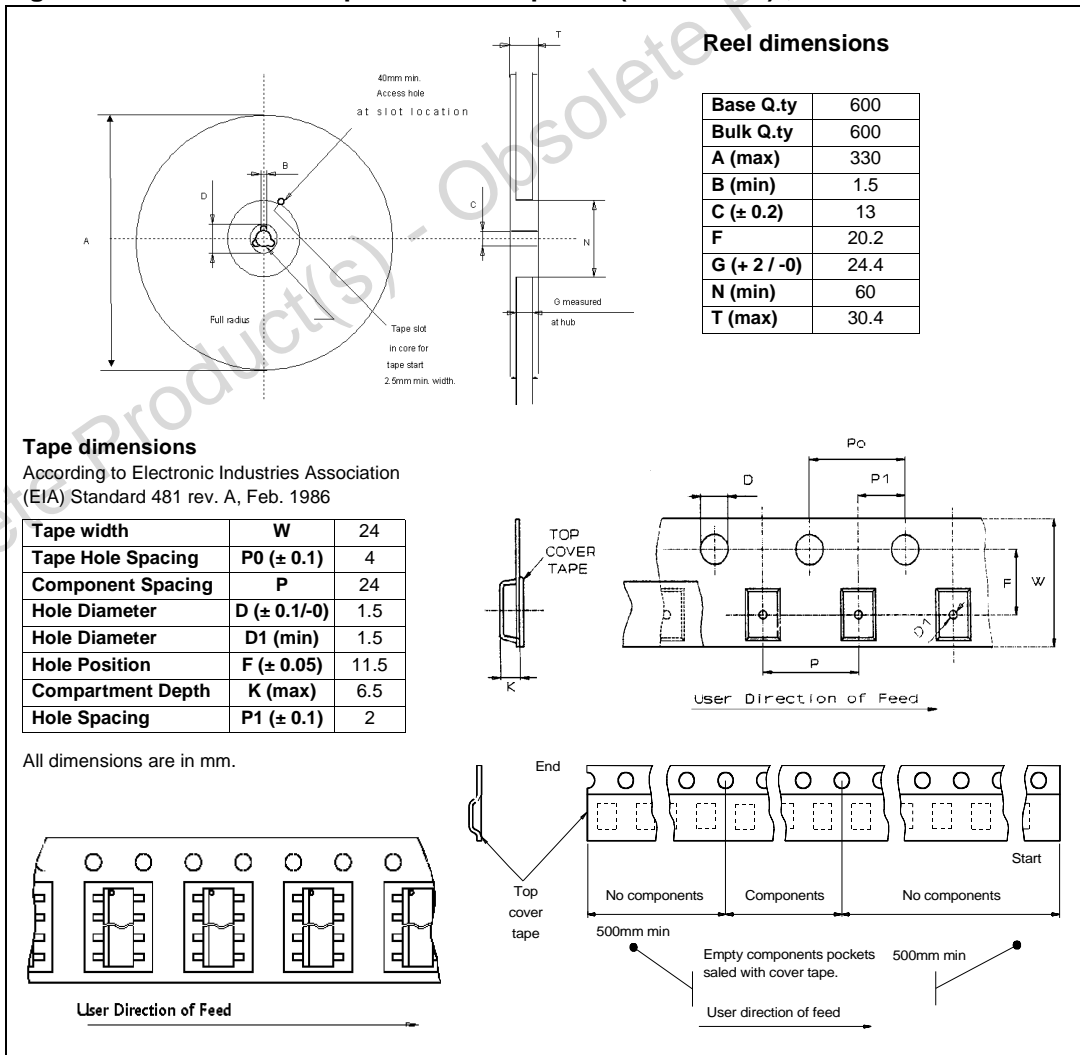


Figure 34. PowerSO-10 tape and reel shipment (suffix “TR”)



## 6 Revision history

**Table 16. Document revision history**

Date	Revision	Changes
09-Sep-2004	1	Initial release.
03-Mar-2008	2	Current and voltage convention update (page 2). Configuration diagram (top view) & suggested connections for unused and n.c. pins insertion (page 2). 6 cm <sup>2</sup> Cu condition insertion in thermal data table (page 3). V <sub>CC</sub> - output diode section update (page 4). Protections note insertion (page 4). Revision history table insertion (page 18). Disclaimers update (page 19).
09-Dec-2008	3	Document reformatted and restructured. Added contents, list of tables and figures. Added <i>ECOPACK</i> <sup>®</sup> packages information.
08-Oct-2010	4	Updated <i>Figure 5: Switching time waveforms</i> .
19-Sep-2013	5	Updated Disclaimer.

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