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NVMFS6H818N

[MOSFET](#) – Power, Single N-Channel
80 V, 3.7 mΩ, 123 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS6H818NWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

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$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	3.7 mΩ @ 10 V	123 A

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	80	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{θJC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	123	A
		T_C = 100°C		87	
Power Dissipation $R_{θJC}$ (Note 1)		T_C = 25°C	P_D	136	W
		T_C = 100°C		68	
Continuous Drain Current $R_{θJA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	20	A
		T_A = 100°C		14	
Power Dissipation $R_{θJA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.8	W
		T_A = 100°C		1.9	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	900	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to + 175	°C
Source Current (Body Diode)			I_S	113	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 9.3 A)			E_{AS}	731	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

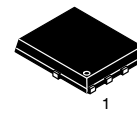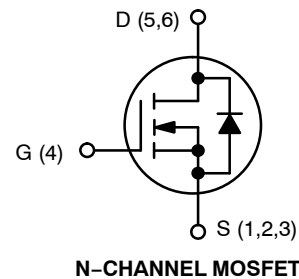| Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State	$R_{θJC}$	1.1	°C/W
Junction−to−Ambient – Steady State (Note 2)	$R_{θJA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

D (5,6)

G (4)

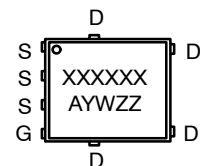S (1,2,3)

N−CHANNEL MOSFET

DFN5 (SO−8FL) CASE 488AA STYLE 1

MARKING DIAGRAM

D
S
S
S
G
D
D
D

XXXXXX
AYWZZ

XXXXXX = 6H818N
(NVMFS6H818N) or
818NWF
(NVMFS6H818NWF)
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				39		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 190 μA		2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				7.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A		3.1	3.7	mΩ
Forward Transconductance	g_{FS}	V_{DS} =15 V, I_D = 50 A			170		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 40 V			3100		pF
Output Capacitance	C_{OSS}				440		
Reverse Transfer Capacitance	C_{RSS}				20		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 40 V; I_D = 50 A			46		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 40 V; I_D = 50 A			9.0		
Gate−to−Source Charge	Q_{GS}				15		
Gate−to−Drain Charge	Q_{GD}				8.0		
Plateau Voltage	V_{GP}				5.0		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 64 V, I_D = 50 A, R_G = 2.5 Ω			22		ns
Rise Time	t_r				98		
Turn−Off Delay Time	$t_{d(OFF)}$				49		
Fall Time	t_f				21		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 20 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			63		ns
Charge Time	t_a				31		
Discharge Time	t_b				32		
Reverse Recovery Charge	Q_{RR}				55		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

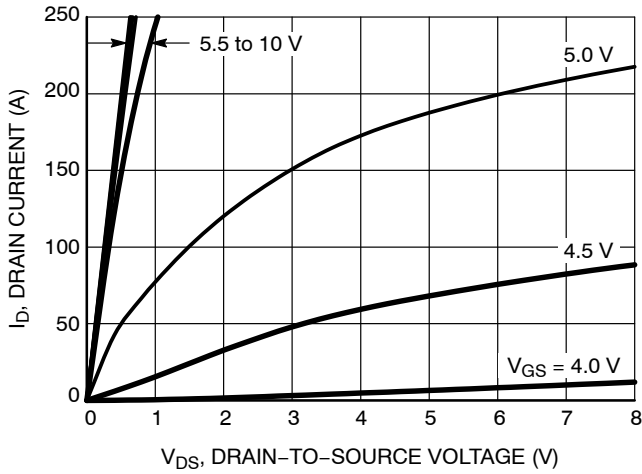## TYPICAL CHARACTERISTICS

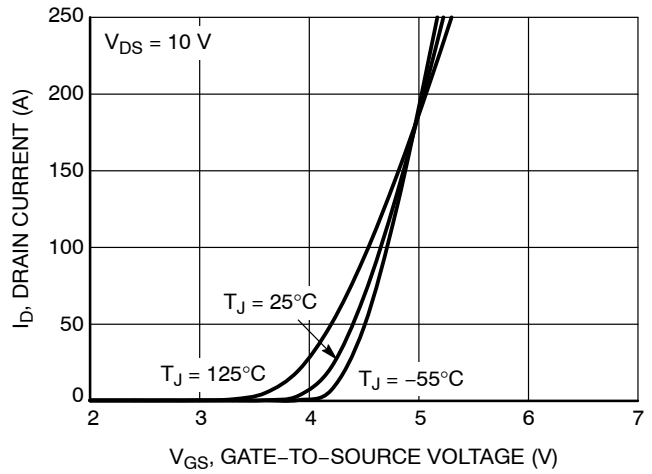Figure 1. On–Region Characteristics
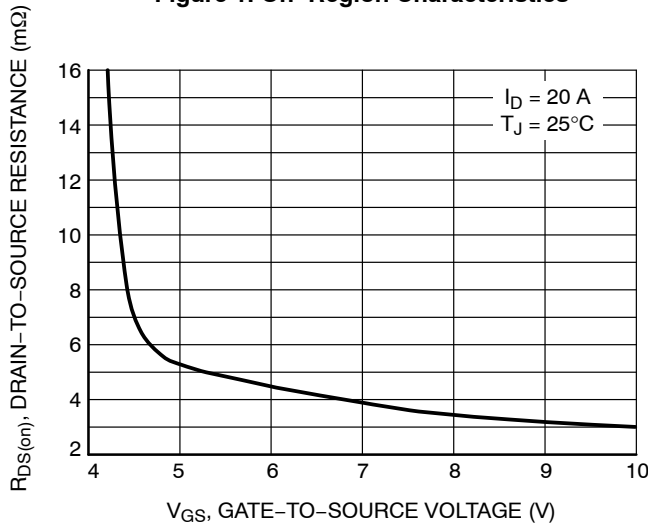

Figure 2. Transfer Characteristics

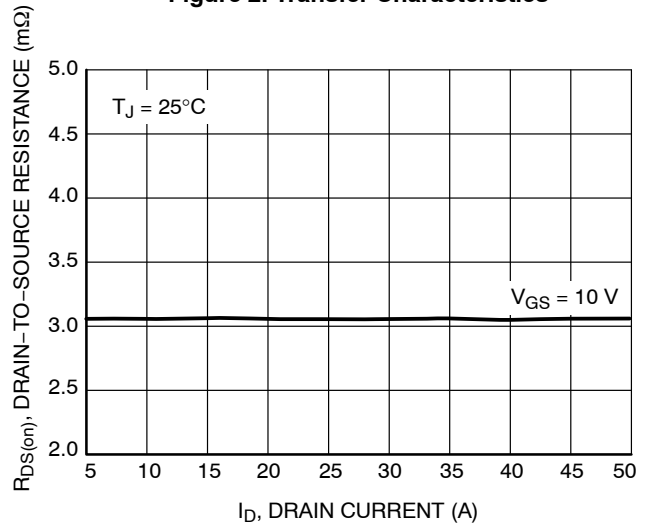Figure 3. On–Resistance vs. Gate–to–Source Voltage

Figure 4. On–Resistance vs. Drain Current and Gate Voltage
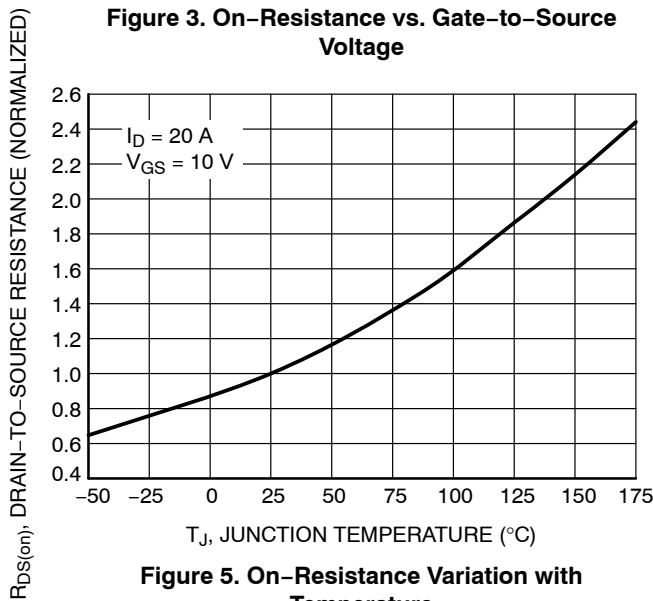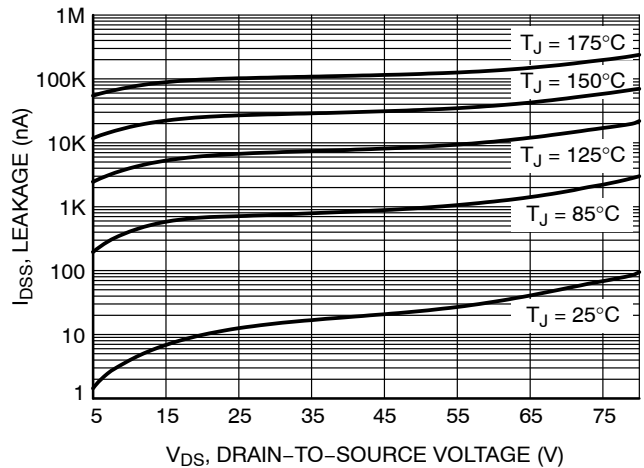

Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain–to–Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

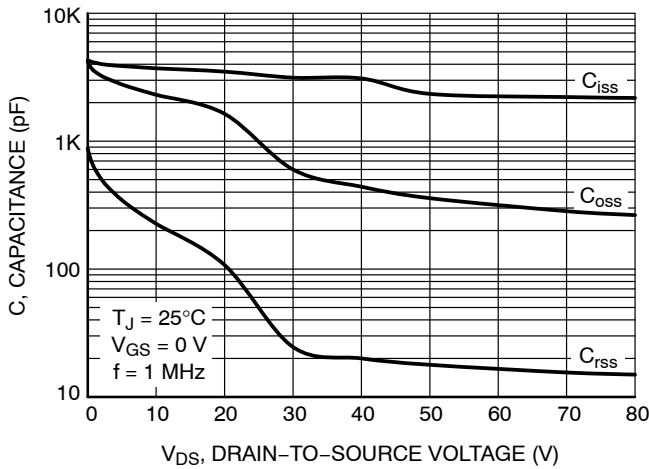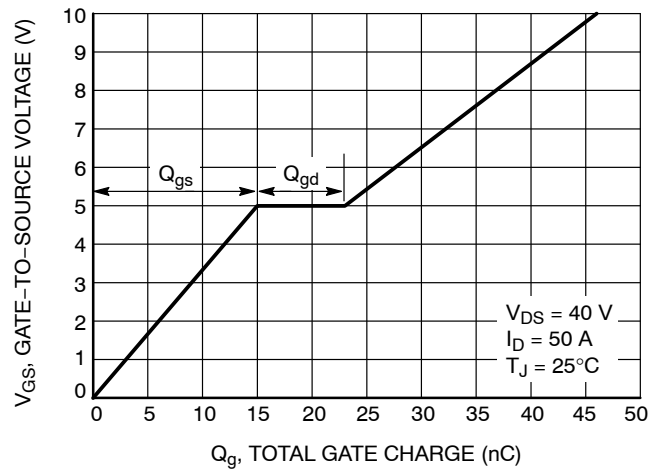Figure 7. Capacitance Variation
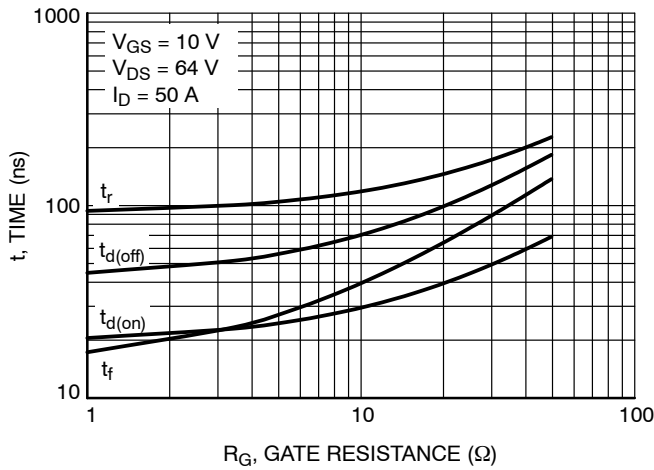

Figure 8. Gate−to−Source vs. Total Charge
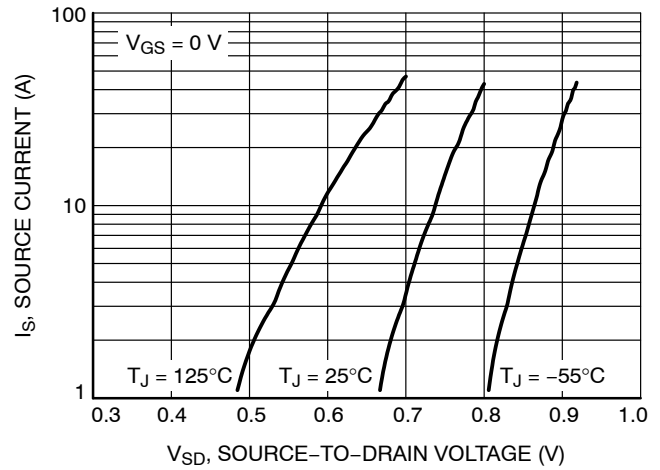

Figure 9. Resistive Switching Time Variation
vs. Gate Resistance

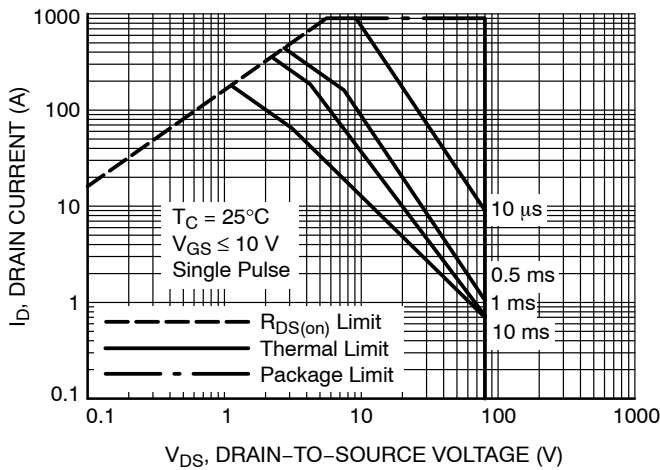Figure 10. Diode Forward Voltage vs. Current

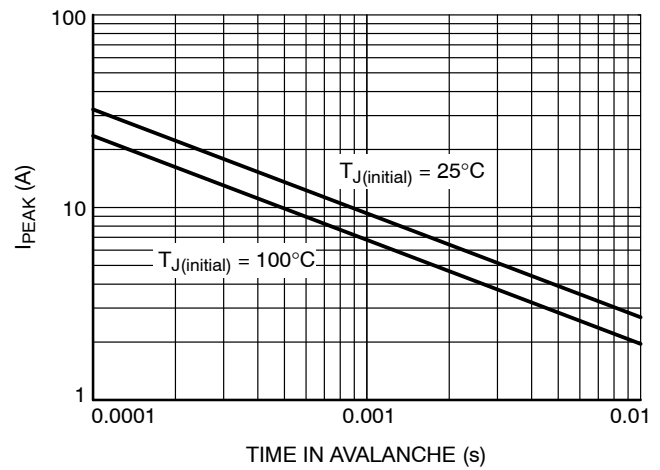Figure 11. Maximum Rated Forward Biased
Safe Operating Area

Figure 12. Maximum Drain Current vs. Time in
Avalanche

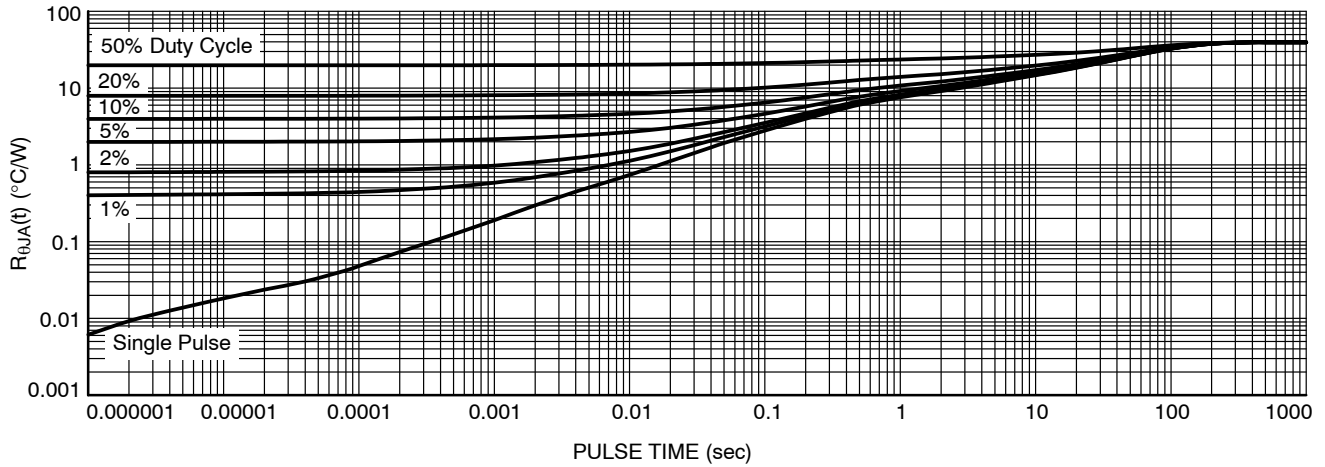# NVMFS6H818N

TYPICAL CHARACTERISTICS

Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NVMFS6H818NT1G	6H818N	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS6H818NWFT1G	818NWF	DFN5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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SCALE 2:1

DFN5 5x6, 1.27P
(SO–8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

2 X
⌒ 0.20 C

A

B

2 X
⌒ 0.20 C

D

D1

E1

E

2

2

4 X
θ

c

A1

DETAIL A

SEATING PLANE
C

1 2 3 4

TOP VIEW

⫽ 0.10 C

⌒ 0.10 C

A

SIDE VIEW

DETAIL A

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °

GENERIC
MARKING DIAGRAM*

1

XXXXXX
AYWZZ

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

8X b
⊕ 0.10 C A B
0.05 c

e/2
e

L

1 4

K

E2

PIN 5
(EXPOSED PAD)

L1 M

G

D2

BOTTOM VIEW

RECOMMENDED
SOLDERING FOOTPRINT*

2X
0.495

4.560

2X
1.530

2X
0.475

3.200

4.530

1.330

2X
0.905

1

0.965

4X
1.000

4X 0.750

1.270
PITCH

DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON14036D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	DFN5 5x6, 1.27P (SO–8FL)		PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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