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MTB2P50E

Preferred Device

Power MOSFET 2 Amps, 500 Volts

P−Channel D²PAK

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage−blocking capability without degrading performance over time. In addition, this Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain−to−source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

Features

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source−to−Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Pb−Free Package is Available

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	500	Vdc
Drain−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate−Source Voltage − Continuous Non−Repetitive (t_p ≤ 10 ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current − Continuous − Continuous @ 100°C − Single Pulse (t_p ≤ 10 μs)	I_D I_D I_{DM}	2.0 1.6 6.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	75 0.6 2.5	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 4.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	80	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient − Junction−to−Ambient (Note 1)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 sec	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using the minimum recommended pad size.

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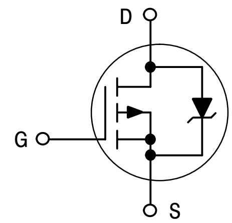
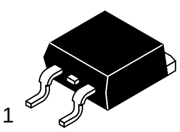
2 AMPERES, 500 VOLTS
$R_{DS(on)}$ = 6 Ω

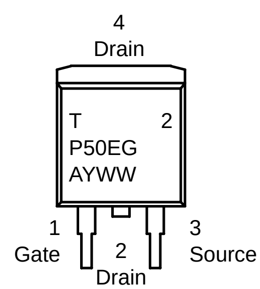
P−Channel





D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



T2P50E = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
MTB2P50ET4	D²PAK	800/Tape & Reel
MTB2P50ET4G	D²PAK (Pb−Free)	800/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

June, 2006 − Rev. 4

Publication Order Number:
MTB2P50E/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	500	−	−	Vdc
Temperature Coefficient (Positive)		−	564	−	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}				μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		−	−	10	
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		−	−	100	
Gate−Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)	I_{GSS}	−	−	100	nAdc
ON CHARACTERISTICS (Note 2)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)		−	4.0	−	mV/°C
Static Drain−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$R_{DS(on)}$	−	4.5	6.0	Ω
Drain−Source On−Voltage (V_{GS} = 10 Vdc)	$V_{DS(on)}$				Vdc
(I_D = 2.0 Adc)		−	9.5	14.4	
(I_D = 1.0 Adc, T_J = 125°C)		−	−	12.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)	g_{FS}	1.5	2.9	−	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	845	1183	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	−	100	140	
Reverse Transfer Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{rss}	−	26	52	
SWITCHING CHARACTERISTICS (Note 3)					
Turn−On Delay Time (V_{DD} = 250 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	−	12	24	ns
Rise Time	t_r	−	14	28	
Turn−Off Delay Time	$t_{d(off)}$	−	21	42	
Fall Time	t_f	−	19	38	
Gate Charge (See Figure 8) (V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	−	19	27	nC
	Q_1	−	3.7	−	
	Q_2	−	7.9	−	
	Q_3	−	9.9	−	
SOURCE−DRAIN DIODE CHARACTERISTICS					
Forward On−Voltage (Note 2) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	−	2.3	3.5	Vdc
(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		−	1.85	−	
Reverse Recovery Time (See Figure 14) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	−	223	−	ns
	t_a	−	161	−	
	t_b	−	62	−	
Reverse Recovery Stored Charge	Q_{RR}	−	1.92	−	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)	L_D	−	4.5	−	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	−	7.5	−	nH

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

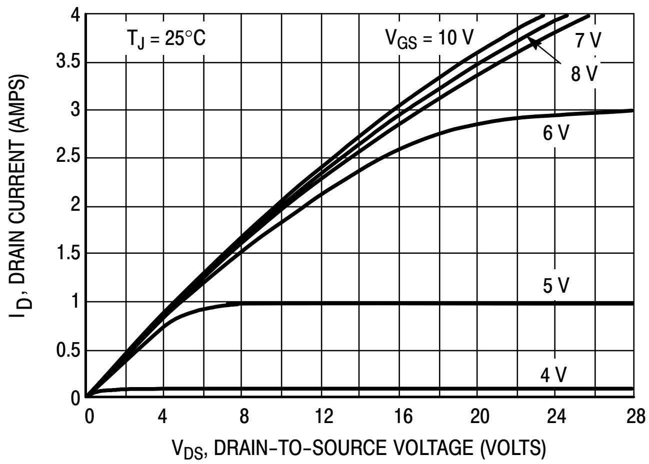


Figure 1. On−Region Characteristics

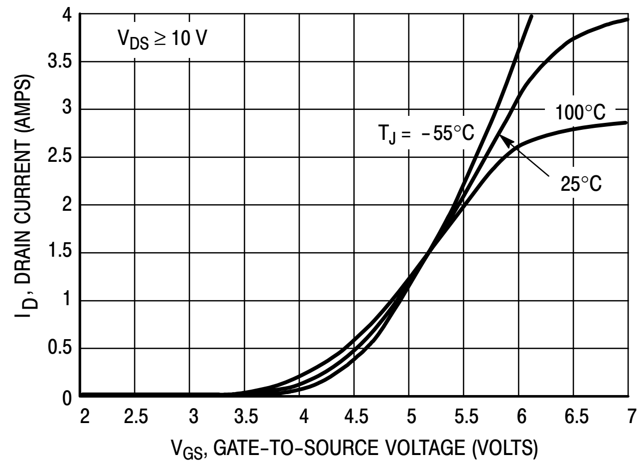


Figure 2. Transfer Characteristics

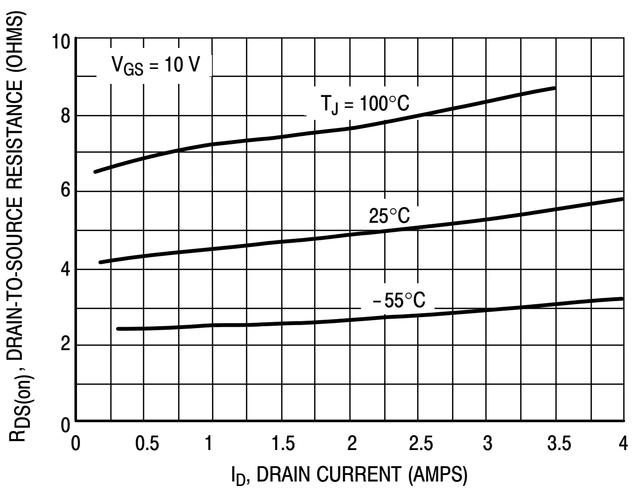


Figure 3. On−Resistance versus Drain Current and Temperature

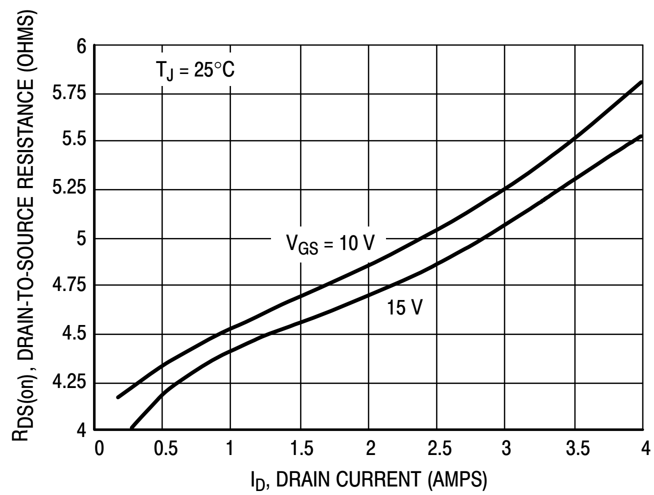


Figure 4. On−Resistance versus Drain Current and Gate Voltage

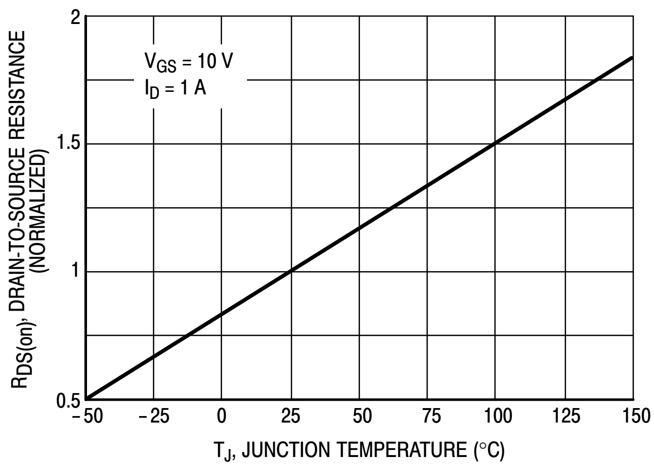


Figure 5. On−Resistance Variation with Temperature

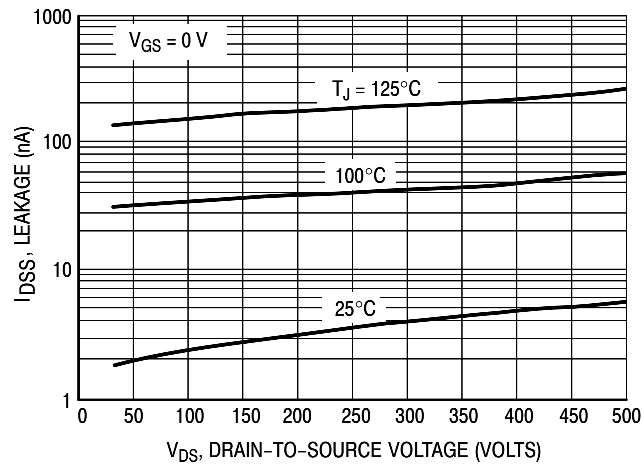


Figure 6. Drain−To−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

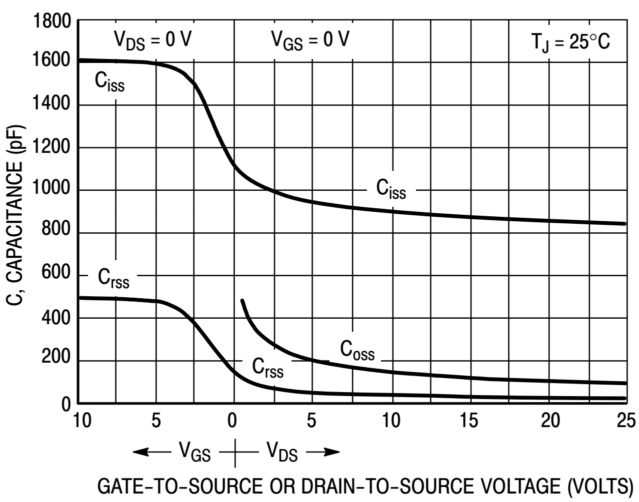


Figure 7a. Capacitance Variation

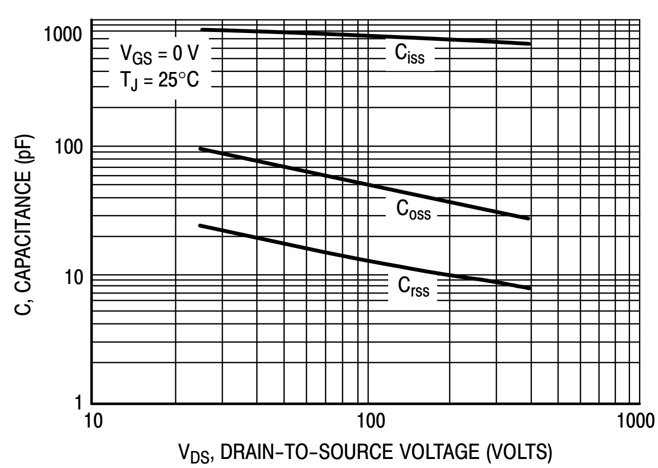


Figure 7b. High Voltage Capacitance Variation

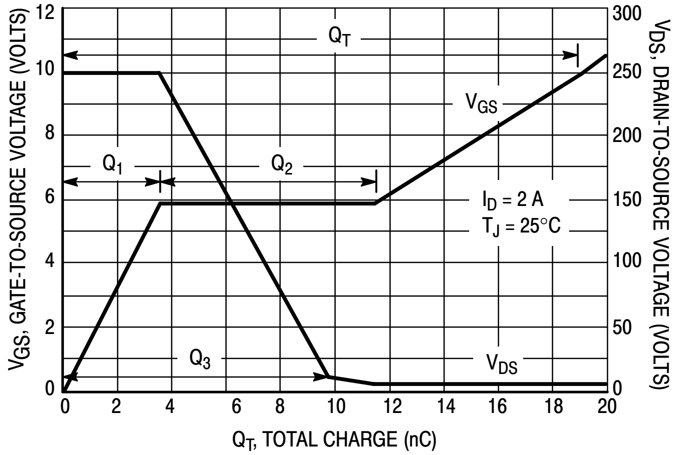


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

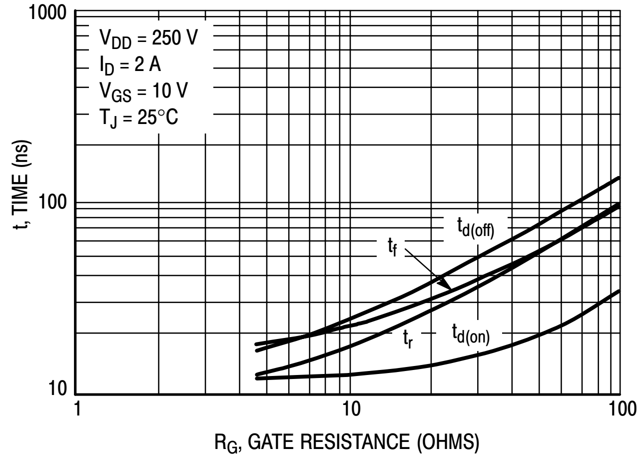


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

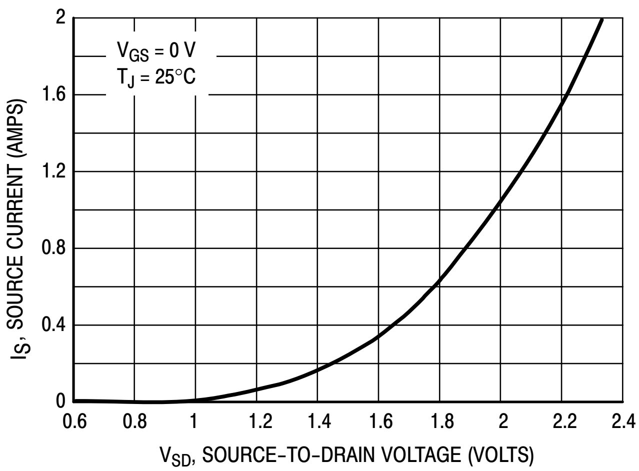


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance−General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{θJC}$).

A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

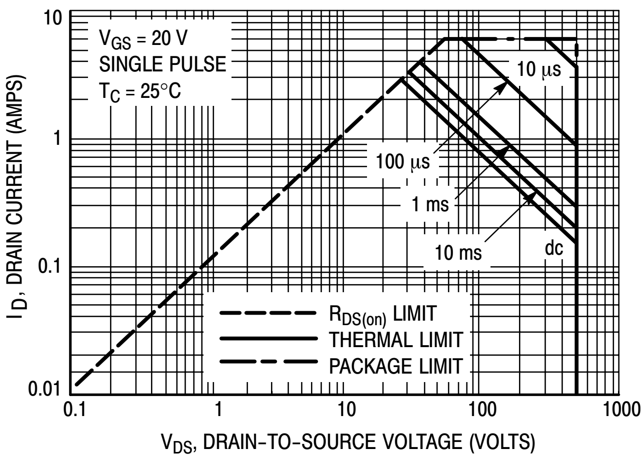


Figure 11. Maximum Rated Forward Biased Safe Operating Area

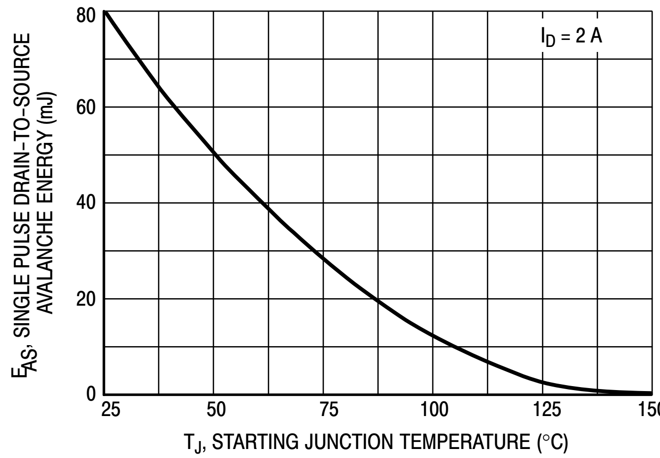


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

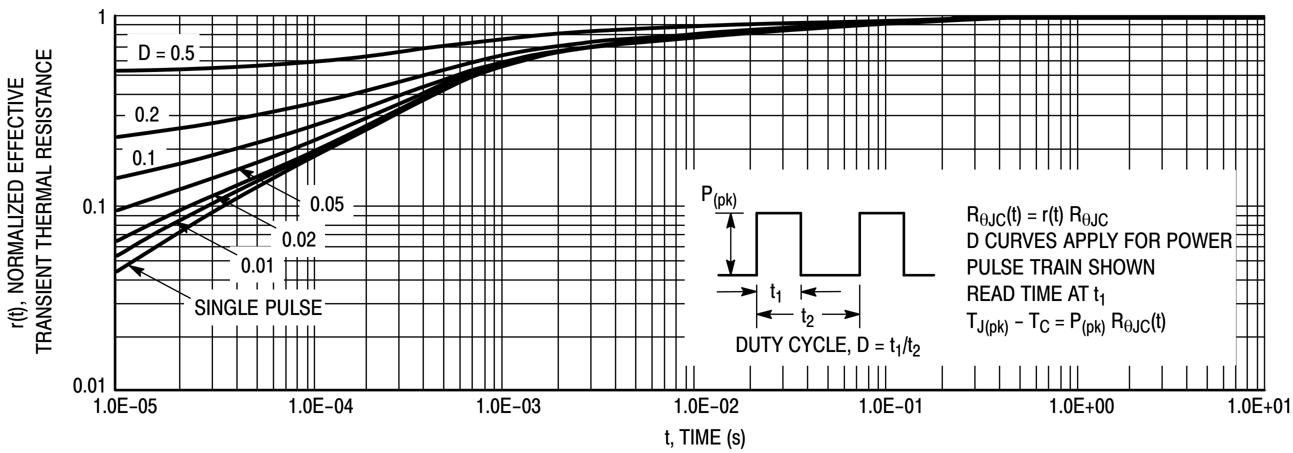


Figure 13. Thermal Response

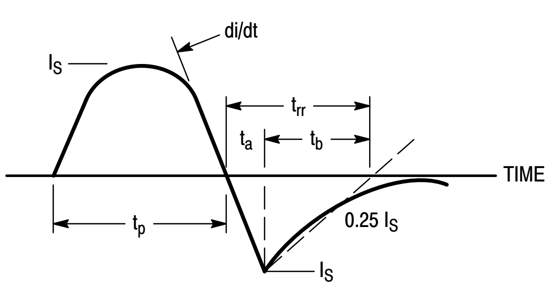


Figure 14. Diode Reverse Recovery Waveform

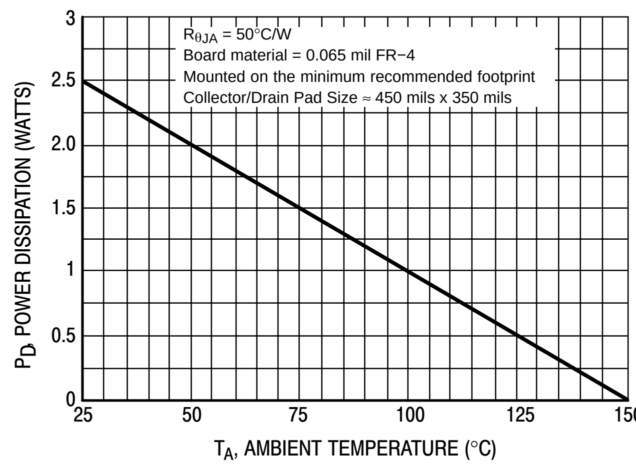
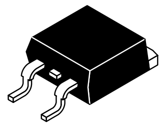


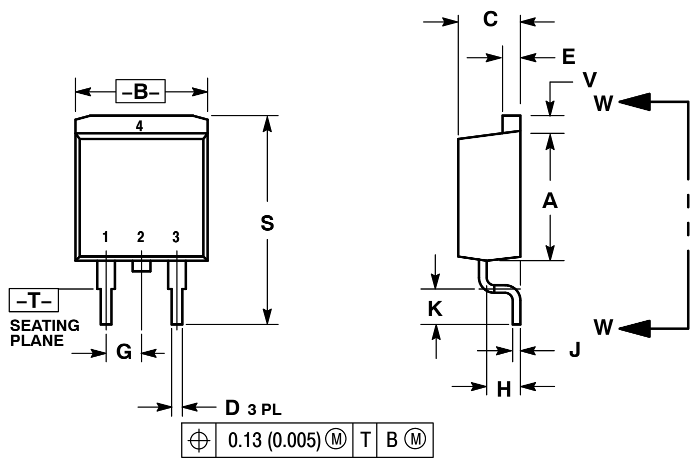
Figure 15. D2PAK Power Derating Curve



D²PAK 3
CASE 418B−04
ISSUE L

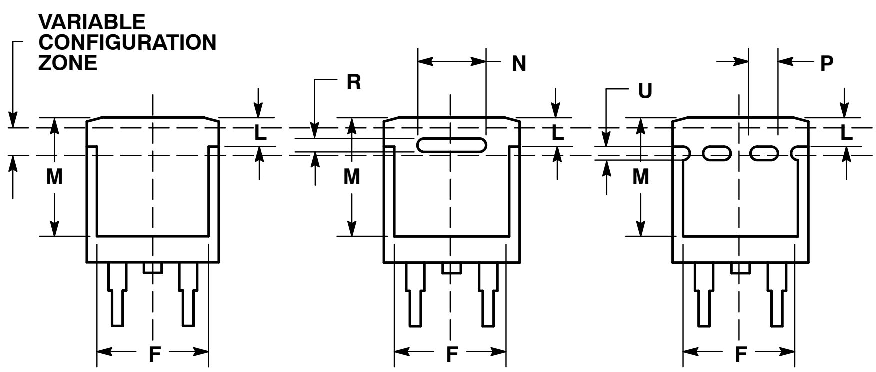
DATE 17 FEB 2015

SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



VIEW W−W 1 **VIEW W−W 2** **VIEW W−W 3**

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE

MARKING INFORMATION AND FOOTPRINT ON PAGE 2

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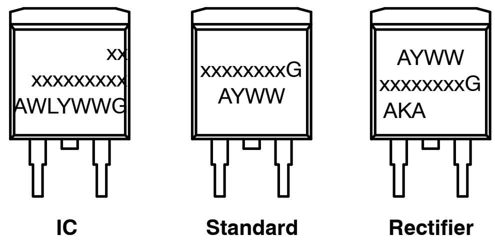
DESCRIPTION:	D²PAK 3	PAGE 1 OF 2

D²PAK 3
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

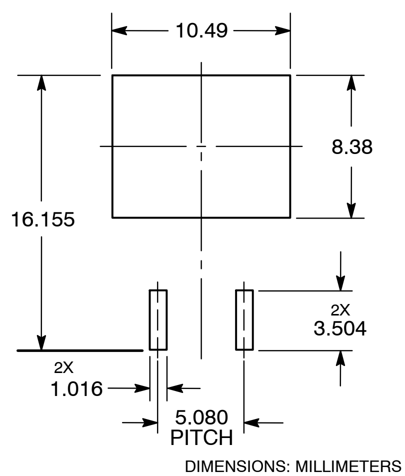
GENERIC
MARKING DIAGRAM*



xx	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package
AKA	= Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	D²PAK 3	PAGE 2 OF 2

PUBLICATION ORDERING INFORMATION

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