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ON Semiconductor®

Advanced Power MOSFET

IRFM120A

IEEE802.3af Compatible

FEATURES

- ❏ Avalanche Rugged Technology
- ❏ Rugged Gate Oxide Technology
- ❏ Lower Input Capacitance
- ❏ Improved Gate Charge
- ❏ Extended Safe Operating Area
- ❏ Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 100V
- ❏ Lower $R_{DS(ON)}$: 0.155 Ω (Typ.)

BV_{DSS} = 100 V

$R_{DS(on)}$ = 0.2 Ω

I_D = 2.3 A

SOT-223

1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	100	V
I_D	Continuous Drain Current (T_A=25℃)	2.3	A
	Continuous Drain Current (T_A=70℃)	1.84	
I_{DM}	Drain Current-Pulsed ①	18	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulsed Avalanche Energy ②	123	mJ
I_{AR}	Avalanche Current ①	2.3	A
E_{AR}	Repetitive Avalanche Energy ①	0.24	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.5	V/ns
P_D	Total Power Dissipation (T_A=25℃) *	2.4	W
	Linear Derating Factor *	0.019	W/℃
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	℃
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient *	--	52	℃/W

* When mounted on the minimum pad size recommended (PCB Mount).

Electrical Characteristics (T_A=25℃ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	100	--	--	V	V_{GS}=0V,I_D=250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	0.12	--	V/℃	I_D=250μA **See Fig 7**
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-20V
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=30V ⑥
		--	--	10		V_{DS}=100V
		--	--	100		V_{DS}=80V,T_A=125℃
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.2	Ω	V_{GS}=10V,I_D=1.15A ④
g_{fs}	Forward Transconductance	--	3.12	--	S	V_{DS}=40V,I_D=1.15A ④
C_{iss}	Input Capacitance	--	370	480	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz **See Fig 5**
C_{oss}	Output Capacitance	--	95	110		
C_{rss}	Reverse Transfer Capacitance	--	38	45		
$t_{d(on)}$	Turn-On Delay Time	--	14	40	ns	V_{DD}=50V,I_D=9.2A, R_G=18Ω **See Fig 13** ④ ⑤
t_r	Rise Time	--	14	40		
$t_{d(off)}$	Turn-Off Delay Time	--	36	90		
t_f	Fall Time	--	28	70		
Q_g	Total Gate Charge	--	16	22	nC	V_{DS}=80V,V_{GS}=10V, I_D=9.2A **See Fig 6 & Fig 12** ④ ⑤
Q_{gs}	Gate-Source Charge	--	2.7	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	7.8	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	2.3	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	18		
V_{SD}	Diode Forward Voltage ④	--	--	1.5	V	T_J=25℃,I_S=2.3A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	98	--	ns	T_J=25℃,I_F=9.2A
Q_{rr}	Reverse Recovery Charge	--	0.34	--	μC	di_F/dt=100A/μs ④

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=35mH, I_{AS}=2.3A, V_{DD}=25V, R_G=27Ω, Starting T_J=25℃

③ I_{SD}≤9.2A, di/dt≤300A/μs, V_{DD}≤BV_{DSS} , Starting T_J=25℃

④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%

⑤ Essentially Independent of Operating Temperature
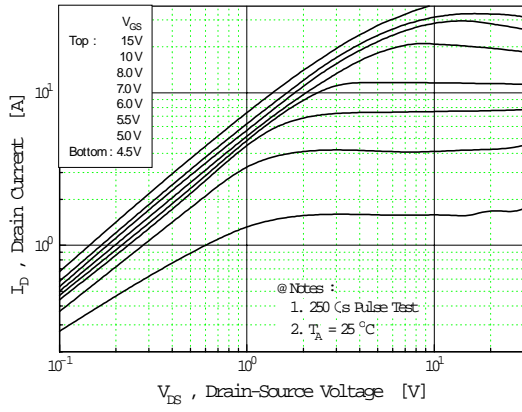
⑥ Adjusted for Cisco

Fig 1. Output Characteristics

V_{GS}
Top :   15V
        10 V
        8.0 V
        7.0 V
        6.0 V
        5.5V
        5.0V
Bottom : 4.5V

@ Notes :
1. 250 µs Pulse Test
2. T_A = 25 °C

I_D , Drain Current   [A]

V_{DS} , Drain-Source Voltage   [V]

Fig 2. Transfer Characteristics

150 °C

25 °C

– 55 °C

@ Notes :
1. V_{GS} = 0 V
2. V_{DS} = 40 V
3. 250 µs Pulse Test

I_D , Drain Current   [A]

V_{GS} , Gate-Source Voltage   [V]
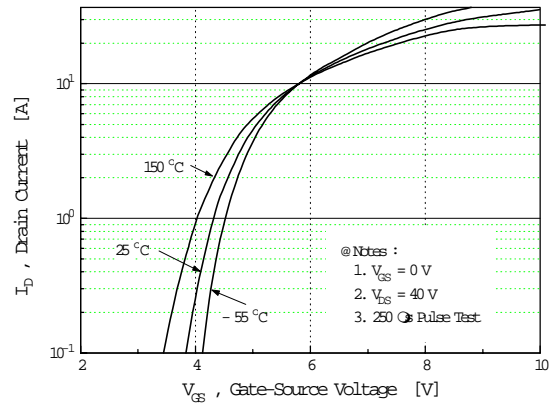
Fig 3. On-Resistance vs. Drain Current

V_{GS} = 10 V

V_{GS} = 20 V

@ Note : T_J = 25 °C

$R_{DS(on)}$, [Ω]
Drain-Source On-Resistance

I_D , Drain Current   [A]
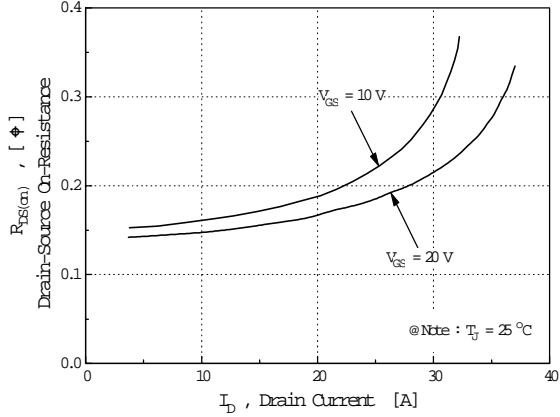
Fig 4. Source-Drain Diode Forward Voltage

150 °C
25 °C

@ Notes :
1. V_{GS} = 0 V
2. 250 µs Pulse Test

I_{DR} , Reverse Drain Current   [A]

V_{SD} , Source-Drain Voltage   [V]
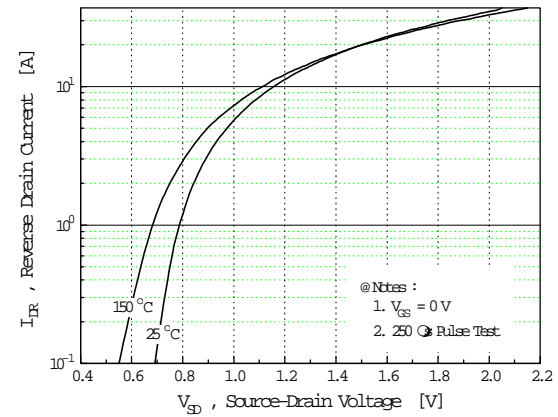
Fig 5. Capacitance vs. Drain-Source Voltage

$C_{iss} = C_{gs} + C_{gd}$ (C_{ds} = shorted)
$C_{oss} = C_{ds} + C_{gd}$
$C_{rss} = C_{gd}$

C_{iss}

C_{oss}

C_{rss}

@ Notes :
1. V_{GS} = 0 V
2. f = 1 MHz

Capacitance   [pF]

V_{DS} , Drain-Source Voltage [V]
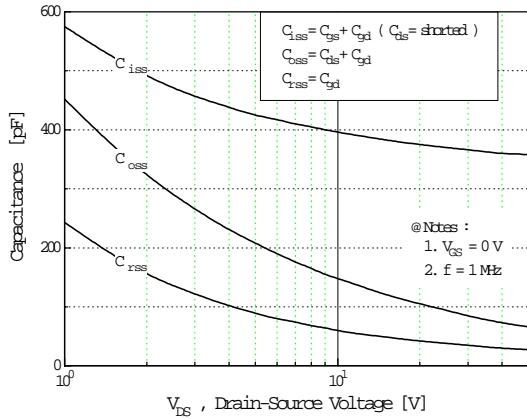
Fig 6. Gate Charge vs. Gate-Source Voltage

V_{DS} = 20 V
V_{DS} = 50 V
V_{DS} = 80 V

@ Notes : I_D = 9.2 A

V_{GS} , Gate-Source Voltage   [V]

Q_G , Total Gate Charge   [nC]
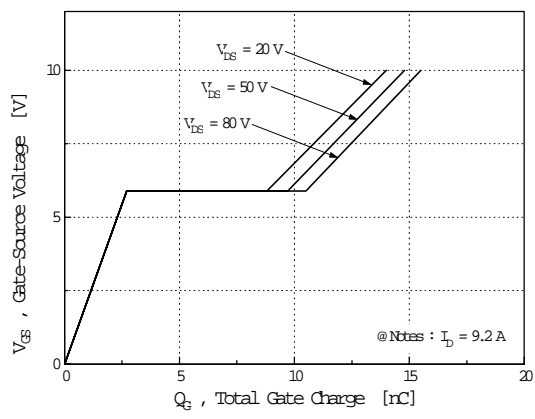
Fig 7. Breakdown Voltage vs. Temperature

BV_{DSS} , (Normalized)
Drain-Source Breakdown Voltage

T_J , Junction Temperature [°C]

@ Notes :
1. V_{GS} = 0 V
2. I_D = 250 µA
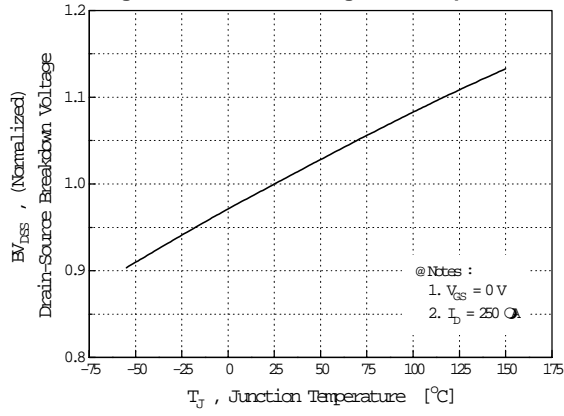
Fig 8. On-Resistance vs. Temperature

$R_{DS(on)}$, (Normalized)
Drain-Source On-Resistance

T_J , Junction Temperature [°C]

@ Notes :
1. V_{GS} = 10 V
2. I_D = 4.6 A
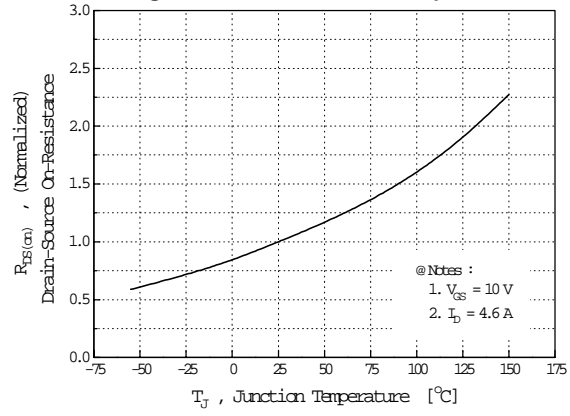
Fig 9. Max. Safe Operating Area

I_D , Drain Current [A]

V_{DS} , Drain-Source Voltage [V]

Operation in This Area
is Limited by $R_{DS(on)}$

10 µs
100 µs
1 ms
10 ms
100 ms
DC

@ Notes :
1. T_A = 25 °C
2. T_J = 150 °C
3. Single Pulse
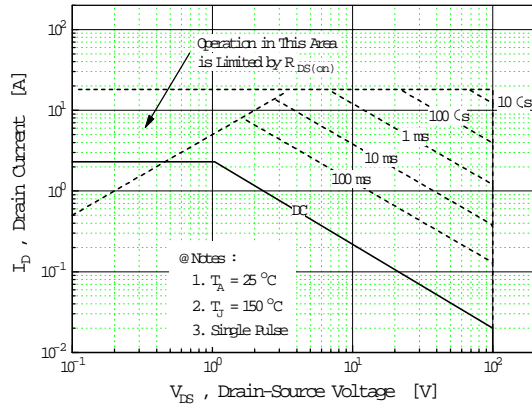
Fig 10. Max. Drain Current vs. Ambient Temperature

I_D , Drain Current [A]

T_A , Ambient Temperature [°C]

Fig 11. Thermal Response

$Z_{\theta JA}(t)$, Thermal Response

t_1 , Square Wave Pulse Duration [sec]

D=0.5
0.2
0.1
0.05
0.02
0.01

@ Notes :
1. $Z_{\theta JA}(t)$=52 °C/W Max.
2. Duty Factor, D=t_1/t_2
3. $T_{JM}-T_A=P_{DM}*Z_{\theta JA}(t)$

P_{DM}
t_1
t_2
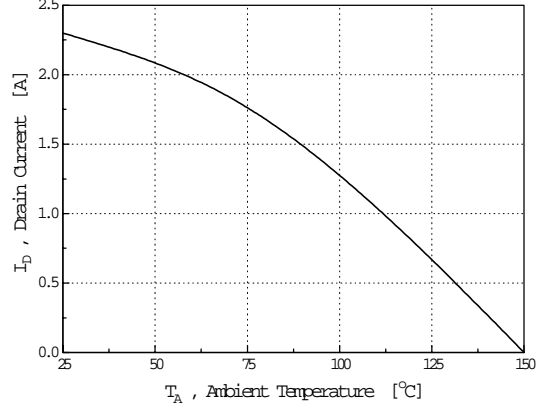
single pulse
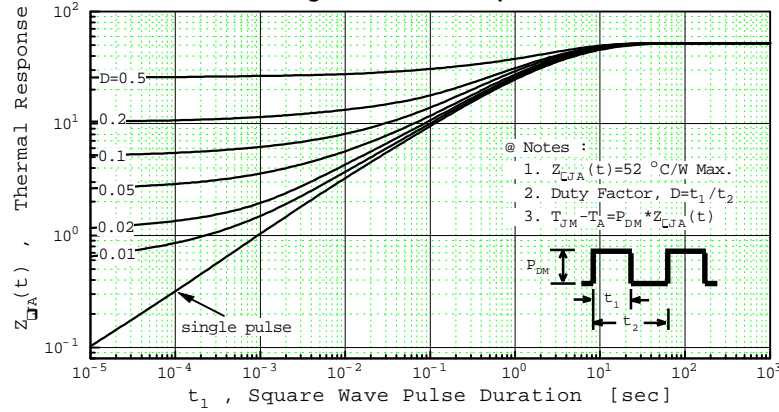
Fig 12. Gate Charge Test Circuit & Waveform

* Current Regulator ”

12V
200nF
50KΩ
300nF
Same Type as DUT
V_{DS}
V_{GS}
DUT
3mA
R_1
R_2
Current Sampling (I_G) Resistor
Current Sampling (I_D) Resistor

V_{GS}
10V
Q_g
Q_{gs}
Q_{gd}
Charge
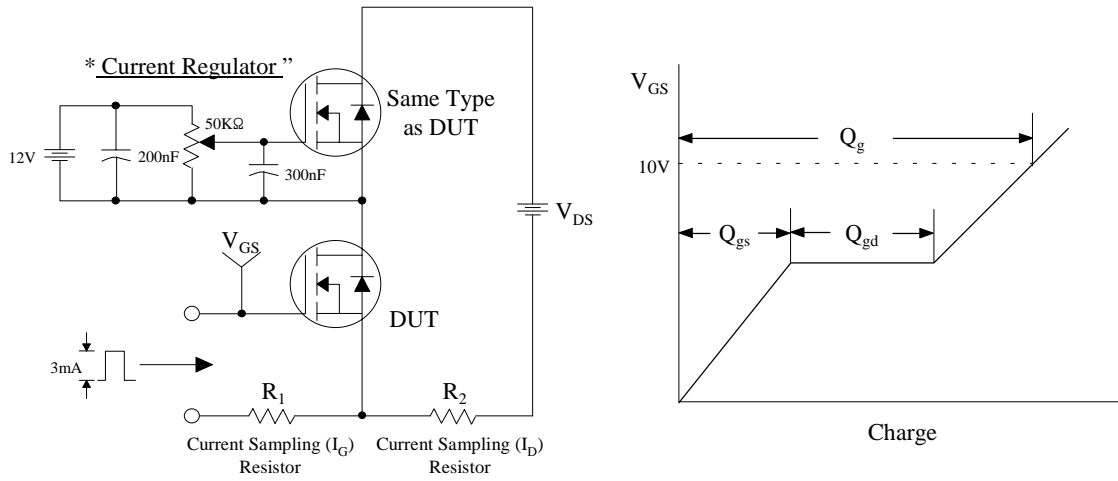
Fig 13. Resistive Switching Test Circuit & Waveforms

R_L
V_{out}
V_{in}
V_{DD}
(0.5 rated V_{DS})
R_G
DUT
10V

V_{out}
90%
V_{in}
10%
$t_{d(on)}$ t_r
t_{on}
$t_{d(off)}$ t_f
t_{off}
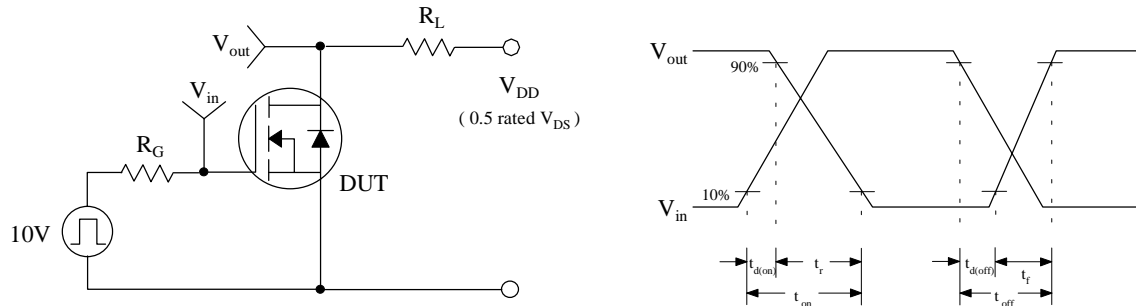
Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

L_L
V_{DS}
I_D
Vary t_p to obtain required peak I_D
R_G
DUT
C
V_{DD}
10V
t_p

$$E_{AS} = \frac{1}{2} L_L I_{AS}{}^2 \frac{BV_{DSS}}{BV_{DSS} -- V_{DD}}$$

BV_{DSS}
I_{AS}
$I_D(t)$
V_{DD}
$V_{DS}(t)$
t_p
Time
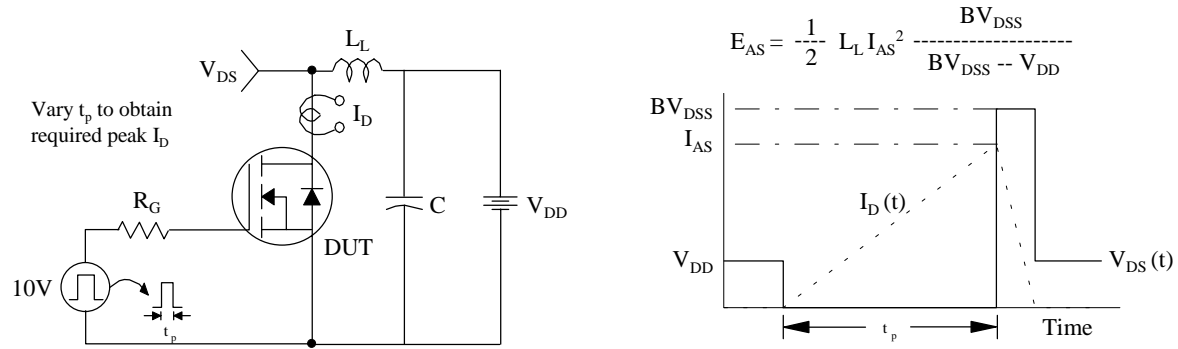
Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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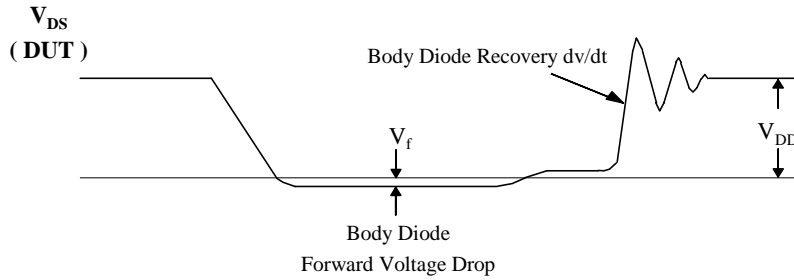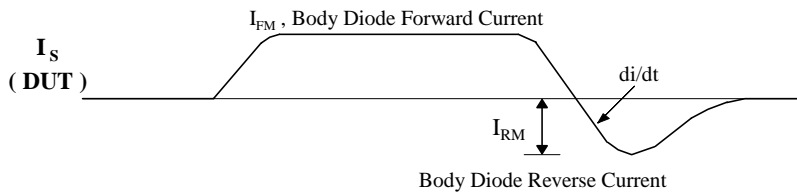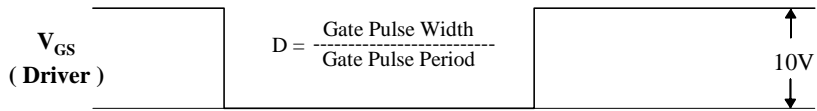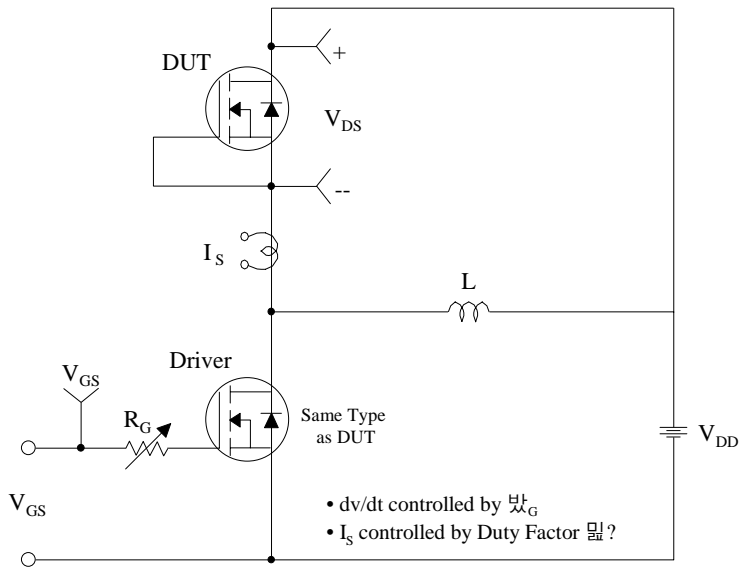
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