MMBF5460LT1

JFET - General Purpose Transistor

P−Channel

ON Semiconductor®

http://onsemi.com

Features

- Pb−Free Package is Available

MAXIMUM RATINGS

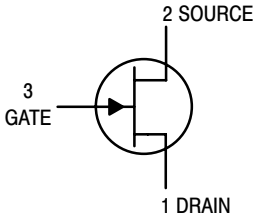
Rating	Symbol	Value	Unit
Drain−Gate Voltage	V_{DG}	40	Vdc
Reverse Gate−Source Voltage	V_{GSR}	40	Vdc
Forward Gate Current	I_{GF}	10	mAdc

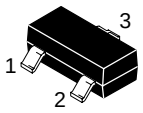
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board, (Note 1) T_A = 25°C Derate above 25°C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

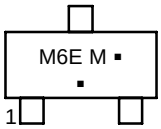
1. FR−5 = 1.0 x 0.75 x 0.062 in.





SOT−23 (TO−236)
CASE 318
STYLE 10

MARKING DIAGRAM



M6E = Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBF5460LT1	SOT−23	3,000 / Tape & Reel
MMBF5460LT1G	SOT−23 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Gate−Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	$V_{(BR)GSS}$	40	−	−	Vdc
Gate Reverse Current (V_{GS} = 20 Vdc, V_{DS} = 0) (V_{GS} = 20 Vdc, V_{DS} = 0, T_A = 100°C)	I_{GSS}	 − −	 − −	 5.0 1.0	 nAdc μAdc
Gate Source Cutoff Voltage (V_{DS} = 15 Vdc, I_D = 1.0 μAdc)	$V_{GS(off)}$	0.75	−	6.0	Vdc
Gate Source Voltage (V_{DS} = 15 Vdc, I_D = 0.1 mAdc)	V_{GS}	0.5	−	4.0	Vdc
ON CHARACTERISTICS					
Zero−Gate−Voltage Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	I_{DSS}	−1.0	−	−5.0	mAdc
SMALL−SIGNAL CHARACTERISTICS					
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|Y_{fs}\|$	1000	−	4000	μmhos
Output Admittance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 kHz)	$\|y_{os}\|$	−	−	75	μmhos
Input Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	−	5.0	7.0	pF
Reverse Transfer Capacitance (V_{DS} = 15 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{rss}	−	1.0	2.0	pF

DRAIN CURRENT versus GATE SOURCE VOLTAGE

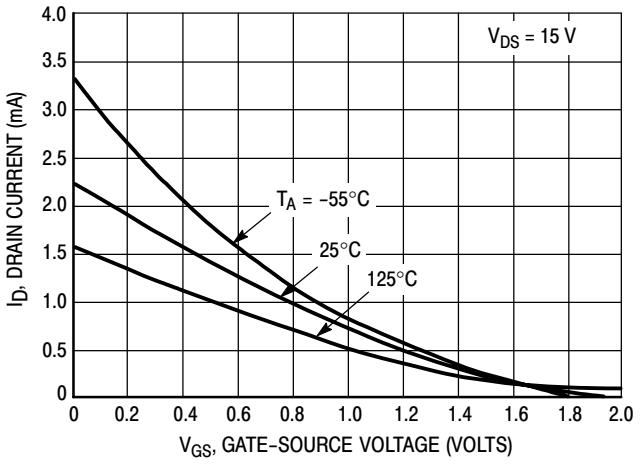


Figure 1. $V_{GS(off)}$ = 2.0 Volts

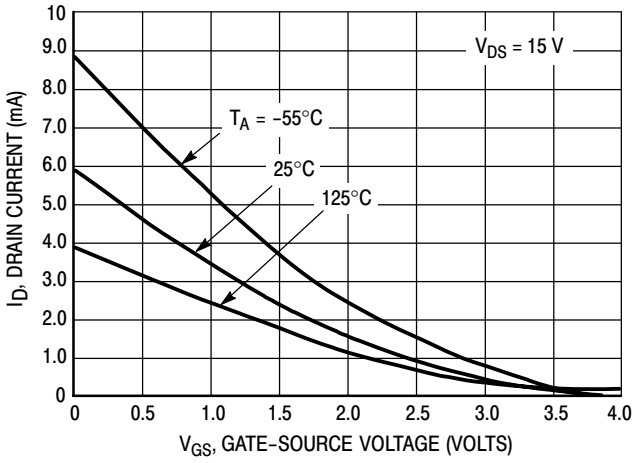


Figure 2. $V_{GS(off)}$ = 4.0 Volts

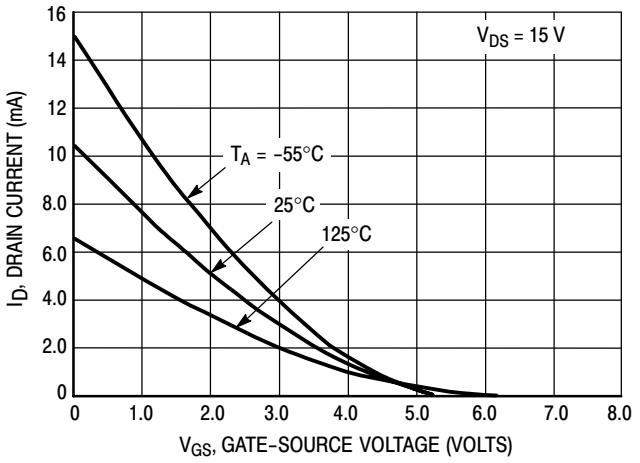


Figure 3. $V_{GS(off)}$ = 5.0 Volts

FORWARD TRANSFER ADMITTANCE versus DRAIN CURRENT

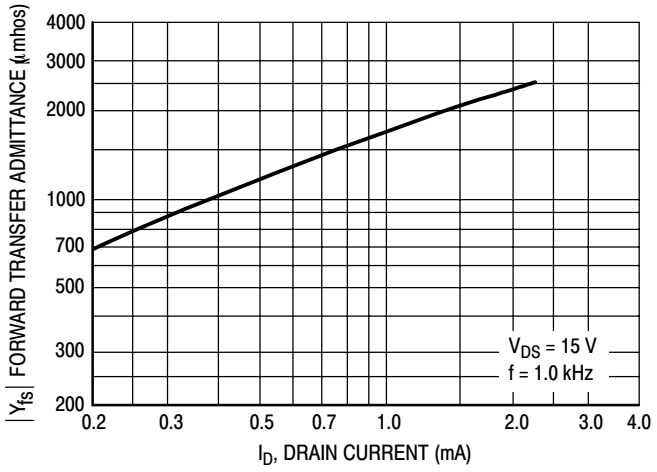


Figure 4. $V_{GS(off)}$ = 2.0 Volts

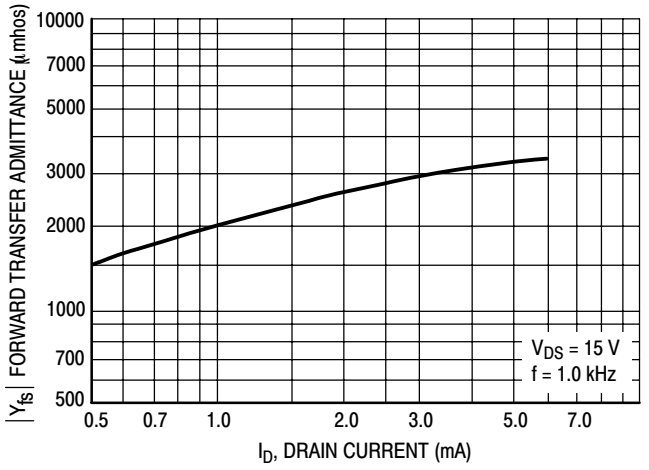


Figure 5. $V_{GS(off)}$ = 4.0 Volts

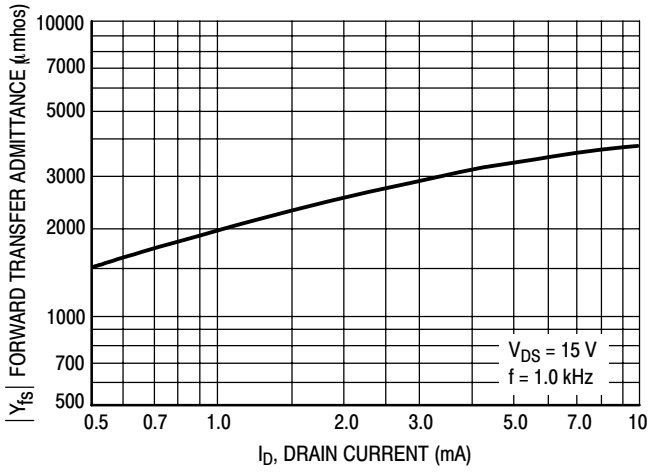


Figure 6. $V_{GS(off)}$ = 5.0 Volts

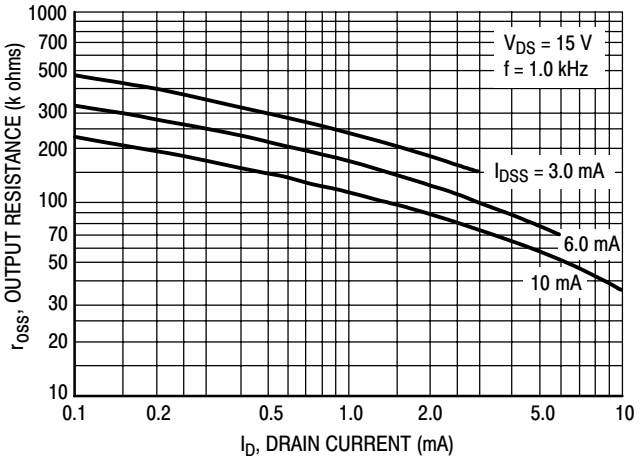


Figure 7. Output Resistance versus Drain Current

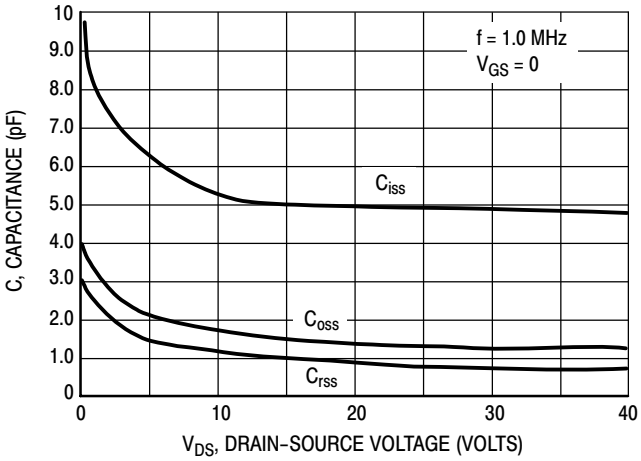


Figure 8. Capacitance versus Drain−Source Voltage

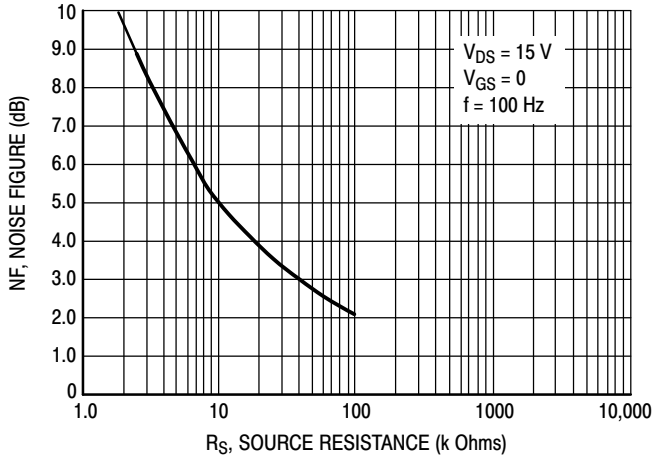
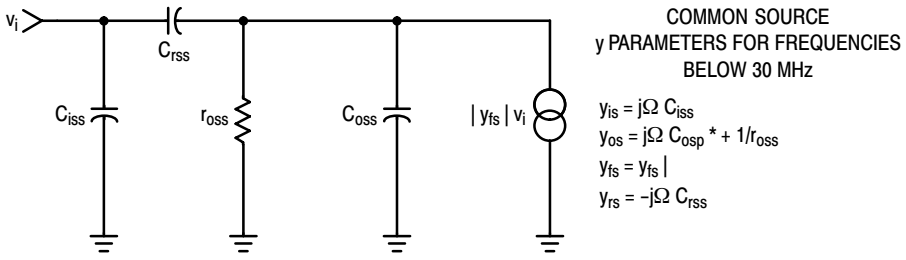


Figure 9. Noise Figure versus Source Resistance



*C_{osp} is C_{oss} in parallel with Series Combination of C_{iss} and C_{rss}.

NOTE:

1. Graphical data is presented for dc conditions. Tabular data is given for pulsed conditions (Pulse Width = 630 ms, Duty Cycle = 10%).

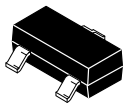
Figure 10. Equivalent Low Frequency Circuit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

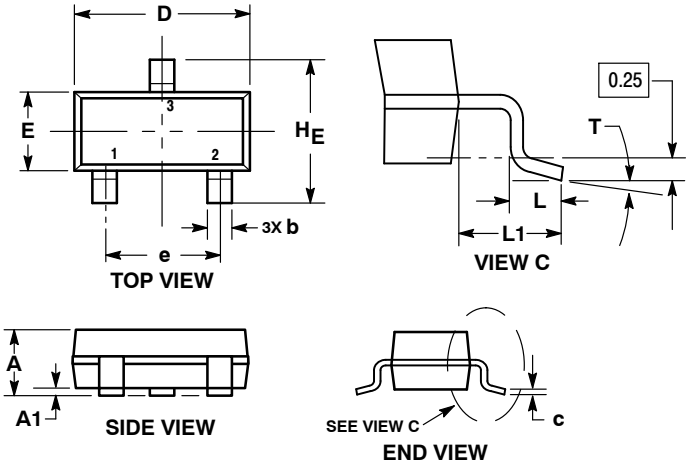
ON Semiconductor®

SOT−23 (TO−236)
CASE 318−08
ISSUE AS

DATE 30 JAN 2018



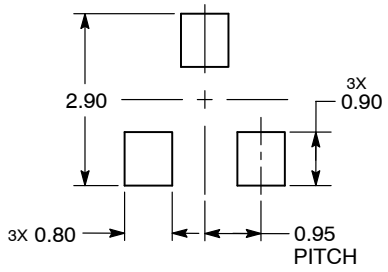
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

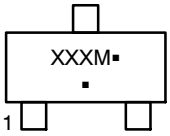
	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.039	0.044
A1	0.01	0.06	0.10	0.000	0.002	0.004
b	0.37	0.44	0.50	0.015	0.017	0.020
c	0.08	0.14	0.20	0.003	0.006	0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.080
L	0.30	0.43	0.55	0.012	0.017	0.022
L1	0.35	0.54	0.69	0.014	0.021	0.027
H_E	2.10	2.40	2.64	0.083	0.094	0.104
T	0°	−−−	10°	0°	−−−	10°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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DESCRIPTION:	**SOT−23 (TO−236)**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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