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MOSFET – Power, N-Channel, SUPERFET III, FRFET 650 V, 36 A, 95 mΩ

NVB095N65S3F

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)} = 78 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 65 \text{ nC}$)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 597 pF)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen-Free/BFR-Free and are RoHS Compliant

Applications

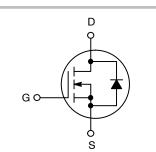
- Automotive On Board Charger HEV-EV
- Automotive DC/DC Converter HEV-EV

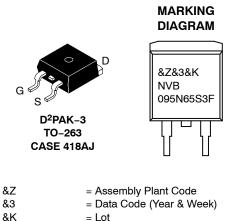


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V _{DSS}	R _{DS(ON)} MAX	I _D MAX	
650 V	95 mΩ @ 10 V	36 A	





NVB095N65S3F = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage	650	V	
V _{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I _D	Drain Current	– Continuous (T _C = 25°C)	36	A
		– Continuous (T _C = 100°C)	22.8	
I _{DM}	Drain Current	- Pulsed (Note 1)		A
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		440	mJ
I _{AS}	Avalanche Current (Note 2)		4.6	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		2.72	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50]
P _D	Power Dissipation	(T _C = 25°C)	272	W
		- Derate Above 25°C	2.176	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds		300	°C

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 4.6 \text{ A}$, $R_G = 25 \Omega$, starting $T_J = 25^{\circ}\text{C}$. 3. $I_{SD} \le 18 \text{ A}$, di/dt $\le 200 \text{ A}/\mu\text{s}$, $V_{DD} \le 400 \text{ V}$, starting $T_J = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case, Max.	0.46	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

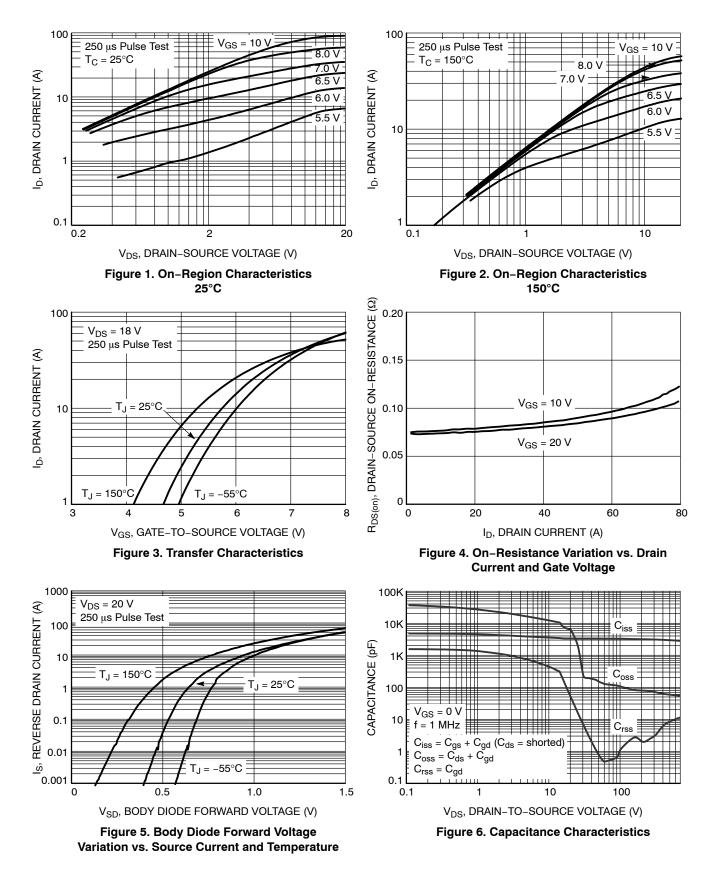
Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping [†]
NVB095N65S3F	NVB095N65S3F	D ² PAK	330 mm	24 mm	800 / Tape & Reel

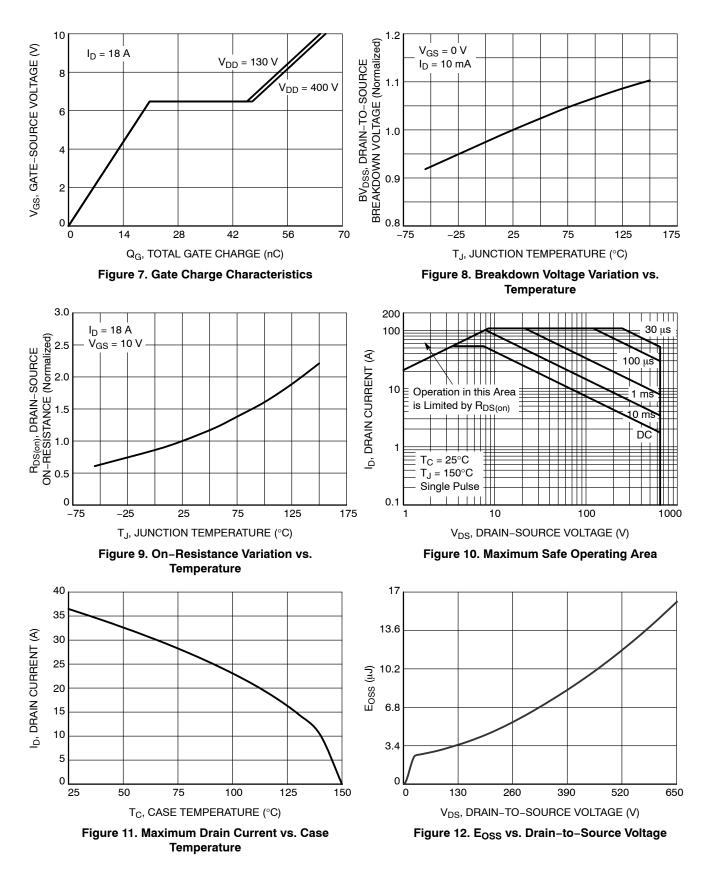
+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

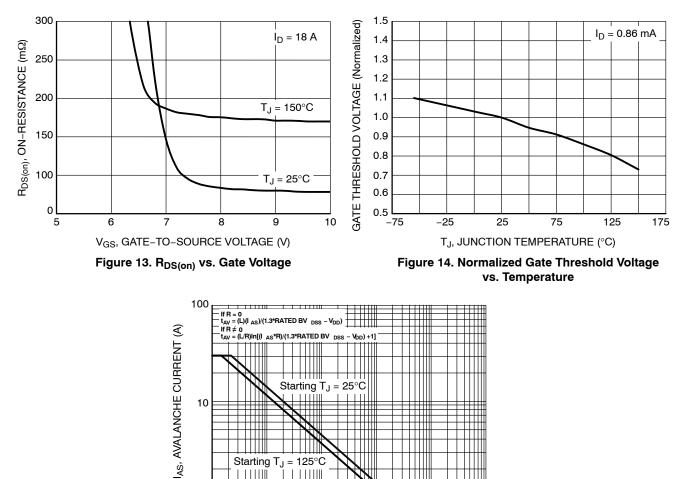
ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}C$ unless otherwise noted)

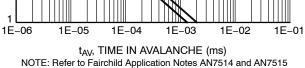
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
OFF CHARACTERISTICS						
Drain to Source Breakdown Voltage	BV _{DSS}	V_{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V_{GS} = 0 V, I_{D} = 10 mA, T_{J} = 150 $^{\circ}C$	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_{J}$	I_D = 15 mA, Referenced to 25°C		640		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 650 V, V_{GS} = 0 V			10	μΑ
		$V_{DS} = 520 \text{ V}, \text{ T}_{C} = 125^{\circ}\text{C}$		12		
Gate to Body Leakage Current	I _{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}, I_D = 0.86 \text{ mA}$	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)} / \Delta T_J$	$V_{GS} = V_{DS}, I_D = 0.86 \text{ mA}$		-7		mV/°C
Static Drain to Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 18 A		78	95	mΩ
Forward Transconductance	9 _{FS}	$V_{DS} = 20 \text{ V}, \text{ I}_{D} = 18 \text{ A}$		19		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{iss}			3020		pF
Output Capacitance	C _{oss}	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		61		1
Reverse Transfer Capacitance	C _{rss}			7.0		
Effective Output Capacitance	C _{oss(eff.)}	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		597		pF
Energy Related Output Capacitance	C _{oss(er.)}	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		107		pF
Total Gate Charge at 10V	Q _{g(tot)}			66		nC
Threshold Gate Charge	Q _{g(th)}	V_{GS} = 10 V, V_{DS} = 400 V, I_{D} = 18 A (Note 4)		13		
Gate to Source Gate Charge	Q _{gs}			22		1
Gate to Drain "Miller" Charge	Q _{gd}			26		_
Equivalent Series Resistance	ESR	f = 1 MHz		2.4		Ω
SWITCHING CHARACTERISTICS	II					
Turn-On Delay Time	t _{d(on)}			26		ns
Turn-On Rise Time	t _r	V_{GS} = 10 V, V_{DD} = 400 V,		26		ns
Turn-Off Delay Time	t _{d(off)}	$I_D = 18 \text{ A}, R_g = 2.2 \Omega$ (Note 4)		62		ns
Turn-Off Fall Time	t _f	× ,		4.0		ns
SOURCE-DRAIN DIODE CHARACTER	L L					
Maximum Continuous Source to Drain Diode Forward Current	۱ _S	V _{GS} = 0 V			36	A
Maximum Pulsed Source to Drain Diode Forward Current	I _{SM}	V _{GS} = 0 V			90	A
Source to Drain Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _{SD} = 18 A			1.3	V
Reverse Recovery Time	t _{rr}			97		ns
Charge Time	t _a	V _{GS} = 0 V, dI _F /dt = 100 A/μs,		78		
Discharge Time	t _b	$V_{GS} = 0$ V, $di_{F}/dt = 100 A/\mu s$, $I_{SD} = 18 A$		19		
Reverse Recovery Charge	Q _{rr}		<u> </u>	349		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Essentially independent of operating temperature typical characteristics.











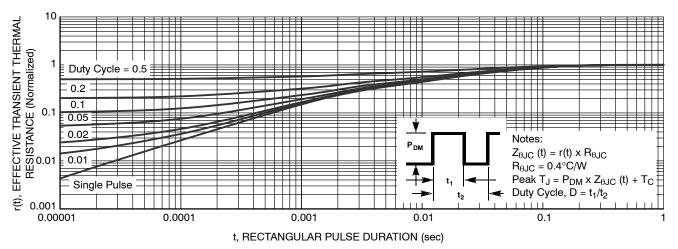


Figure 16. Transient Thermal Response

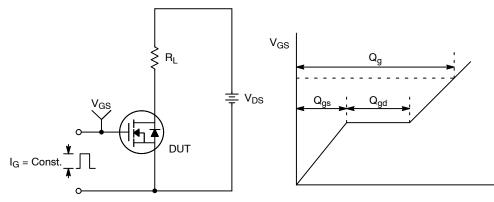


Figure 17. Gate Charge Test Circuit & Waveform

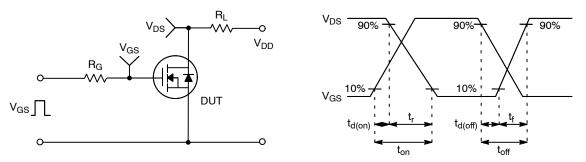


Figure 18. Resistive Switching Test Circuit & Waveforms

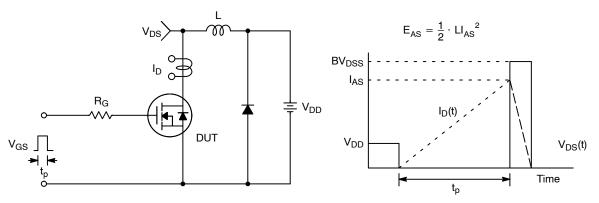
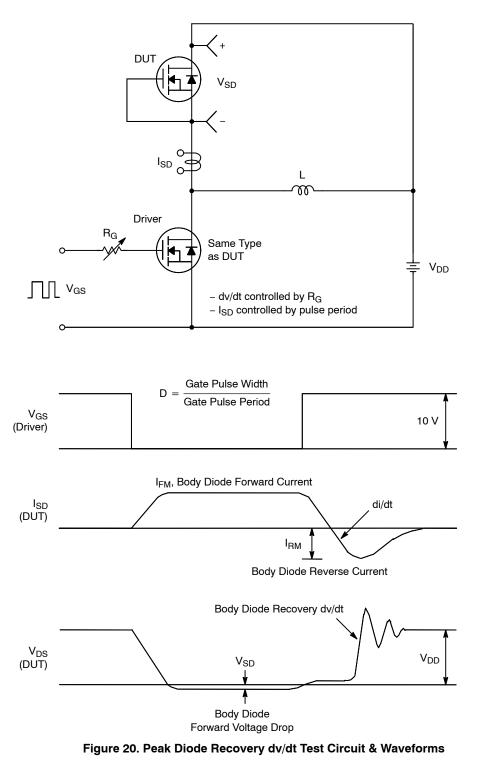


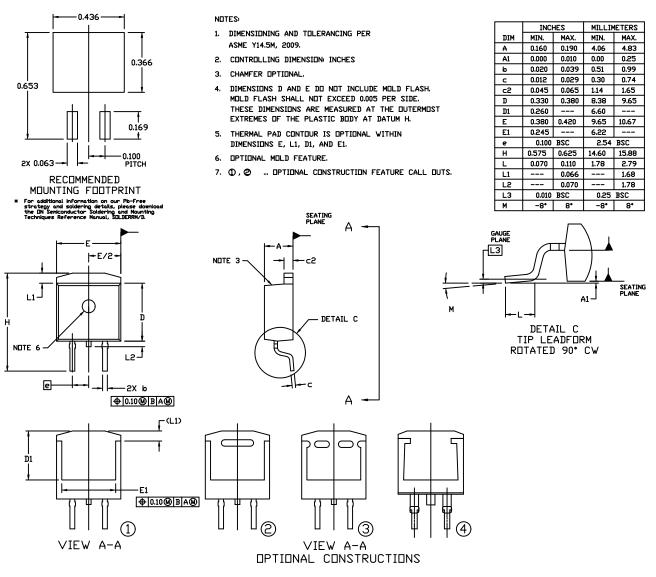
Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms



PACKAGE DIMENSIONS

D²PAK-3 (TO-263, 3-LEAD) CASE 418AJ

ISSUE E



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