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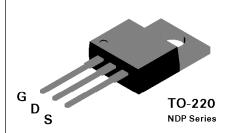
NDP6020P / NDB6020P P-Channel Logic Level Enhancement Mode Field Effect Transistor

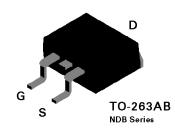
General Description

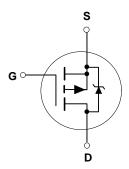
These logic level P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP6020P	NDB6020P	Units	
V _{DSS}	Drain-Source Voltage	-20		V	
V _{GSS}	Gate-Source Voltage - Continuous	±8		V	
I _D	Drain Current - Continuous	-2	24	А	
	- Pulsed	-7	70		
P _D	Total Power Dissipation @ T _C = 25°C	6	0	W	
	Derate above 25°C	0.	.4	W/°C	
T _J ,T _{STG}	Operating and Storage Temperature Range	ting and Storage Temperature Range -65 to 175		°C	

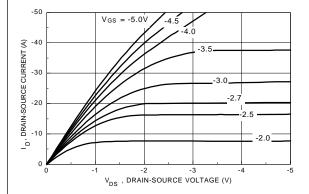
Electri	cal Characteristics (T _c = 25°C ur	nless otherwise noted)					
Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CH	ARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$		-20			V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$				-1	μA
			$T_J = 55^{\circ}C$			-10	μA
I _{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 8 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAI	RACTERISTICS (Note 1)						
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$		-0.4	-0.7	-1	V
			T _J = 125°C	-0.3	-0.56	-0.7	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_{D} = -12 \text{ A}$			0.041	0.05	Ω
			T _J = 125°C		0.06	0.08	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -2.7 \text{ V}, I_{D} = -10 \text{ A}$			0.059	0.07	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = -2.5 \text{ V}, I_{D} = -10 \text{ A}$			0.064	0.075	
I _{D(on)}	On-State Drain Current	$V_{GS} = -4.5 \text{ V}, V_{DS} = -5 \text{ V}$		-24			Α
g _{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -12 \text{ A}$			14		S
DYNAMI	CCHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$			1590		pF
Coss	Output Capacitance				725		pF
C _{rss}	Reverse Transfer Capacitance				215		pF
SWITCHI	NG CHARACTERISTICS (Note 1)			•		•	
t _{D(on)}	Turn - On Delay Time	$V_{DD} = -20 \text{ V}, \ I_{D} = -3 \text{ A},$			15	30	nS
t _r	Turn - On Rise Time	$V_{GS} = -5 \text{ V}, R_{GEN} = 6 \Omega$		27	60	nS	
t _{D(off)}	Tum - Off Delay Time				120	250	nS
t _f	Turn - Off Fall Time				70	150	nS
Q _g	Total Gate Charge	V _{DS} = -10 V,			25	35	nC
Q_{gs}	Gate-Source Charge	$I_D = -24 \text{ A}, \ V_{GS} = -5 \text{ V}$			5		nC
Q_{gd}	Gate-Drain Charge				10		nC

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DRAIN-S	OURCE DIODE CHARACTERISTICS	•				
I _s	Maximum Continuous Drain-Source Diode Forward Current				-24	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-80	Α
V _{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -12 \text{ A (Note 1)}$		-1.1	-1.3	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = -24 \text{ A},$ $dI_F/dt = 100 \text{ A/}\mu\text{s}$		60		ns
I _{rr}	Reverse Recovery Current			-1.7		Α
THERMA	AL CHARACTERISTICS					
R _{ØJC}	Thermal Resistance, Junction-to-Case				2.5	°C/W
R _{OJA}	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:

^{1.} Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics



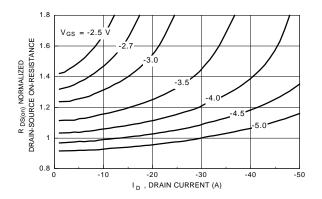
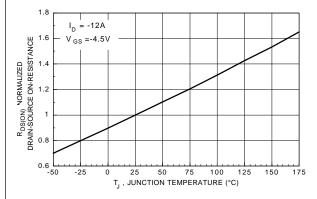


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.



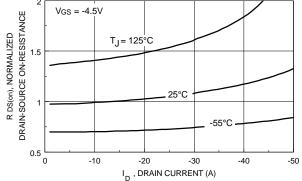
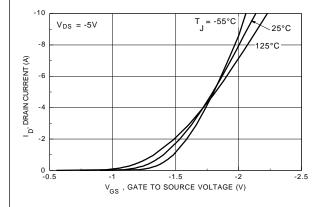


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Drain Current and Temperature.



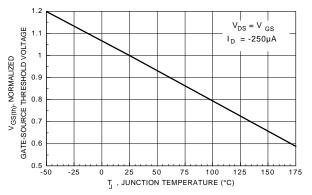


Figure 5. Transfer Characteristics.

Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

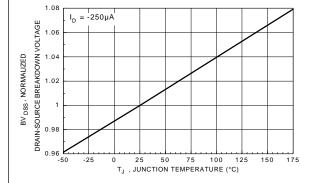


Figure 7. Breakdown Voltage Variation with Temperature.

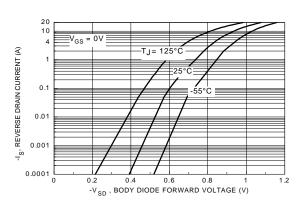


Figure 8. Body Diode Forward Voltage
Variation with Current and Temperature.

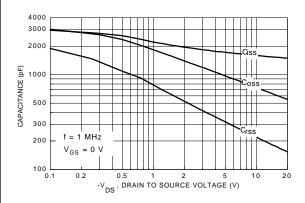


Figure 9. Capacitance Characteristics.

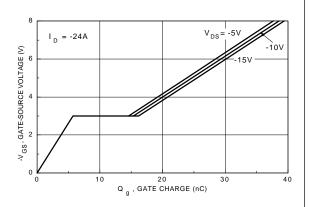


Figure 10. Gate Charge Characteristics.

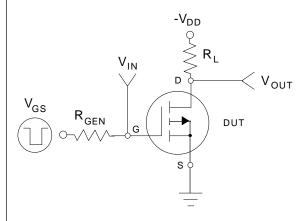


Figure 11. Switching Test Circuit.

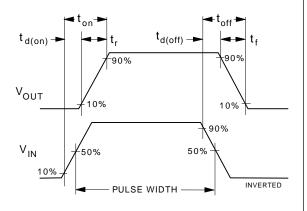
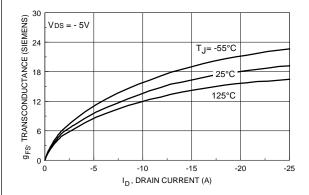


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)



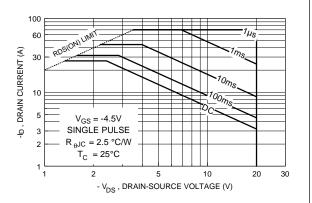


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

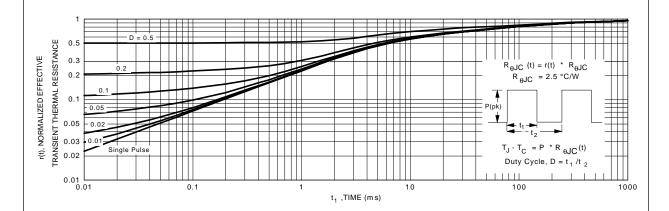


Figure 15. Transient Thermal Response Curve.

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