## **ON Semiconductor**

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## **Power MOSFET**

## 24 V, 80 A, N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### **Features**

• These Devices are Pb-Free and are RoHS Compliant

#### **Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	24	Vdc
Gate-to-Source Voltage - Continuous	$V_{GS}$	±20	Vdc
Drain Current – Continuous @ $T_C$ = 25°C – Single Pulse ( $t_p$ = 10 $\mu$ s)	I <sub>D</sub> I <sub>DM</sub>	80* 200	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C	$P_{D}$	75	Watts
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J$ = 25°C ( $V_{DD}$ = 24 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 17 Apk, $L$ = 5.0 mH, $R_G$ = 25 $\Omega$ )	E <sub>AS</sub>	733	mJ
Thermal Resistance  – Junction-to-Case  – Junction-to-Ambient (Note 1)  – Junction-to-Ambient (Note 2)	$egin{array}{c} R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA} \end{array}$	1.65 67 120	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
- When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

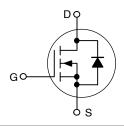


#### ON Semiconductor®

#### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX	
24 V	5.0 mΩ	80 A	

#### N-Channel



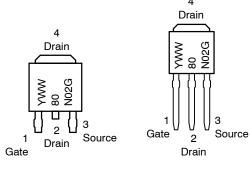






CASE 369AA CASE 369C CASE 369D
DPAK DPAK DPAK
(Surface Mount) (Surface Mount) (Straight Lead)
STYLE 2 STYLE 2 STYLE 2

# MARKING DIAGRAMS & PIN ASSIGNMENTS



 80N02
 = Device Code

 Y
 = Year

 WW
 = Work Week

 G
 = Pb-Free Package

#### **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

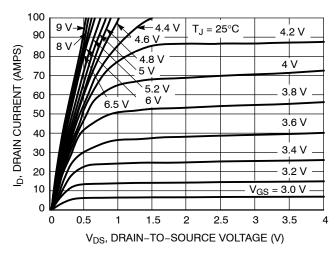
<sup>\*</sup>Chip current capability limited by package.

### **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS		,			ı	1
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Positive Temperature Coefficient		V <sub>(BR)DSS</sub>	24 -	27 25	_ _	Vdc mV/°C
Zero Gate Voltage Drain Current $(V_{GS} = 0 \text{ Vdc}, V_{DS} = 24 \text{ Vdc})$ $(V_{GS} = 0 \text{ Vdc}, V_{DS} = 24 \text{ Vdc}, T_J$	= 125°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub>	= $\pm 20$ Vdc, $V_{DS} = 0$ Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 250 \mu Adc)$ Negative Threshold Temperature C	Coefficient	V <sub>GS(th)</sub>	1.0	1.9 -3.8	3.0	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3)		R <sub>DS(on)</sub>	- - -	5.0 7.5 5.0 7.5	5.8 9.0 5.8 9.0	mΩ
Forward Transconductance (V <sub>DS</sub> =	= 15 Vdc, I <sub>D</sub> = 10 Adc) (Note 3)	9FS	-	20	-	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V <sub>DS</sub> = 20 Vdc,	C <sub>iss</sub>	_	2250	2600	pF
Output Capacitance	$V_{GS} = 0 V$	C <sub>oss</sub>	-	900	1100	
Transfer Capacitance	f = 1.0 MHz)	C <sub>rss</sub>	-	400	525	
SWITCHING CHARACTERISTICS (	Note 4)		_			
Turn-On Delay Time	(V <sub>GS</sub> = 4.5 Vdc,	t <sub>d(on)</sub>	-	17	30	ns
Rise Time	$V_{DD} = 20 \text{ Vdc},$	t <sub>r</sub>	-	67	125	
Turn-Off Delay Time	I <sub>D</sub> = 20 Adc,	t <sub>d(off)</sub>	-	28	45	
Fall Time	$R_G = 2.5 \Omega$ )	t <sub>f</sub>	-	40	75	
Gate Charge	$(V_{GS} = 4.5 \text{ Vdc},$	$Q_T$	-	30	42	nC
	I <sub>D</sub> = 20 Adc,	Q1	-	7.0	12	
	V <sub>DS</sub> = 20 Vdc) (Note 3)	Q2	_	18	28	
SOURCE-DRAIN DIODE CHARAC	TERISTICS					
		V <sub>SD</sub>		0.92 1.05 0.70	1.2 - -	Vdc
Reverse Recovery Time	$(I_S = 20 \text{ Adc}, V_{GS} = 0 \text{ Vdc},$ $dI_S/dt = 100 \text{ A/}\mu\text{s}) \text{ (Note 3)}$	t <sub>rr</sub>	-	38	52	ns
		t <sub>a</sub>	-	20	-	1
		t <sub>b</sub>	_	18	-	1
Reverse Recovery Stored Charge		Q <sub>rr</sub>	_	0.038	_	μС

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

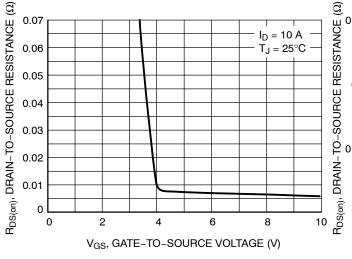
#### **TYPICAL CHARACTERISTICS**



160 150  $V_{DS} \ge 24 \text{ V}$ 140 130 120 DRAIN CURRENT (AMPS) 110 100 80 70 T<sub>J</sub> = 25°C 60 50 40  $T_J = 125^{\circ}C$ 30 20  $T_J = -55^{\circ}C$ 10 ے 2 V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



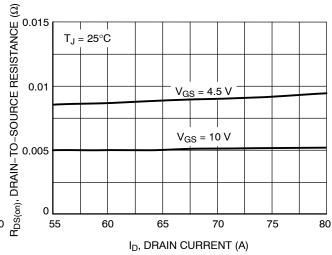
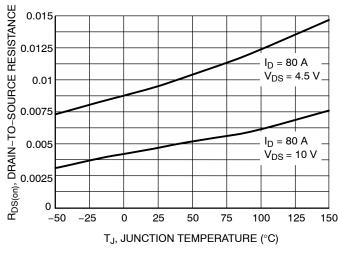


Figure 3. On-Resistance versus Gate-To-Source Voltage

Figure 4. On-Resistance versus Drain Current and Gate Voltage



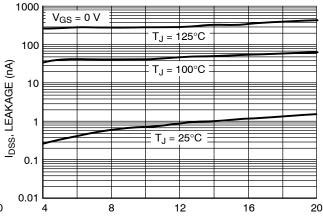


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-To-Source Leakage
Current versus Voltage

V<sub>DS</sub>, DRAIN-TO-SOURCE VOLTAGE (V)

#### **TYPICAL CHARACTERISTICS**

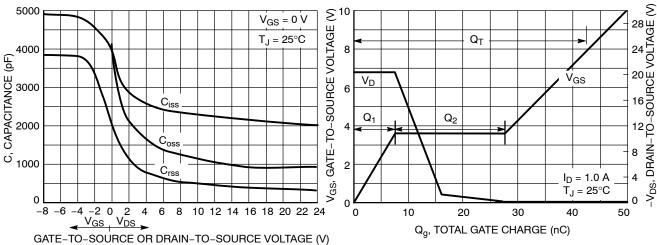


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

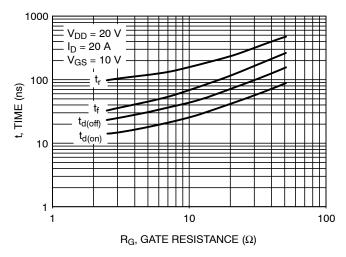
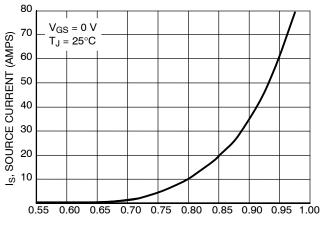


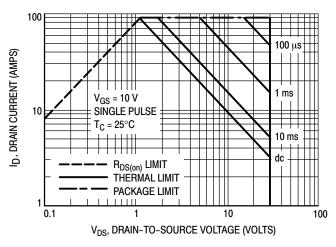
Figure 9. Resistive Switching Time Variation versus Gate Resistance



V<sub>SD</sub>, SOURCE-TO-DRAIN VOLTAGE (V)

Figure 10. Diode Forward Voltage versus Current

#### **TYPICAL CHARACTERISTICS**



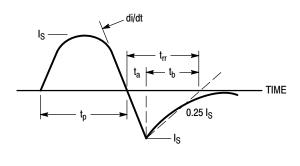


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Diode Reverse Recovery Waveform

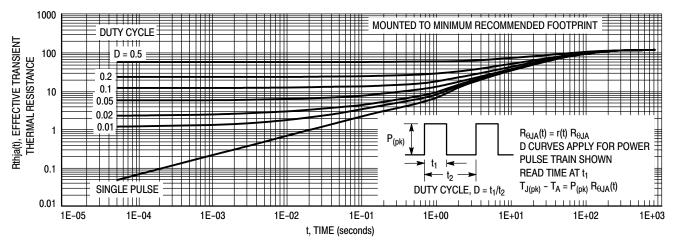


Figure 13. Thermal Response - Various Duty Cycles

#### ORDERING INFORMATION

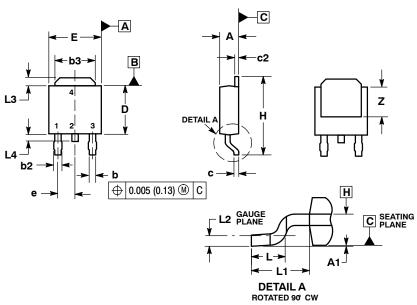
Order Number	Package	Shipping <sup>†</sup>
NTD80N02T4G	DPAK-3 (Pb-Free)	2500 / Tape & Reel
NTD80N02-1G	DPAK-3 Straight Lead (Pb-Free)	75 Units / Rail

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

### **DPAK (SINGLE GAUGE)**

CASE 369AA-01 **ISSUE B** 



- NOTES:

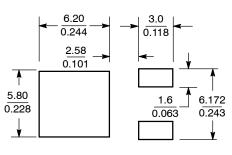
  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: INCHES.
  3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
  5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
Е	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
Η	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51	BSC
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE

4. DRAIN

#### **SOLDERING FOOTPRINT\***



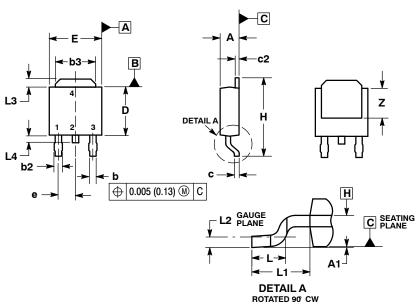
 $\left(\frac{\text{mm}}{\text{inches}}\right)$ SCALE 3:1

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### **PACKAGE DIMENSIONS**

#### **DPAK (SINGLE GAUGE)**

CASE 369C-01 ISSUE D



#### NOTES:

- NOTES:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.

  2. CONTROLLING DIMENSION: INCHES.

  3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.

  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.

  5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

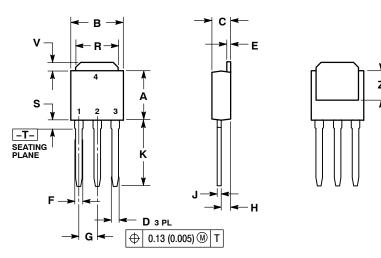
  6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
Е	0.250	0.265	6.35	6.73
е	0.090 BSC		2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020	0 BSC 0.5		BSC
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
7	0 155		3.93	

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

#### PACKAGE DIMENSIONS

#### **DPAK** CASE 369D-01 **ISSUE B**



#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

STYLE 2: PIN 1. GATE

- 2 DRAIN
- SOURCE DRAIN

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NTD80N02/D