Buck Converter - High Current, Synchronous

NCP3233

The NCP3233 is a high current, high efficiency voltage−mode synchronous buck controller which operates from 3.0 V to 21 V input and generates output voltages down to 0.6 V at up to 20 A.

Features

- Wide Input Voltage Range from 3.0 V to 21 V
- 0.6 V 1% Accurate Internal Reference Over Temperature
- Fixed Switching Frequency: 500 kHz (1 MHz and 300 kHz options contact factory)
- External Programmable Soft−Start
- Lossless Low−side and High−side FET Current Sensing
- Output Overvoltage Protection and Undervoltage Protection
- Recoverable Overvoltage Protection
- Hiccup Mode Operation for UVP, LS OCP and TSD
- Pre−bias Start−up
- Adjustable Output Voltage
- Power Good Output
- Internal Overtemperature Protection
- Adjustable Input UVLO
- This is a Pb−Free Device

Typical Application

- Cellular Base Stations
- ASIC, FPGA, DSP and CPU Core and I/O Supplies
- Telecom and Network Equipment
- Server and Storage System

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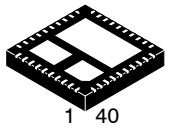
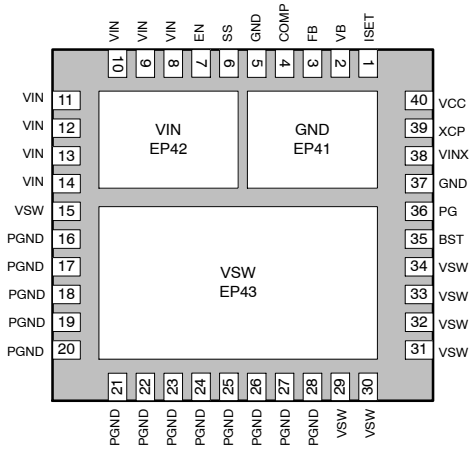


QFN40 6x6, 0.5P
CASE 485AZ

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3233MNTXG	QFN40 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

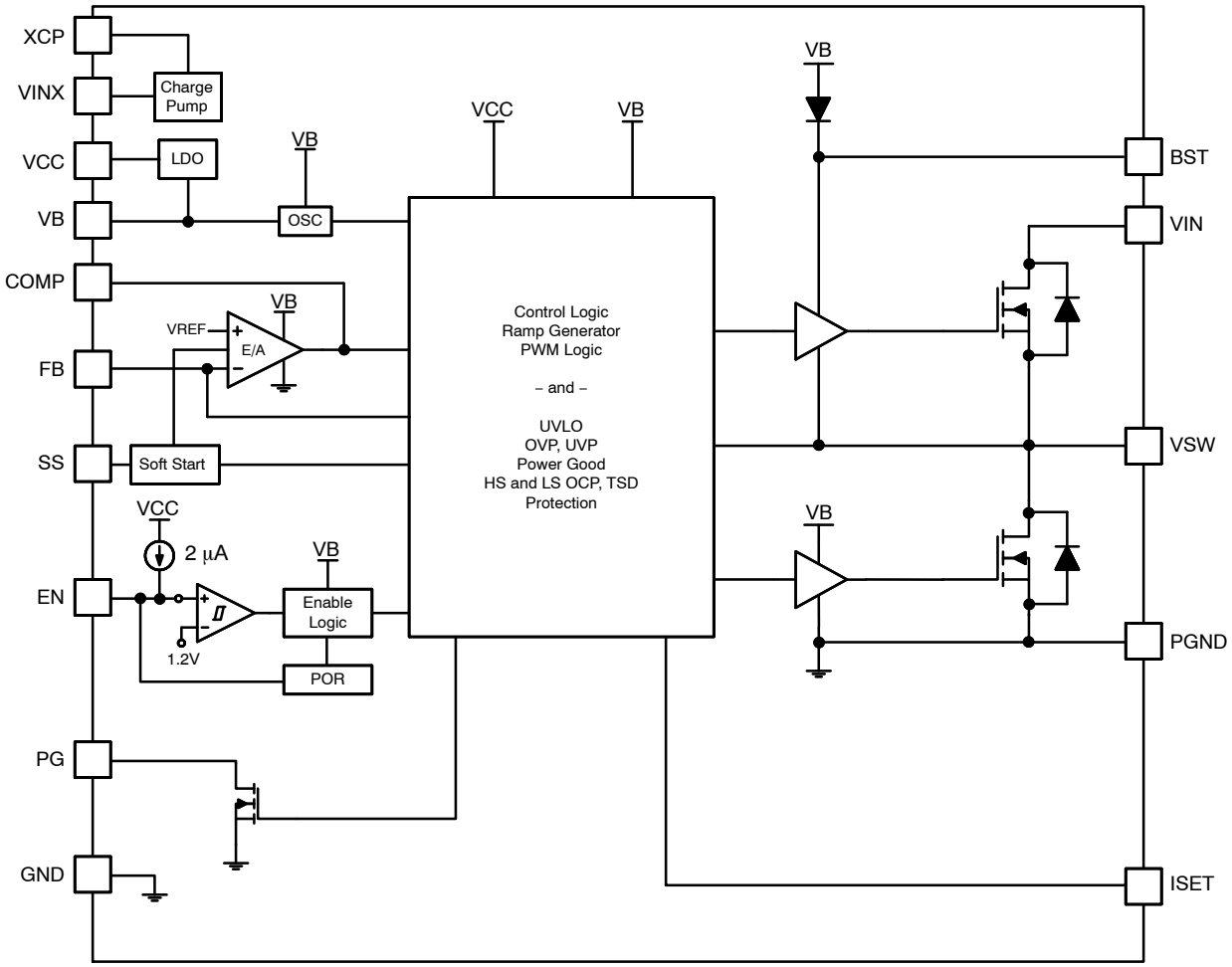


Figure 1. NCP3233 Block Diagram

PIN DESCRIPTION

Pin No.	Symbol	Description
1	ISET	A resistor from this pin to ground sets the low−side overcurrent protection (OCP) threshold.
2	VB	The internal LDO output and input supply for the NCP3233. Connect a minimum of 4.7 μF ceramic capacitor from this pin to PGND.
3	FB	Output voltage feedback.
4	COMP	Output of the error amplifier.
5, 37	GND	Analog ground.
6	SS	A capacitor from this pin to GND allows the user to adjust the soft−start ramp time.
7	EN	Logic control for enabling the switcher. An internal pull−up enables the device automatically. The EN pin can also be driven high to turn on the device, or low to turn off the device. A comparator and precision reference allow the user to implement this pin as an adjustable UVLO circuit.
8−14, EP42	VIN	The VIN pin is connected to the internal power MOSFETs. Connect input capacitor from VIN to PGND as close as possible.
15, 29−34, EP43	VSW	The VSW pin is connection of the drain and source of the internal power MOSFETs. Connect VSW to one terminal of the inductor.
16−28	PGND	Ground reference and high−current return path for the low−side gate driver and low−side MOSFET.
35	BST	Top gate driver input supply, a bootstrap capacitor connection between the switch node and this pin.
36	PG	Power good indicator of the output voltage. Open−drain output. Connect PG to VCC with an external resistor.
38	VINX	Input pin of internal charge pump, tie to VIN for 3.3 V input voltage application cases and tie to GND for 5 V or higher input voltage application cases.
39	XCP	Switching node of internal charge pump, leave it floating for 5 V or higher input voltage application cases
40	VCC	Input Supply for IC.
EP41	GND	Exposed Pad. Connect GND to a large copper plane at ground potential to improve thermal dissipation.

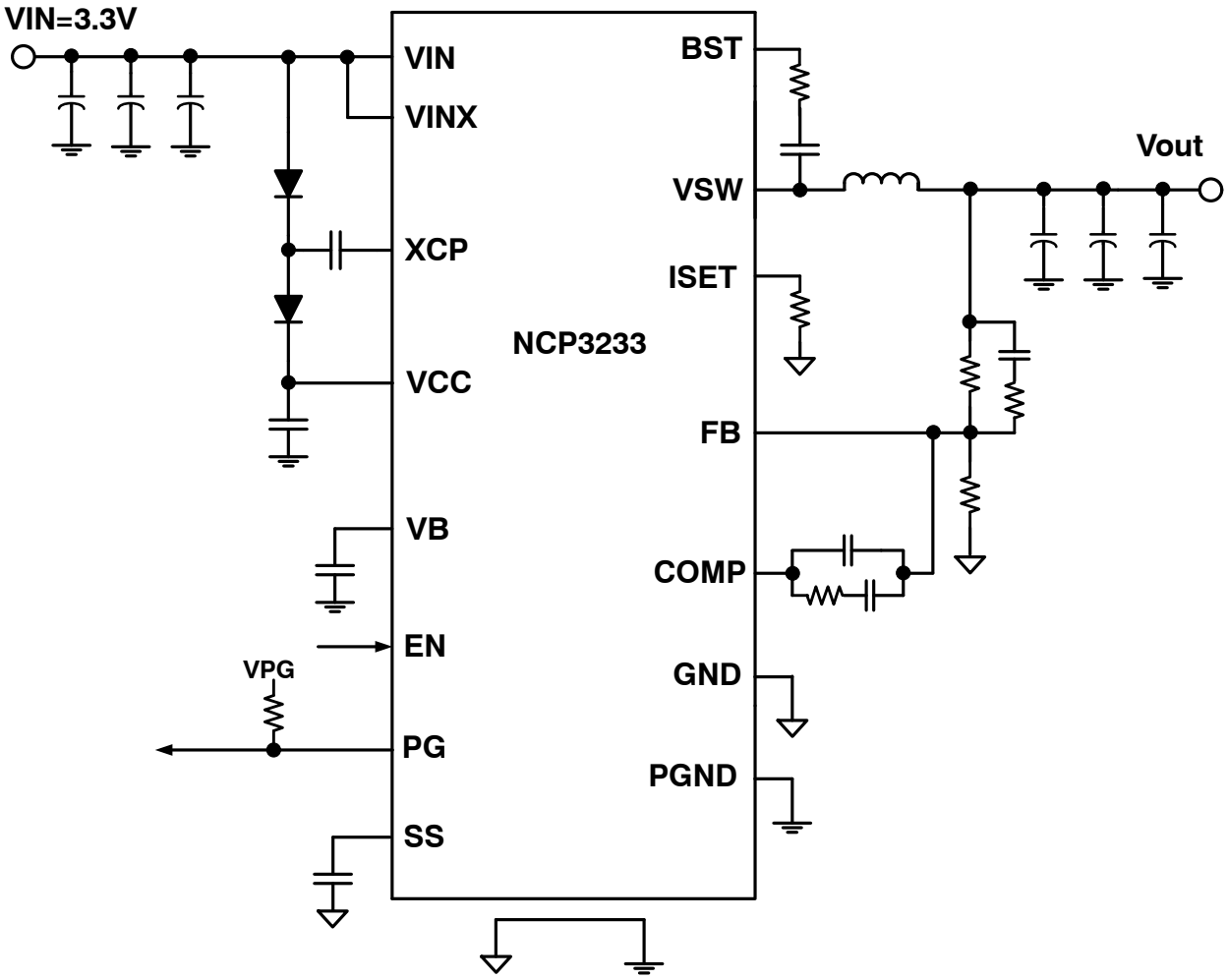


Figure 2. Typical Application Circuit for V_{IN} = 3.3 V

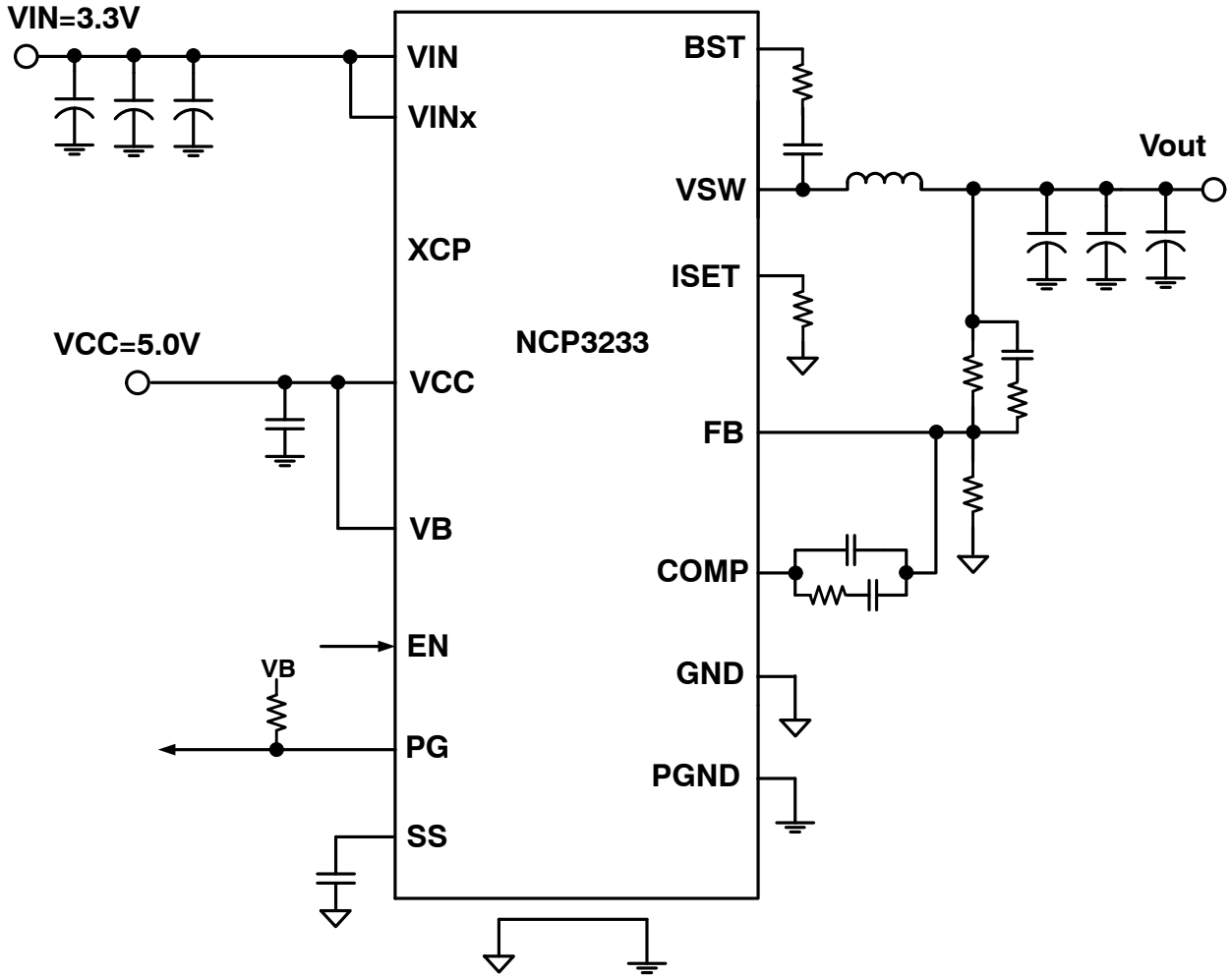


Figure 3. Typical Application Circuit for Separate Rail in System V_{IN} = 3.3 V and V_{CC} = 5 V

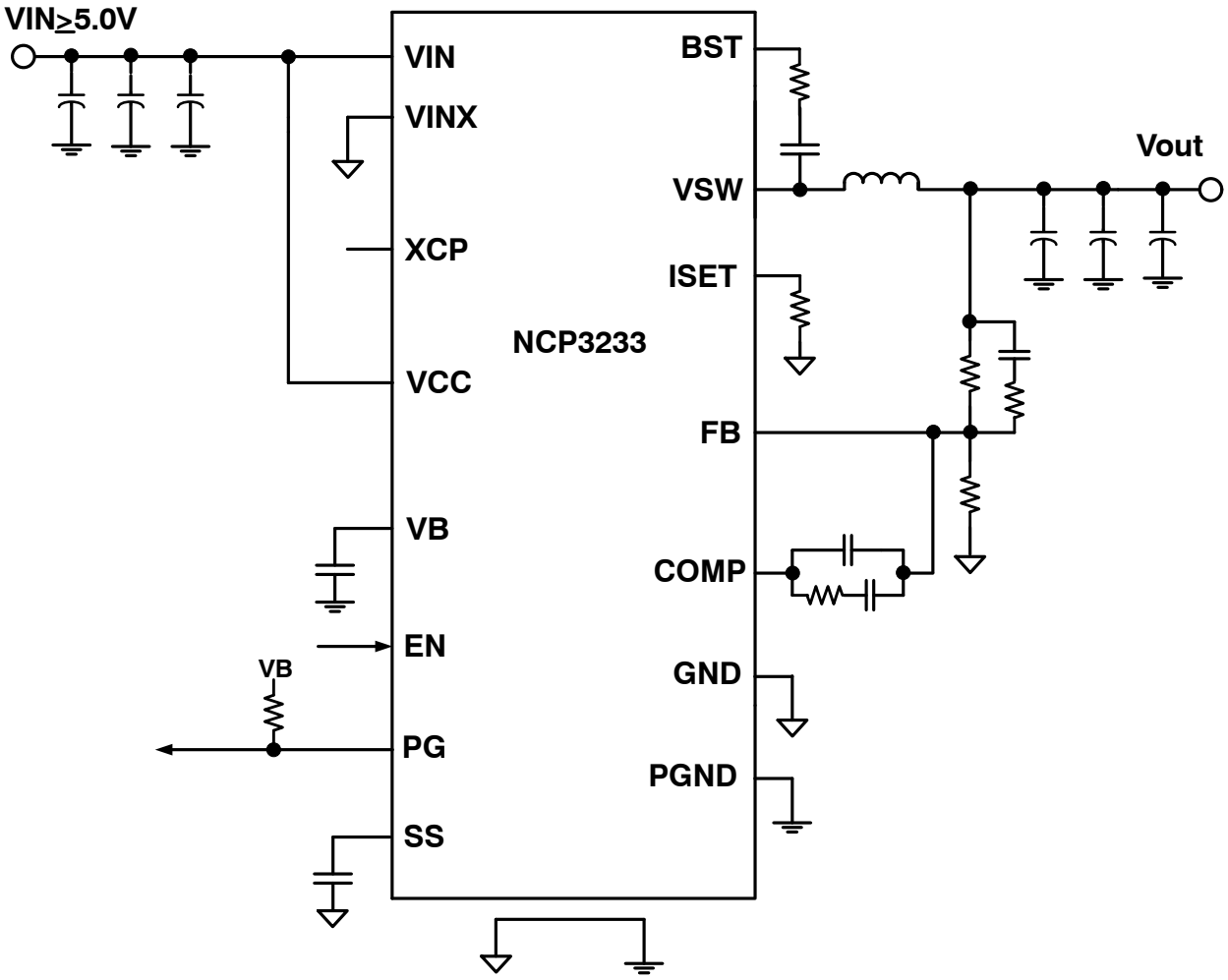


Figure 4. Typical Application Circuit for V_{IN} ≥ 5.0 V

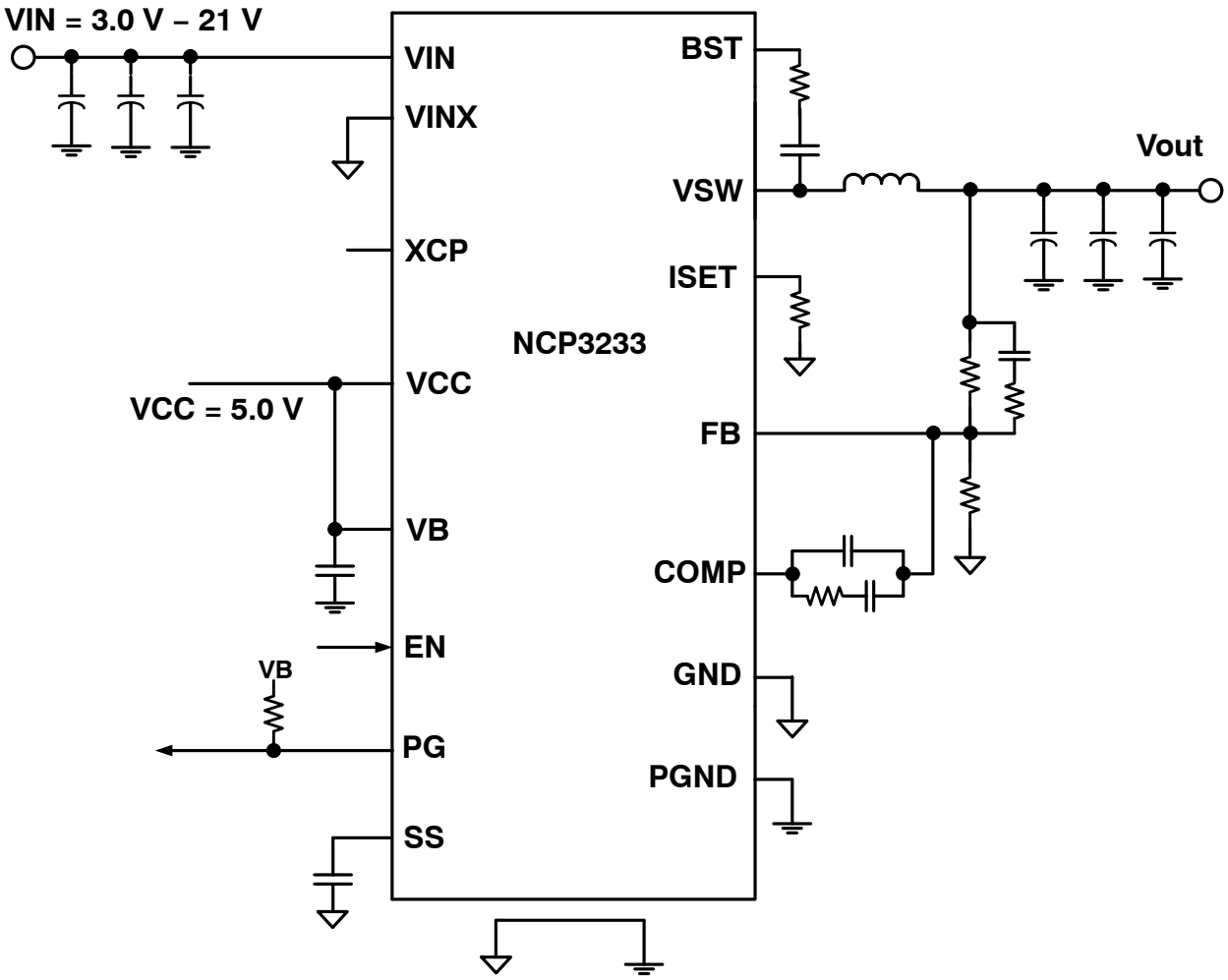


Figure 5. Typical Application Circuit for V_{IN} = 3.0 V – 21 V and V_{CC} = 5 V

ABSOLUTE MAXIMUM RATINGS (measured vs. GND pads, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply to GND	VIN, VCC (Note 1)	21 −0.3	V
VSW to GND	VSWH	23 −0.6 (DC) 28 (t < 50 ns) −5 (t < 50 ns)	V
BST to GND	BST	28 (DC) −0.6 (DC) 33 (t < 50 ns)	V
BST to VSW	VBST_SWH	6.5 (DC) −0.3 (DC)	V
VIN to VSW, VIN = VCC		−0.3 to 26 (DC) −4 (t < 50 ns)	V
All other pins		6.0 −0.3	V
Operating Ambient Temperature Range	T_A	−40 to +125	°C
Operating Junction Temperature Range (Note 1)	T_J	−40 to +125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Electrostatic Discharge − Human Body Model	HBM	1.0	kV
Electrostatic Discharge − Charged Device Model	CDM	2.0	kV
HS FET Junction−to−Case Thermal Resistance (Note 2)	$R_{\theta JC-HS}$	1.3	°C/W
LS FET Junction−to−Case Thermal Resistance (Note 2)	$R_{\theta JC-LS}$	0.6	°C/W
Junction−to−Ambient Thermal Resistance	$R_{\theta JA}$	35	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When VIN and VCC are connected together, VCC max value is 21 V.
2. $R_{\theta JC}$ thermal resistance is obtained by simulating a cold plate test on the exposed power pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30−88.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < +125°C, V_{IN} = V_{CC} = 12 V, for min/max values unless otherwise noted, T_J = +25°C for typical values)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VIN Operation Voltage	VIN		3.0		21	V
VINX Operation Voltage	VINX	VINX not connected to GND	3.0		5.5	V
VCC Operation Voltage	VCC	Vin ≥ 5 V	5.0		21	V
VB UVLO Threshold (Rising)			4.2	4.4	4.5	V
VB UVLO Threshold (Falling)			3.9	4.0	4.1	V
VINX UVLO Threshold (Rising)			2.7	2.9	3.05	V
VINX UVLO Threshold (Falling)			2.4	2.6	2.8	V
VINX UVLO Hysteresis				0.275		V
VB UVLO Falling Blanking Time				2		μs
VB Output Voltage	VB	V_{CC} = 6 V, 0 ≤ IB ≤ 40 mA	4.9	5.15	5.45	V
VB Dropout Voltage		IB = 25 mA, V_{CC} = 4.5 V		50	100	mV
VB Current Limit		V_{CC} = 12 V		100		mA
VCC Quiescent Current		EN = H, COMP = H, no switching; PG open		4.5	7	mA
Shutdown Supply Current		EN = 0; V_{CC} = 16 V; PG open		110	130	μA
		EN = 0; V_{CC} = 4.5 V; PG open		70	80	μA
XCP Frequency		V_{INx} = 3.3 V		250		kHz
XCP Drive Low Resistance		V_{INx} = 3.3 V		3.3		Ω
XCP Drive High Resistance		V_{INx} = 3.3 V		7.7		Ω
FEEDBACK VOLTAGE						
FB Input Voltage	V_{FB}	T_J = 25°C, 4.5 V ≤ V_{CC} ≤ 21 V	0.597	0.6	0.603	V
		−40°C < T_J < 125°C; 4.5 V ≤ V_{CC} ≤ 21 V	0.594	0.6	0.606	
Feedback Input Bias Current	IFB	V_{FB} = 0.6 V			75	nA
ERROR AMPLIFIER						
Open Loop DC Gain (GBD)			60	85		dB
Open Loop Unity Gain Bandwidth	F0dB,EA			24		MHz
Open Loop Phase Margin				60		°
Slew Rate		COMP pin to GND = 10 pF		2.5		V/μ
COMP Clamp Voltage, High			3.1	3.4	3.6	V
COMP Clamp Voltage, Low				0.5		V
Output Source Current		V_{FB} = 0 V	18			mA
Output Sink Current		V_{FB} = 1 V	20			mA
CURRENT LIMIT						
Low−side RDSON over ISET Current	RDSON/ISET	T_J = 25°C See OCP section for more information	56.5	59.0	61.5	Ω/A
Low−side ISET Current Source Temperature Coefficient	TC_LS_I−SET			+0.23		%/°C
Low−side OCP Switch−over Threshold				600		mV
Low−side Programmable OCP Range	LS_OCPth	Guaranteed by characterization			600	mV
High−side Fixed OCP	HS_OCP			30		A
HS OCP Min on time	HS_Tblnk			150		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (−40°C < T_J < +125°C, V_{IN} = V_{CC} = 12 V, for min/max values unless otherwise noted, T_J = +25°C for typical values)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CURRENT LIMIT						
LS OCP Blanking time	LS_Tblnk			150		ns
PWM						
Maximum duty cycle		f_{sw} = 500 kHz, V_{FB} = 0 V, V_{IN} = 5 V f_{sw} = 500 kHz, V_{FB} = 0 V, V_{IN} = 12 V f_{sw} = 500 kHz, V_{FB} = 0 V, V_{IN} = 21 V Guaranteed by characterization	88 86 67	92 88 85		%
Minimum duty cycle		VCOMP < PWM Ramp Offset Voltage		0		%
Minimum GH on−time		Guaranteed by characterization		50	65	ns
PWM Ramp Amplitude		Feedforward Ramp V_{INx} = 0 V		V_{IN} / 5.4		V
		Feedforward Ramp V_{INx} = 3.3 V		V_{IN} / 1.4		
PWM Ramp Offset				0.63		V
OSCILLATOR						
Oscillator Frequency Range	f_{sw}	f_{sw} = 500 kHz, 3 V < V_{CC} < 21 V	450	500	550	kHz
Hiccup Time Duration	t_{hiccup}	f_{sw} = 500 kHz, t_{SS} > 1 ms f_{sw} = 500 kHz, t_{SS} < 1 ms		4*t_{ss} 4		ms
ENABLE INPUT (EN)						
EN Input Operating Range					5.5	V
Enable Threshold Voltage		VEN rising	1.13	1.2	1.27	V
Enable Hysteresis		VEN falling Guaranteed by characterization	60	140	210	mV
Deep Disable Threshold				0.8	1.1	V
Enable Pull−up Current				2		μA
SOFTSTART INPUT (SS)						
SS Start Delay	t_{SSD}		2.3	2.6	3.0	ms
SS End Threshold	SSEND			0.6		V
SS Source Current	I_{SS}		2.15	2.5	2.8	μA
VOLTAGE MONITOR						
Power Good Sink Current		PG = 0.15 V	9	12	17	mA
Output Overvoltage Rising			725	750	775	mV
Overvoltage Fault Blanking Time				5		μs
Output Under−Voltage Trip Threshold			500	525	550	mV
Under−voltage Protection Blanking Time				20		μs
UVP Enable Delay				t_{SS}		s
POWER STAGE						
High−side on Resistance	R_{DSONH}	−40°C < T_J < +125°C	2.8	4.8	6.7	mΩ
Low−side on Resistance	R_{DSONL}	−40°C < T_J < +125°C V_{GS} = 5.2 V, I_D = 20 A	0.9	2.0	3.9	mΩ
VFBOOT		IBOOT = 2 mA		0.2		V
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				25		°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

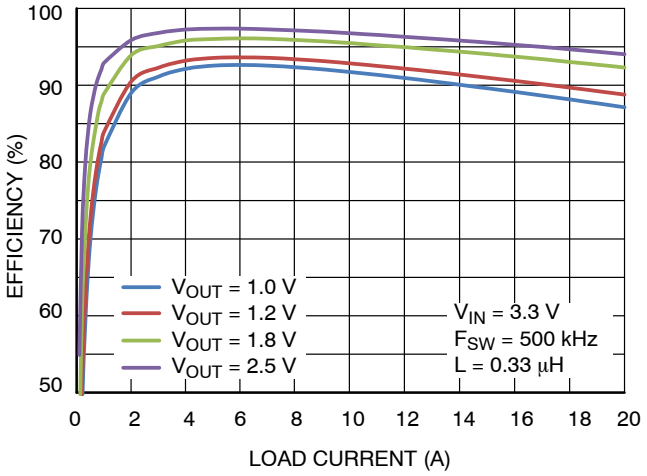


Figure 6. Efficiency vs. Load Current (V_{IN} = 3.3 V), Inductor: Wurth Electronics 7443320033

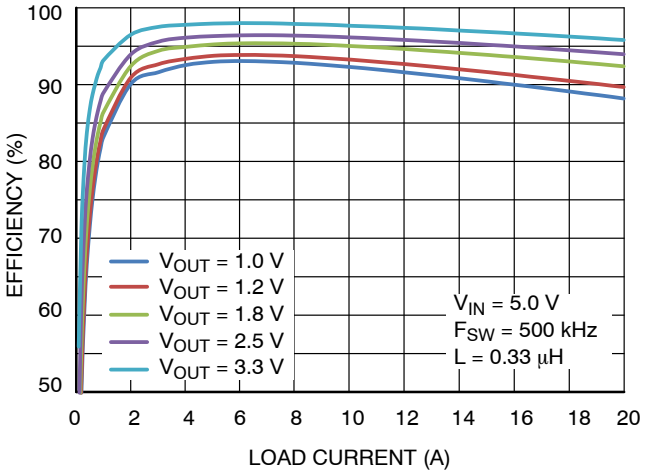


Figure 7. Efficiency vs. Load Current (V_{IN} = 5.0 V), Inductor: Wurth Electronics 7443320033

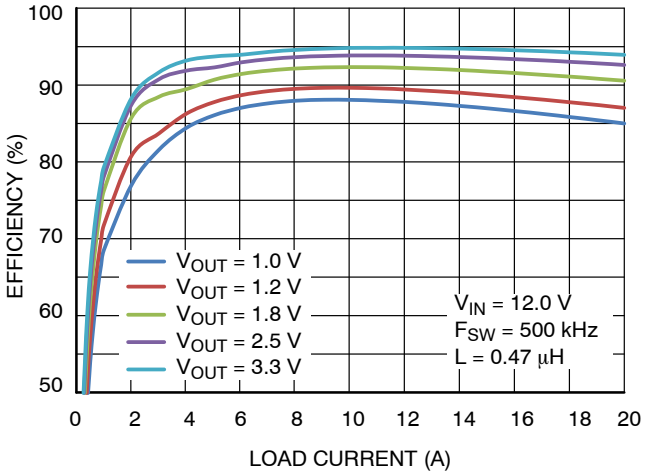


Figure 8. Efficiency vs. Load Current (V_{IN} = 12.0 V), Inductor: Wurth Electronics 7443320047

TYPICAL CHARACTERISTICS

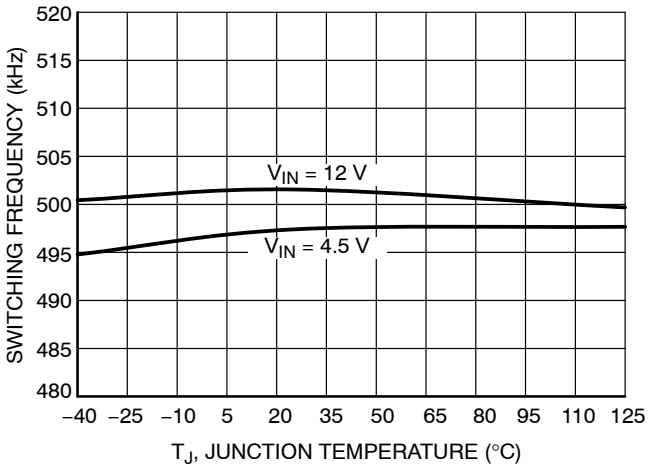


Figure 9. Switching Frequency vs. Junction Temperature

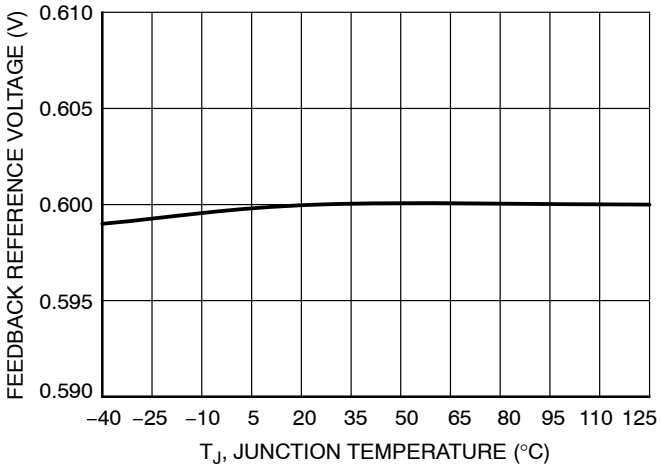


Figure 10. Feedback Reference Voltage vs. Junction Temperature (V_{IN} = 4.5 V and 12 V)

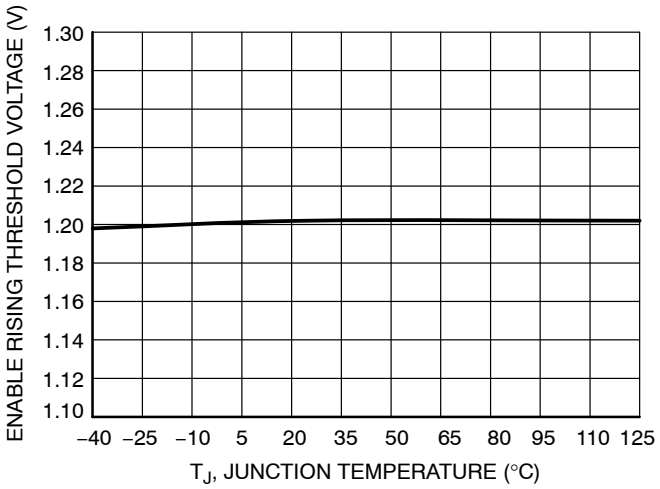


Figure 11. Enable Rising Threshold Voltage vs. Junction Temperature

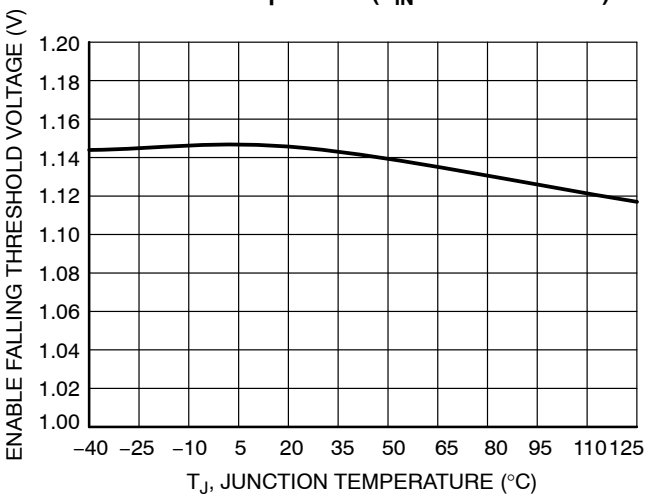


Figure 12. Enable Falling Threshold Voltage vs. Junction Temperature

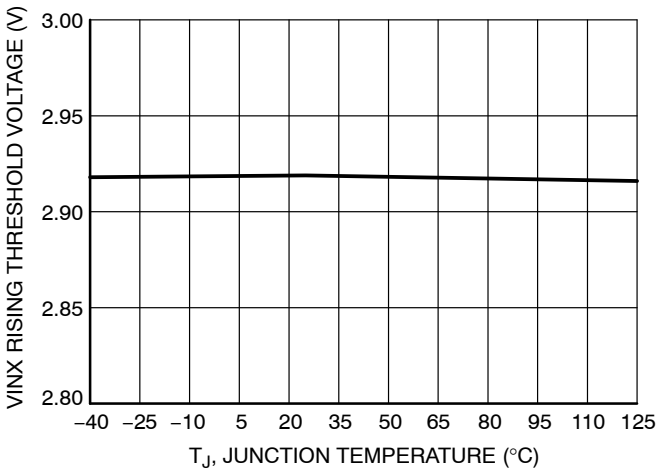


Figure 13. VINX Rising Threshold Voltage vs. Junction Temperature

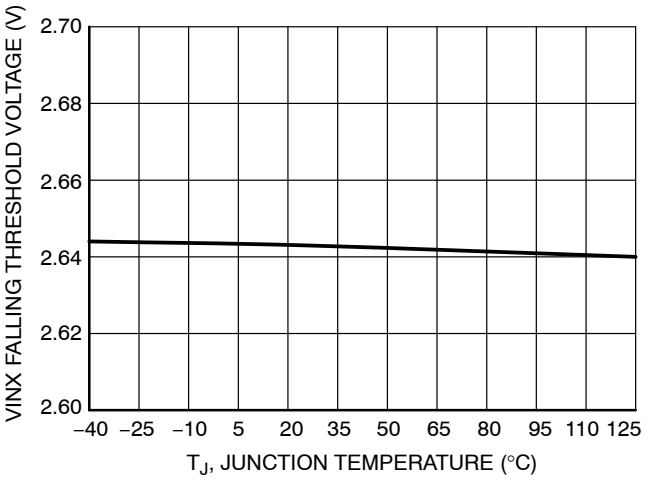


Figure 14. VINX Falling Threshold Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

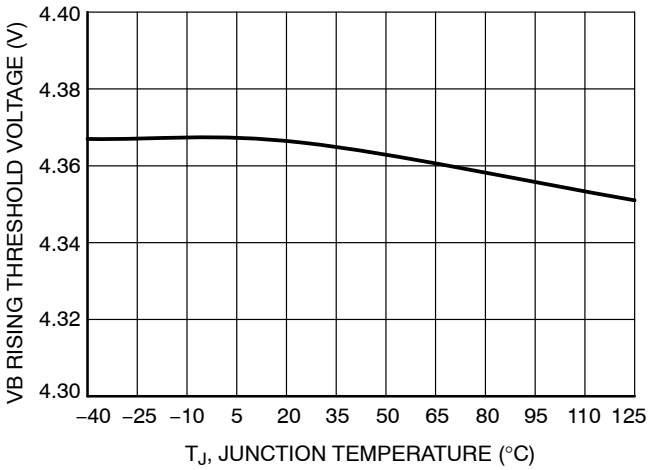


Figure 15. VB Rising Threshold Voltage vs. Junction Temperature

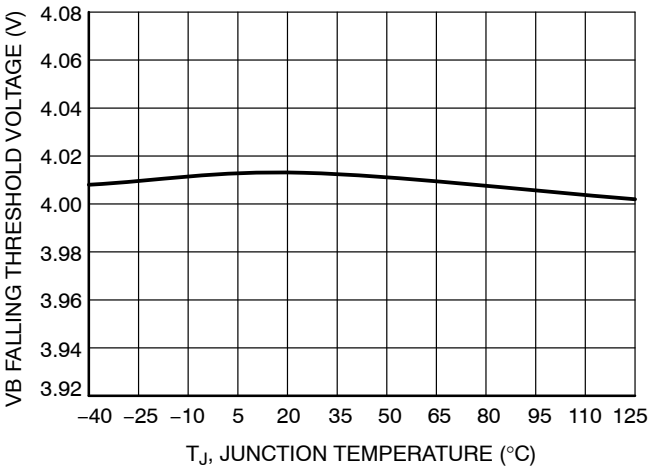


Figure 16. VB Falling Threshold Voltage vs. Junction Temperature

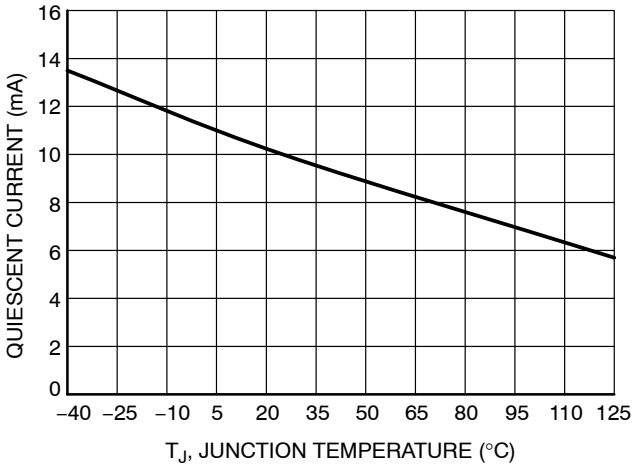


Figure 17. Quiescent Current vs. Junction Temperature (V_{CC} = 12 V, No Switching)

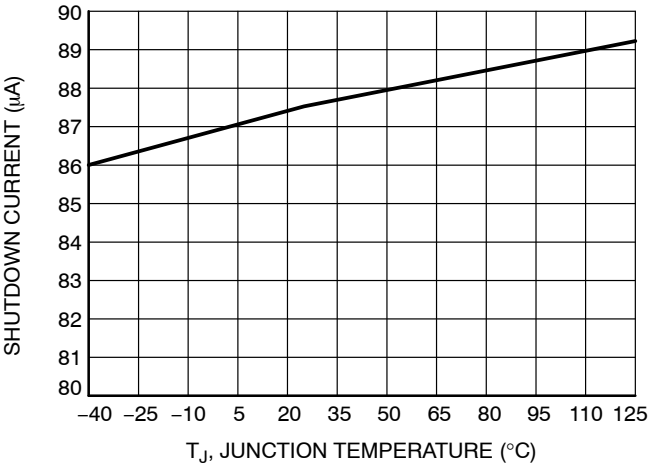


Figure 18. Shutdown Current vs. Junction Temperature (V_{IN} = 12 V)

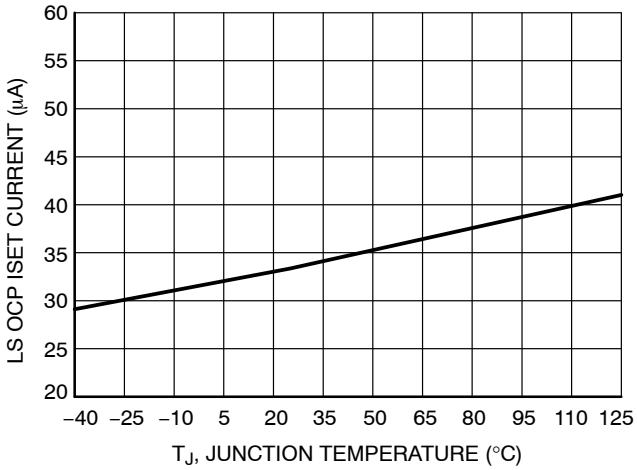


Figure 19. LS OCP ISET Current vs. Junction Temperature

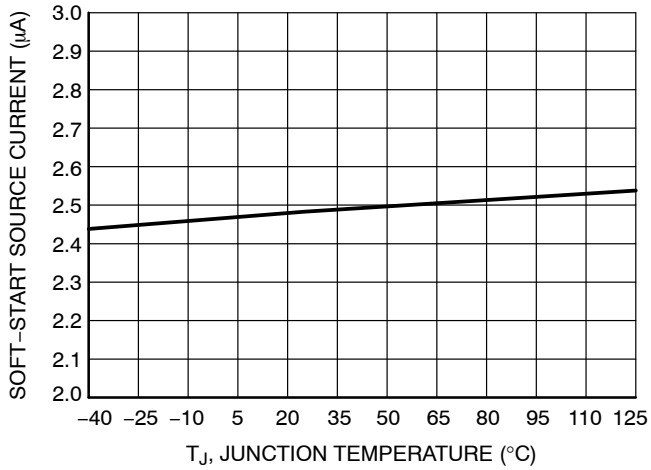


Figure 20. Soft−Source Current vs. Junction Temperature

OPERATION DESCRIPTION

Overview

The NCP3233 is a 500 kHz fixed switching frequency, high efficiency, and high current PWM synchronous buck converter with a wide range of input voltage. It operates with a single supply voltage from 3.0 V to 21 V and provides output current as high as 20 A. NCP3233 utilizes voltage mode control with input voltage feed−forward to provide for easier compensation over the supply range of the converter. For 3.3 V input voltage applications, with pin VINX connected to pin VIN it enables an internal charge pump to boost input voltage high enough to supply the internal LDO and internal circuits. The internal charge pump's operating frequency is 250 kHz to reduce its power consumption. For 5.0 V or higher input voltage applications, with pin VINX connected to GND, it disables the internal charge pump to optimize the overall efficiency. The device also includes pre−bias start−up capability to allow monotonic startup in the event of a pre−biased output condition.

Protection features include over current protection (OCP), output over and under voltage protection (OVP, UVP), and internal thermal shut down (TSD) and power good indicator. The enable function is highly programmable to allow for adjustable startup voltages at higher input voltages. There is also an SS pin for user to adjust the soft start time.

Reference Voltage

The NCP3233 incorporates an internal reference that allows output voltages as low as 0.6 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

Oscillator / Ramp

The ramp waveform is a saw tooth form at the PWM frequency with a peak−to−peak amplitude of VCC/5.4 and VCC/1.4, offset from GND by 0.7 V. The PWM duty cycle is limited to a maximum of 92%, allowing the bootstrap capacitors to charge during each cycle.

Error Amplifier

The error amplifier's primary function is to regulate the converter's output voltage using a resistor divider connected from the converter's output to the FB pin of the controller, as shown in the Applications Schematic. A type III compensation network must be connected around the error amplifier to stabilize the converter. It has a bandwidth of greater than 24 MHz, with open loop gain of at least 60 dB.

Programmable Soft−Start

An external capacitor connected from the SS pin to ground sets up the soft−start period, which can limit the start−up inrush current. The soft−start period can be programmed based on the following equations:

$$t_{SS} = \frac{C_{SS} \times V_{ref}}{I_{SS}} \qquad \text{(eq. 1)}$$

OCP is the only fault that is active during a soft−start.

Adaptive Non−Overlap Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET freewheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. NCP3233 implements adaptive dead time control to minimize the dead time, as well as preventing shoot through.

Pre−bias Startup

In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residue charge or the converter's output may be held up by a low current standby power supply. NCP3233 supports pre−bias startup by holding off switching until the output voltage rises above the set regulated voltage. If the pre−bias voltage is higher than the set regulated voltage, switching does not occur until the output voltage drops back to the regulation point.

Precision Enable (EN)

The ENABLE block allows the output to be toggled on and off and is a precision analog input.

When the EN voltage exceeds V_EN, the controller will initiate the soft−start sequence as long as the input voltage and sub−regulated voltage have exceeded their UVLO thresholds. V_EN_hyst helps to reject noise and allow the pin to be resistively coupled to the input voltage or sequenced with other rails.

If the EN voltage is held below 0.8 V, the NCP3233 enters a deep shutdown state where the internal bias circuitry is off. As the voltage at EN continues to rise, the Enable comparator and reference are active and provide a more accurate EN threshold. The drivers and charge pump are held off until the rising voltage at EN crosses V_EN.

An internal 2 μA pullup automatically enables the device when the EN pin is left floating.

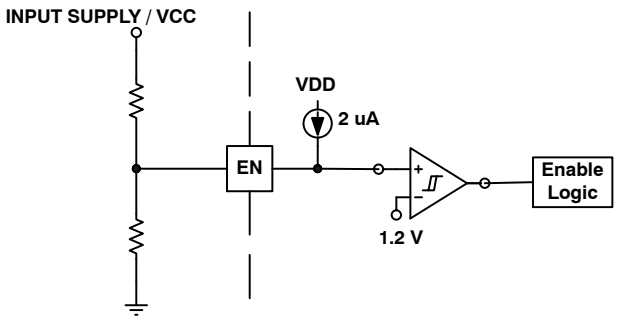


Figure 21.

PROTECTION FEATURES

Under Voltage Protection (UVP)

A UVP circuit monitors the VFB voltage to detect an undervoltage event. If the VFB voltage is below this threshold for more than 20 μs, a UVP fault is set and the device will enter hiccup mode. (See below)

Over Voltage Protection (OVP)

Two−stage recoverable overvoltage protection scheme is used in NCP3233. If FB pin voltage is higher than 690 mV, the part enters stage I. In this stage, the control loop tends to regulate the output voltage by turning off the HS MOSFET and turning on the LS MOSFET to discharge the output voltage. In stage I, the PG is still kept high. If FB pin voltage is higher than 750 mV, the part enters stage II, and it keeps LS MOSFET ON to discharge the output voltage and protects the load, and the PG is pulled low. If the output voltage returns to the nominal value, the loop is enabled again and PG is pulled high. The control loop naturally takes over to make sure that the part returns to normal operation.

Power Good Monitor (PG)

NCP3233 monitors the output voltage and signal when the output is out of regulation or during a non−regulated pre−bias condition, or fault condition. When the output voltage is within the OVP and UVP thresholds, the power good pin is a high impdence output. If the NCP3233 detects an OCP, OVP, UVP, TSD or is in soft start, the PG pin it pulls PG pin low. The PG pin is an open drain output and sink up to 5 mA.

Over Current Protection (OCP)

The NCP3233 overcurrent scheme senses the high−side MOSFET current for high side overcurrent protection. The high−side MOSFET drain to source voltage is compared against a preset voltage reference. Once the overcurrent protection is triggered, the protection scheme will do cycle−by−cycle limitation to protect the device. It also senses the freewheeling current in the low−side MOSFET after a blanking time of 150 ns. The low−side MOSFET drain to source voltage is compared against the voltage of an internal temperature compensated current source and a user−selected resistor RSET. The value of RSET for a given OCP level is defined by the follow equation:

$$RSET = \frac{i_{LS} \times RDSON \times 5}{i_{SET}} \quad \text{(eq. 2)}$$

In this equation, i_{LS} is the inductor peak current value, *RDSON* is the on resistance of low−side MOSFET, and i_{SET} is an internal current source used to compensate the temperature effects of on resistance of low−side MOSFET. NCP3233 can guarantee that $RDSON/i_{SET}$ is a constant value. By doing this, OCP accuracy won't be affected by the variation of MOSFET *RDSON*. In case RSET is not connected, the device switches the OCP threshold to a fixed 600 mV threshold.

After one OCP event is detected, the NCP3233 keeps the high−side MOSFET off until the low−side MOSFET falls below the trip point again and the high−side MOSFET turns on in the next clock cycle. So the low−side overcurrent protection shows pulse skipping behavior. An internal OCP counter will count up to 3 consecutive OCP events. After the third consecutive count, the device enters hiccup mode. The LSOCP scheme is described in Figure 22.

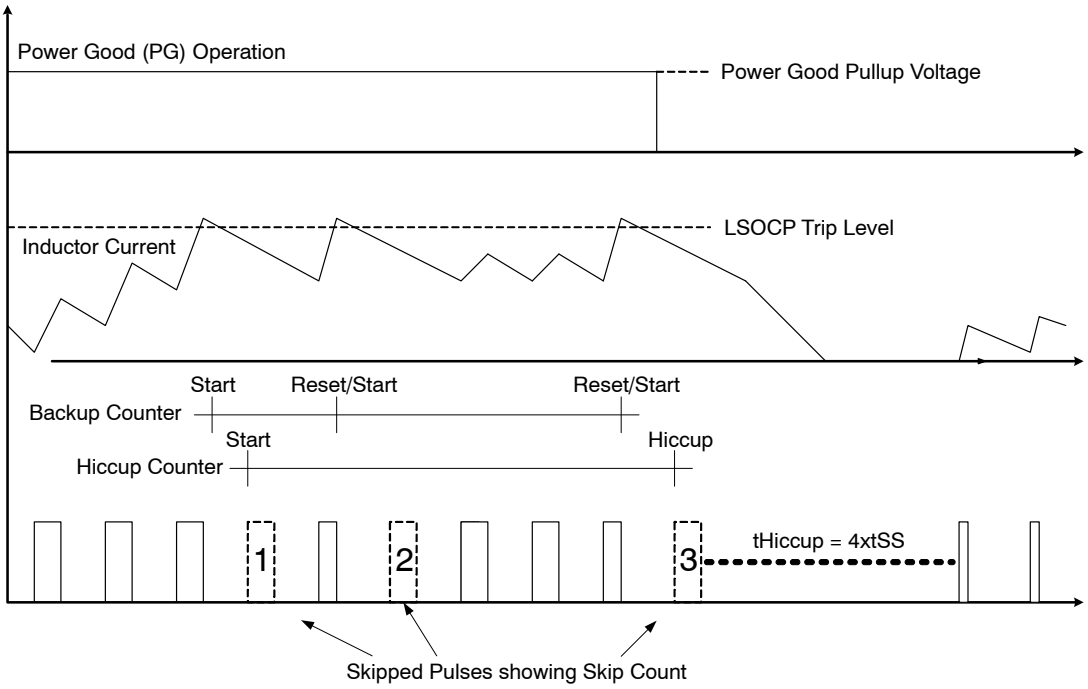


Figure 22. LSOCP Function with Counters and Power Good Shown (exaggerated for informational purposes)

Hiccup Mode

The NCP3233 utilizes hiccup mode for all of its fault conditions. After the fault conditions have been met, the NCP3233 turns off the high side and low side FET's and PG goes low. It waits for tHICCUP ms before reinitiating a soft−start. OVP and OCP are the active fault detections during the hiccup mode soft−start.

Thermal Shutdown (TSD)

The NCP3233 protects itself from overheating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold both the upper and lower MOSFETs will be shut OFF. Once the temperature drops below the falling hysteresis threshold, the voltage at the COMP pin will be pulled below the ramp valley voltage and a hiccup will be initiated.

Application Note

When the input is 3.3 V or even at the minimum value 2.9 V and the load is heavy or is changing in step rapidly if the impedance of input power supply is not optimized, it can generate enough voltage drop to trigger input voltage UVLO. In these applications, **the input inductance should be minimized, and input capacitance should be sufficient for the biggest step load current.**

In case that the input inductor is a must due to other requirement and input capacitance are limited, an R/C filter patch on the VINX pin can prevent VINX UVLO protection from being trigged, when VIN voltage valley drops below UVLO threshold 2.6 V during the transient of large step up load current. As shown in the Figure, R is 1 or 2 ohms, while C is selected by the needs of the filtering, usually 1 or 2 pieces of 22 μF MLCC.

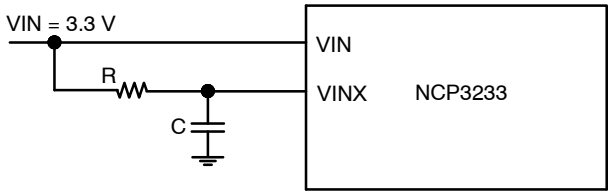


Figure 23.

Layout Guidelines

When laying out a power PCB for the NCP3233 there are several general key points and special key points to consider.

General layout guide: these are the common techniques for high frequency high power board layout design.

Base component placement: High current path components should be placed to keep the current path as tight as possible. Placement of components on the bottom of the board such as input or output decoupling can add loop inductance.

Ground Return for Power and Signals: Solid, uninterrupted ground planes must be present and adjacent to the high current path.

Copper Shapes on Component Layers: Large copper planes on one or multiple layers with adequate vias will increase thermal transfer, reduce copper conduction losses, and minimize loop inductance. Greater than 20 A designs require 2~3 layer shapes or more, increasing the number of layers will only improvement performance.

Via Placement for Power and Ground: Place enough vias to adequately connect outer layers to inner layers for thermal transfer and to minimize added inductance in layer transition. Multiple vias should be placed near important components like input ceramics and output ceramic capacitors.

Key Signal Routes: Do not route sensitive signals, such as FB near or under noisy nets such as the switch node VSW and BST node, to reduce noise coupling effects on the sensitive lines.

Special layout guide: please pay attention to the special requirement of layout guide.

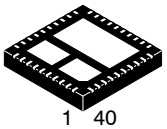
To improve the Low−side OCP accuracy, users should use single ground connection instead of separate analog ground and power ground. Make sure that the inner layers (at least 2nd layer, 3rd layer and 4th layer) are dedicated for ground plane. For thermal improvement, add vias as many as possible to connect top layer to bottom layer and inner layers. Keep copper pour of GND large, continuous and not interrupted by other traces, which may affect the heat transfer.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

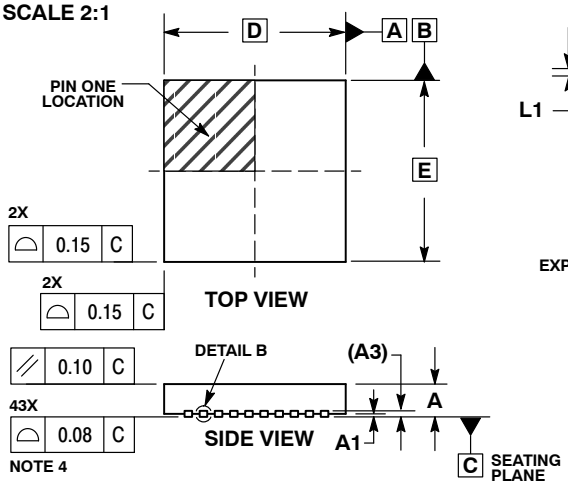
ON Semiconductor®

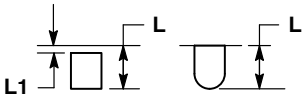
QFN40 6x6, 0.5P
CASE 485AZ−01
ISSUE O

DATE 09 JAN 2009

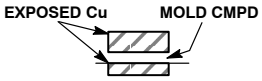


SCALE 2:1

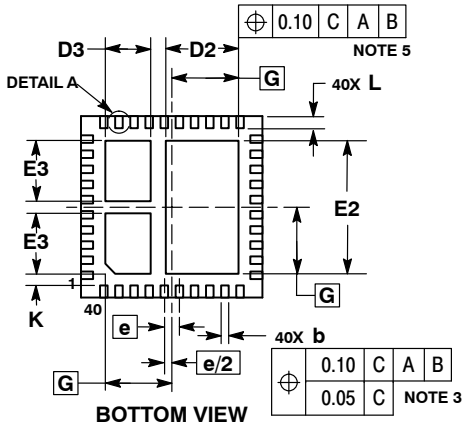




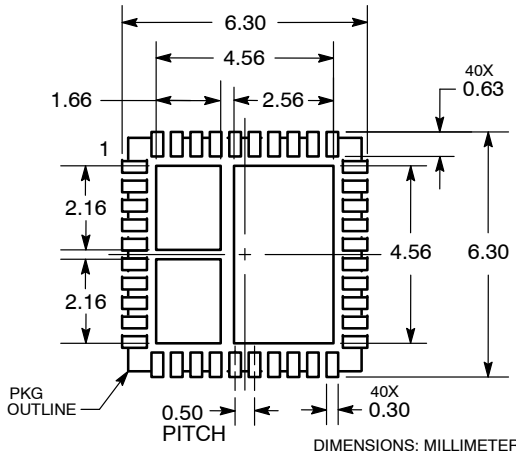
DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION



SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	−−−	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.30	2.50
D3	1.40	1.60
E	6.00 BSC	
E2	4.30	4.50
E3	1.90	2.10
e	0.50 BSC	
G	2.20 BSC	
K	0.20	−−−
L	0.30	0.50
L1	−−−	0.15

GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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