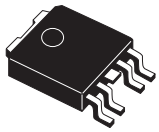
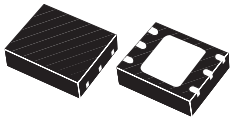
LD49150

1.5 A ultra low-dropout voltage regulator

Datasheet - production data



PPAK



DFN6 (3x3 mm)

Features

- Input voltage range:
  - V_I = 1.4 V to 5.5 V
  - V_{BIAS} = 3 V to 6 V
- Stable with ceramic capacitors
- ±1.5% initial tolerance
- Maximum dropout voltage (V_I - V_O) 200 mV over the operating temperature range
- Adjustable output voltage starting from 0.8 V
- Fast transient response (up to 10 MHz bandwidth)
- Excellent line and load regulation specifications
- Logic-controlled shutdown option
- Thermal shutdown and current limit protection
- Junction temperature range: - 25 °C to 125 °C

Applications

- Graphics processors
- PC add-in cards
- Microprocessor core voltage supply
- Low voltage digital ICs
- High efficiency linear power supplies
- SMPS post regulators

Description

The LD49150 is a high-bandwidth, low-dropout, 1.5 A voltage regulator, ideal for powering core voltages of low power microprocessors. The LD49150 implements a dual supply configuration, which guarantees a very low output impedance and a very fast transient response. The LD49150 requires a bias input supply and a main input supply, allowing ultra-low input voltages on the main supply rail. The input supply operates from 1.4 V to 5.5 V and the bias supply requires between 3 V and 6 V to work properly. The LD49150 offers fixed output voltages from 0.8 V to 1.8 V and adjustable output voltages starting from 0.8 V. The LD49150 requires a minimum output capacitance for stability, and works optimally with small ceramic capacitors.

Table 1. Device summary

Order codes		Output voltages
PPAK (tape and reel)	DFN6 (tape and reel) (1)	
LD49150PT08R		Adjustable from 0.8 V
LD49150PT10R	LD49150PU10R	1.0 V
LD49150PT12R	LD49150PU12R	1.2 V

1. Available on request.

Contents

1 Typical application circuits

Figure 1. Adjustable version

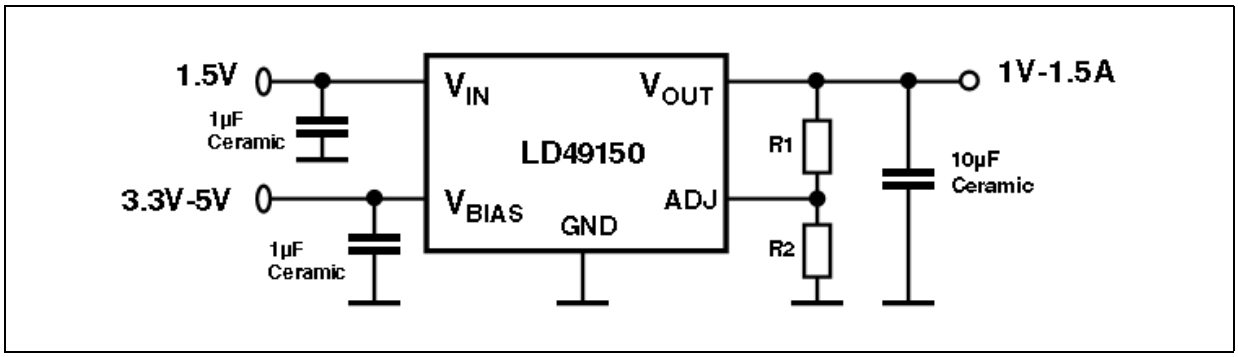
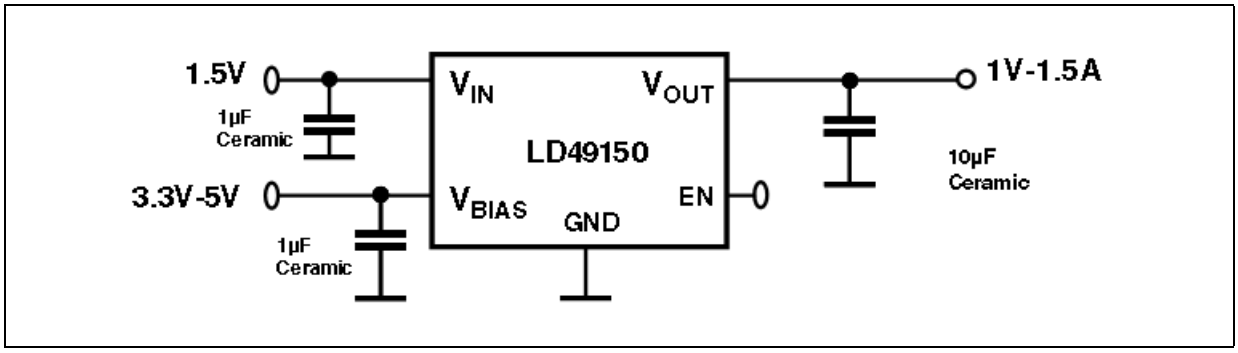


Figure 2. Fixed version with enable



2 Alternative application circuits

Figure 3. Single supply voltage solution

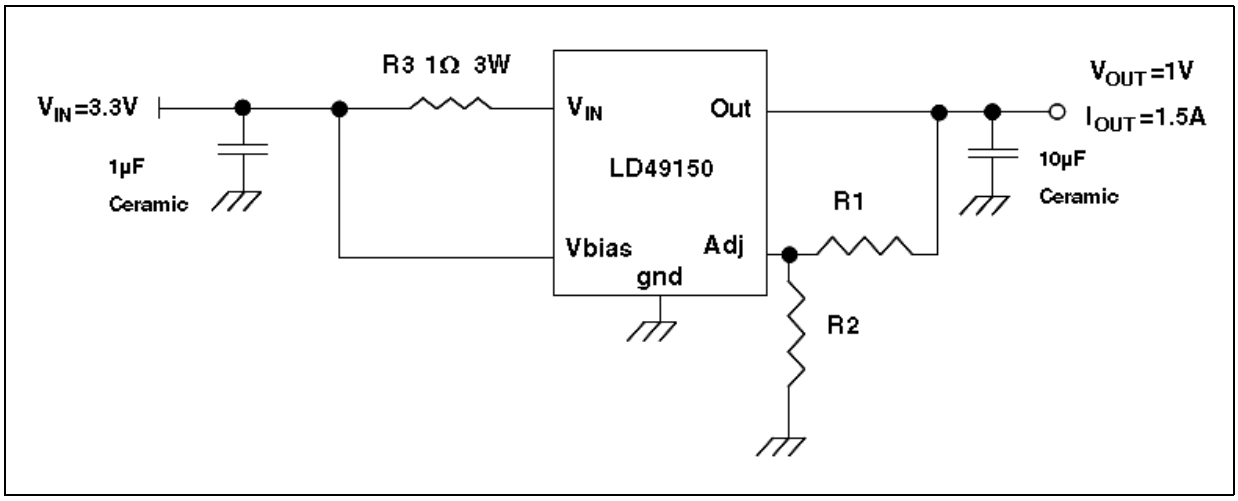
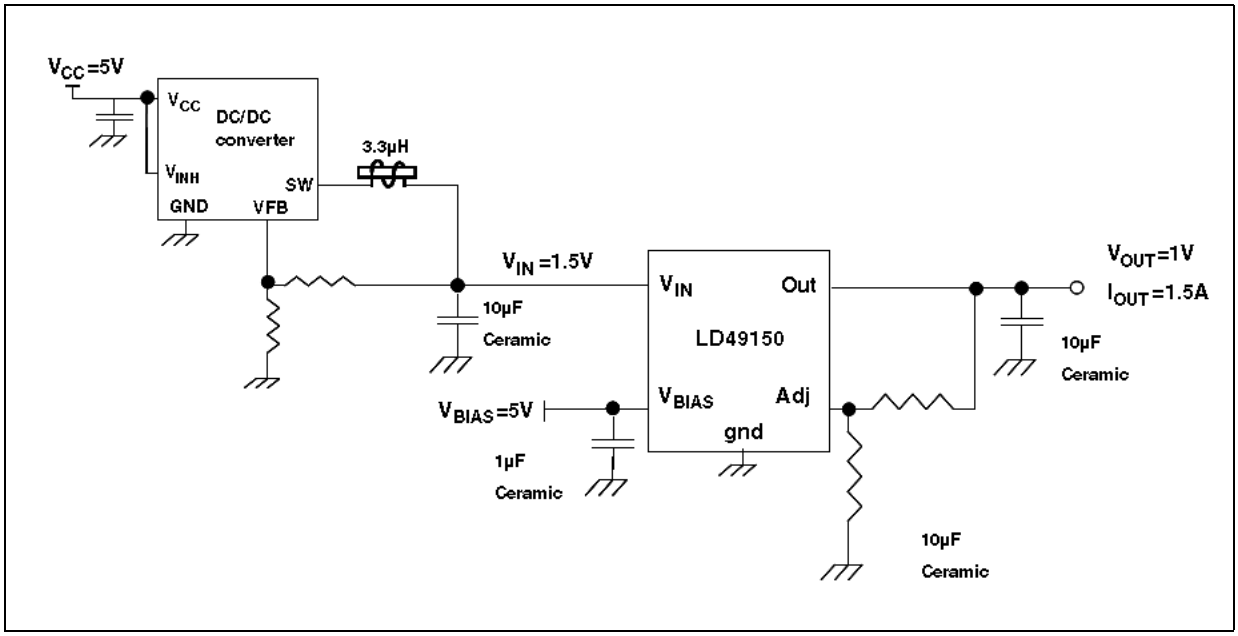
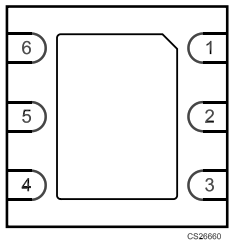


Figure 4. LD49150 and DC-DC pre-regulator to reduce power dissipation

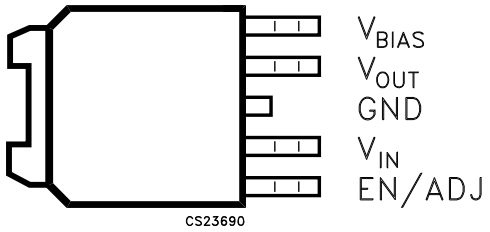


3 Pin configuration

Figure 5. Pin connections (PPAK top view, DFN bottom view)



DFN6 (3x3 mm)



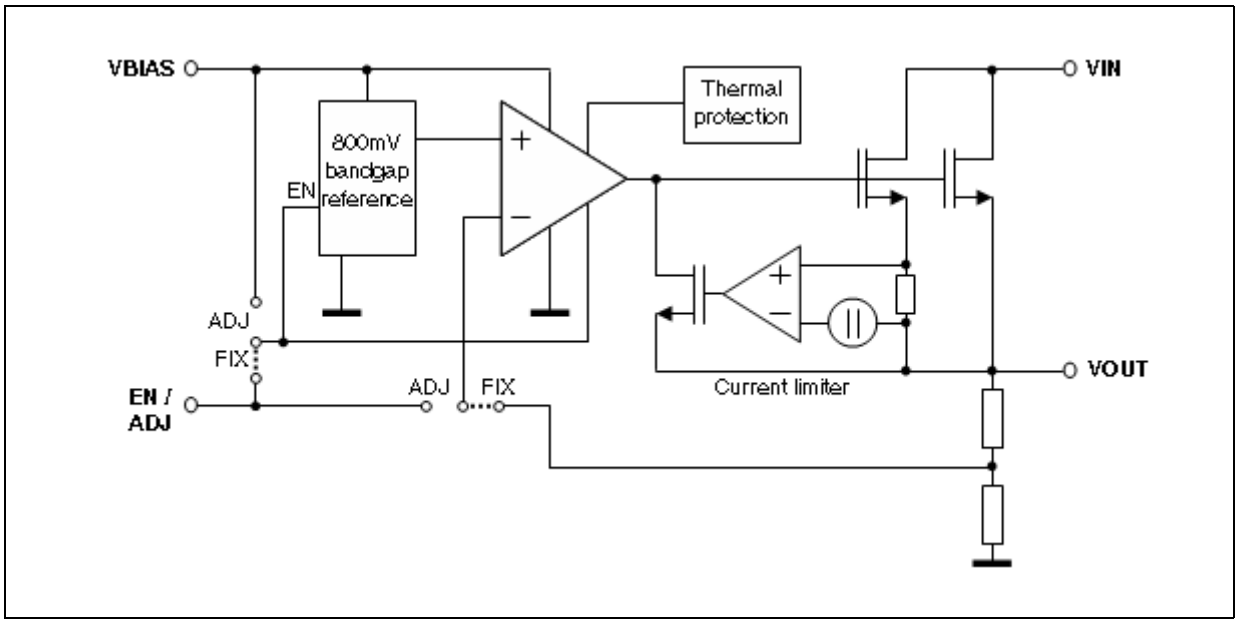
PPAK

Table 2. Pin description

PPAK pin	DFN pin	Symbol	Note
1	2	EN	Enable (input): logic high = enable, logic low = shutdown
		ADJ	Adjustable regulator feedback input connected to resistor voltage divider
2	3	V_{IN}	Input of the voltage regulator
3	1	GND	Ground (tab is connected to ground)
4	4	V_{OUT}	Regulator output
5	6	V_{BIAS}	Input bias voltage powers circuitry on the regulator with the exception of the output power device
	5	N.C.	Not connected

4 Diagram

Figure 6. Block diagram



5 Maximum ratings

Table 3. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	-0.3 to 7	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3 -0.3 to V_{BIAS} + 0.3	V
V_{BIAS}	Bias supply voltage	-0.3 to 7	V
V_{EN}	Enable input voltage	-0.3 to 7	V
P_D	Power dissipation	Internally limited	
T_{STG}	Storage temperature range	-50 to 150	°C

1. All values are referred to ground.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Operating ratings

Symbol	Parameter	Value	Unit
V_{IN}	Supply voltage	1.4 to 5.5	V
V_{OUT}	Output voltage	0.8 to 4.5	V
V_{BIAS}	Bias supply voltage	3 to 6	V
V_{EN}	Enable input voltage	0 to V_{BIAS}	V
T_J	Junction temperature range	-25 to 125	°C

6 Electrical characteristics

T_J = - 25 °C to 125 °C; V_{BIAS} = V_O + 2.1 V (1); V_I = V_O+1 V; V_{EN} = V_{BIAS}(2); I_O = 10 mA; C_I = 1 µF; C_O = 10 µF; C_{BIAS} = 1 µF; unless otherwise specified. Typical values refer to T_J = 25 °C.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage accuracy	T_J = 25 °C, fixed voltage option	-1.5		1.5	%
		T_J = -25 °C to 125 °C	-3		3	
V_{LINE}	Line regulation	V_I = V_O + 1 V to 5.5 V	-0.1		0.1	%/V
V_{LOAD}	Load regulation	I_L = 0 mA to 1.5 A, V_{BIAS} ≥ 3 V			1	%
V_{DROP}	Dropout voltage (V_I - V_O)	I_L = 1.5 A			200	mV
V_{DROP}	Dropout voltage (V_{BIAS}- V_O)	I_L = 1.5 A(1)		1.5	2.1	V
I_{GND}	Ground pin current	I_L = 0 mA		4	6	mA
		I_L = 1.5 A		4	6	
I_{GND_SHD}	Ground pin current in shutdown	V_{EN} ≤ 0.4 V(2)			5	µA
I_{VBIAS}	Current through V_{BIAS}	I_L = 0 mA		3	5	mA
		I_L = 1.5 A		3	5	
I_L	Current limit	V_O = 0 V	2.5			A
Enable input(2)						
V_{EN}	Enable input threshold (fixed voltage only)	Regulator enable	1.4			V
		Regulator shutdown			0.4	
I_{EN}	Enable pin input current			0.1	1	µA
Reference						
V_{REF}	Reference voltage	T_J = 25 °C	0.788	0.8	0.812	V
		T_J = -25 °C to 125 °C	0.776	0.8	0.824	
SVR	Supply voltage rejection	V_I = 2.5 V ± 0.5 V, V_O = 1 V, F = 120 Hz, V_{BIAS} = 3.3 V		68		dB

1. For V_O ≤ 1 V, V_{BIAS} dropout specification is not applied due to 3 V minimum V_{BIAS} input.
2. Fixed output voltage version only.

7 Typical characteristics

Figure 7. Reference voltage vs. temperature

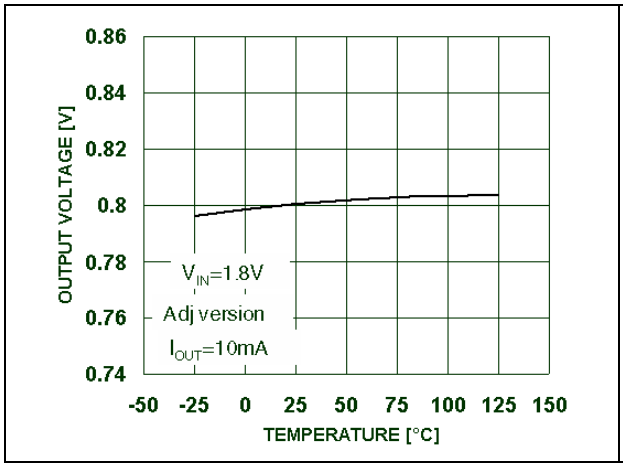


Figure 8. Output voltage vs. temperature

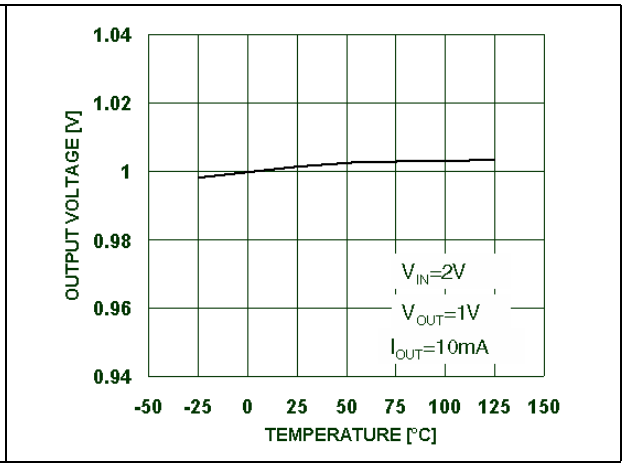


Figure 9. Load regulation vs. temperature

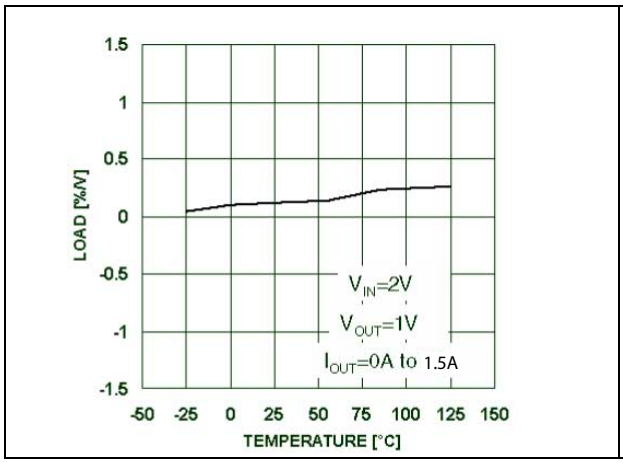


Figure 10. Line regulation vs. temperature

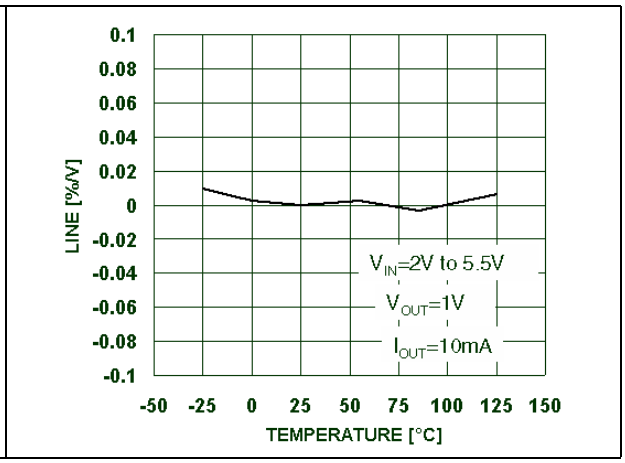


Figure 11. Output voltage vs. input voltage

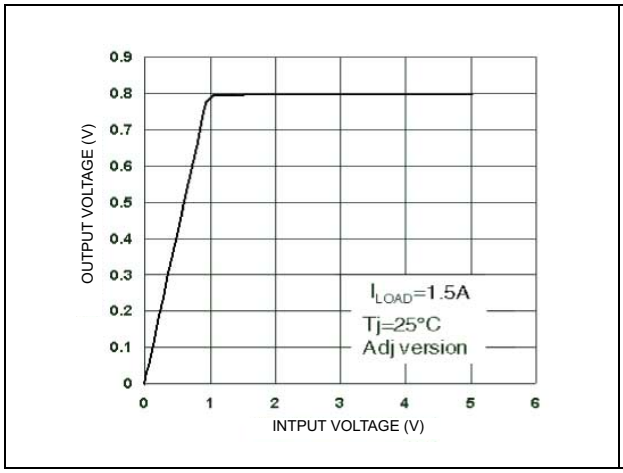


Figure 12. Dropout voltage (V_{IN}-V_{OUT}) vs. temperature

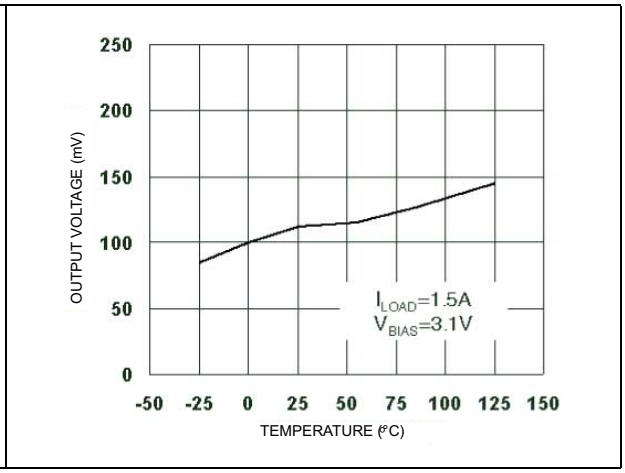


Figure 13. V_{BIAS} pin current vs. temperature

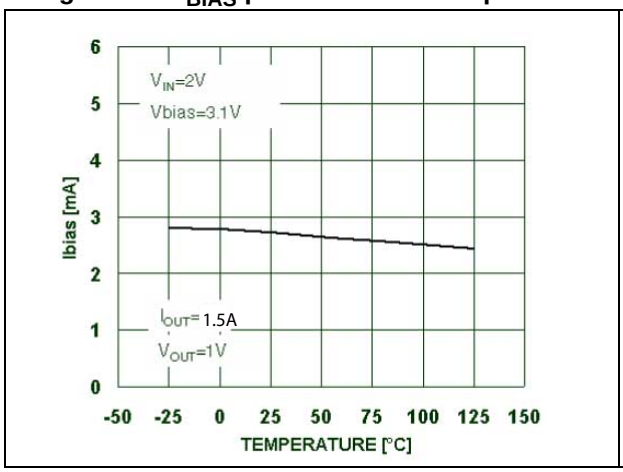


Figure 14. Noise vs. frequency

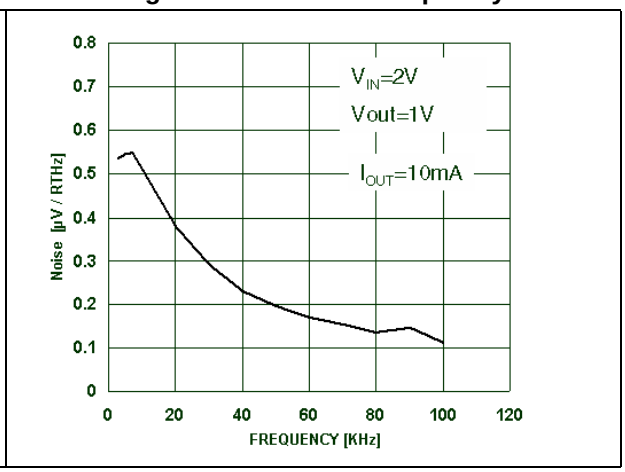


Figure 15. Quiescent current vs. temperature

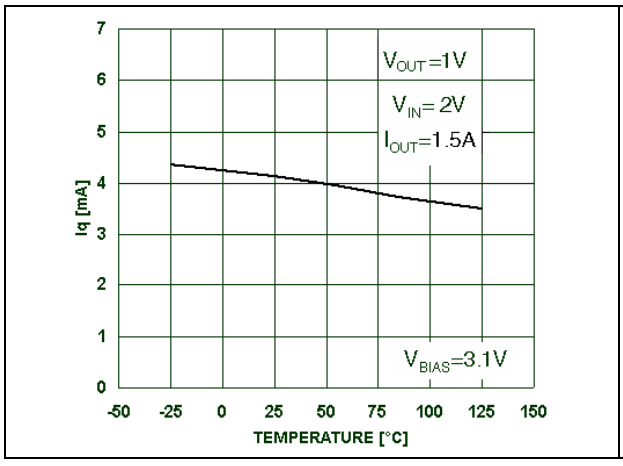


Figure 16. Supply voltage rejection vs. output current

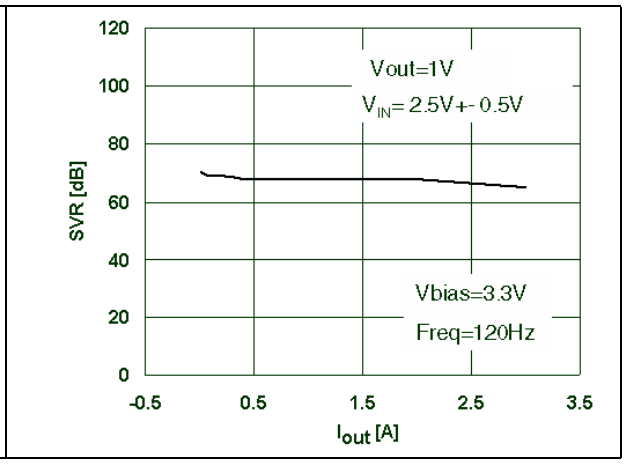


Figure 17. Stability region vs. C_{OUT} and high ESR

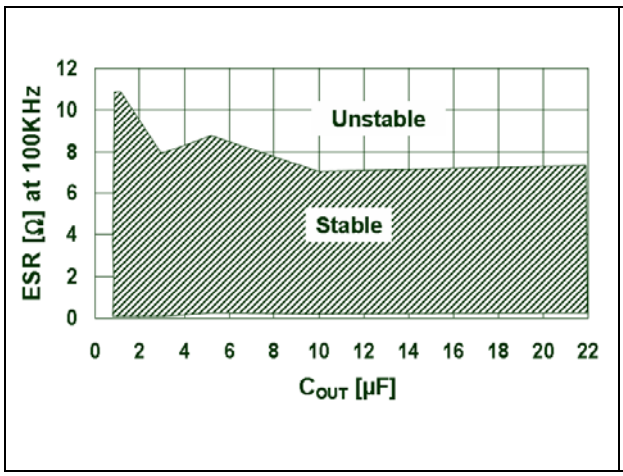


Figure 18. Stable region vs. C_{OUT} and low ESR

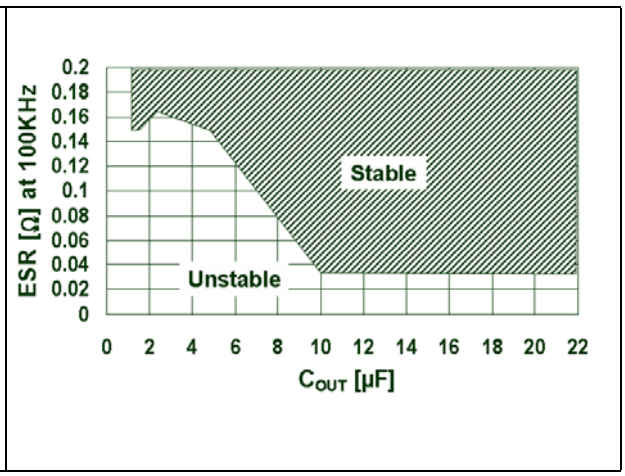
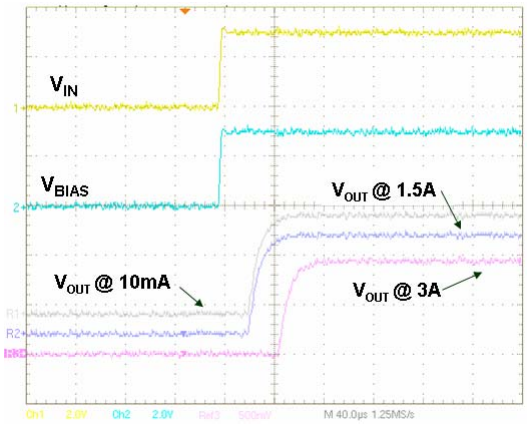
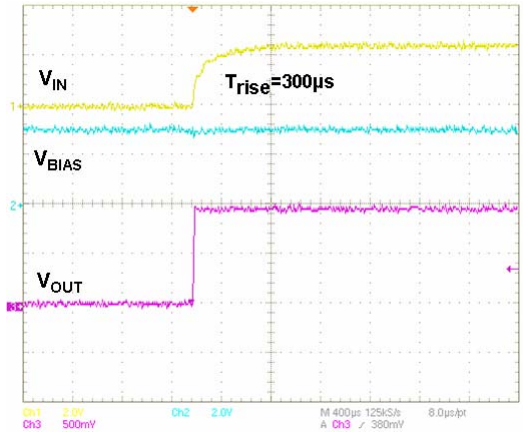


Figure 19. V_{BIAS} and V_{IN} start-up transient response (V_{IN} and V_{BIAS} startup at the same time)



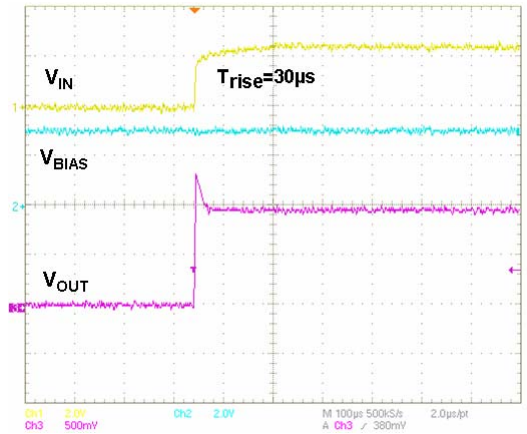
V_{IN}=V_{BIAS}=V_{EN}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 20. V_{IN} start-up transient response (V_{BIAS} startup before than V_{IN}) T_{rise} = 300 µs



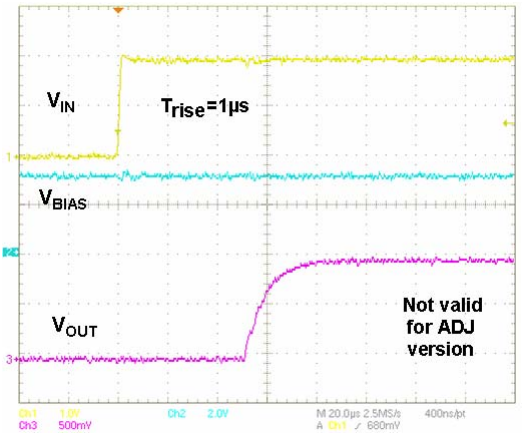
V_{IN}=2.5V, V_{BIAS}=V_{EN}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 21. V_{IN} start-up transient response (V_{BIAS} startup before than V_{IN}) T_{rise} = 30 µs



V_{IN}=2.5V, V_{BIAS}=V_{EN}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

Figure 22. V_{IN} start-up transient response (V_{BIAS} startup before than V_{IN} and V_{EN}=V_{IN})



V_{IN}=V_{EN}=2.5V, V_{BIAS}=3.1V, V_{OUT}=1V, C_{OUT}=1µF

8 Application hints

The LD49150 is a low-dropout linear regulator, designed for high-current applications requiring a fast transient response. The LD49150 has separate input and bias voltage ports, in order to reduce dropout voltage. Thanks to the LD49150, a minimum quantity of external components is required.

8.1 Input supply voltage (V_{IN})

V_{IN} provides the LD49150 with power input current. The minimum input voltage can be as low as 1.4 V, allowing conversion from very low voltage supplies to achieve low output voltage levels and low power dissipation.

8.2 Bias supply voltage (V_{BIAS})

The LD49150 control circuitry is supplied by V_{BIAS} pin, which requires a very low bias current (3 mA typ.) even at the maximum output current level (1.5 A). A bypass capacitor on V_{BIAS} pin improves the LD49150 performance during line and load transient. The small ceramic capacitor from V_{BIAS} to ground reduces high frequency noise that could be injected into the control circuitry. In typical applications, one ceramic chip capacitor of 1 µF may be used. V_{BIAS} input voltage has to be 2.1 V above the output voltage, with a minimum V_{BIAS} input voltage of 3 V.

8.3 External capacitors

To assure regulator stability, input and output capacitors are required as shown in *Section 1*.

8.4 Output capacitor

The LD49150 requires a minimum output capacitance to maintain stability. At least 1 µF ceramic chip capacitor is required. However, a specific capacitor selection assures the transient response. 1 µF ceramic chip capacitor satisfies most applications but 10 µF guarantees a better transient performance. In applications where V_{IN} level is close to the maximum operating voltage (V_{IN} > 4 V), a minimum 10 µF output capacitor avoids overvoltage stress on the input/output power pins during short-circuit conditions due to parasitic inductive effect. The output capacitor has to be as closer as possible to the LD49150 output pin. ESR output capacitor (equivalent series resistance) has to be within the stable region as shown in *Section 7*. Both ceramic and tantalum capacitors are suitable.

8.5 Minimum load current

The LD49150 does not require a minimum load to maintain the output voltage regulation.

8.6 Power sequencing recommendations

To assure the correct biasing and settling of the regulator internal circuitry during the start-up phase, and to avoid overvoltage spikes on the output, the correct power sequencing has to be provided.

As general rule, V_{IN} and V_{INH} signal timings should be chosen properly, so that they are applied to the device after V_{BIAS} voltage has already been settled on its minimum operative value (see *Section 8.2*). This can be achieved, for instance, by avoiding too slow V_{BIAS} rising edges (T_r >10 ms).

Provided that the above condition is satisfied, when fast V_{IN} transient input (T_r < 100 µs) is present, a smooth startup, with limited overvoltage on the output, can be achieved by V_{IN} and V_{BIAS} voltage simultaneously (refer to *Figure 20*, *Figure 21* and *Figure 22*).

In the fixed voltage version, overvoltage spikes can be reduced during very fast startup (T_r << 100 µs) by pulling V_{EN} pin up to V_{IN} voltage (see *Figure 23*).

8.7 Power dissipation/heatsinking

In relation to the maximum power dissipation and maximum ambient temperature of the application, a heatsink may be required. Junction temperature has to be within the specified range under operating conditions. The total power dissipation of the device is given by:

Equation 1

$$P_D = V_{IN} \times I_{IN} + V_{BIAS} \times I_{BIAS} - V_{OUT} \times I_{OUT}$$

where:

- V_{IN} = input supply voltage
- V_{BIAS} = bias supply voltage
- V_{OUT} = output voltage
- I_{OUT} = load current

The required θ_{SA} thermal resistance for the heatsink is given by the following formula:

Equation 2

$$\theta_{SA} = (T_J - T_A/P_D) - (\theta_{JC} + \theta_{CS})$$

T_{Rmax}, the maximum allowed temperature rise depends on T_{Amax}, the maximum ambient temperature of the application, and T_{Jmax}, the maximum allowable junction temperature:

Equation 3

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

θ_{JA}, the maximum allowable value for junction-to-ambient thermal resistance can be calculated as follows:

Equation 4

$$\theta_{JAmax} = T_{Rmax} / P_D$$

The thermal resistance depends on the amount of copper area or heatsink, and on the air flow. If $\theta_{JA}$the maximum allowable value is ≥ 100 °C/W for the PPAK package, no heatsink is

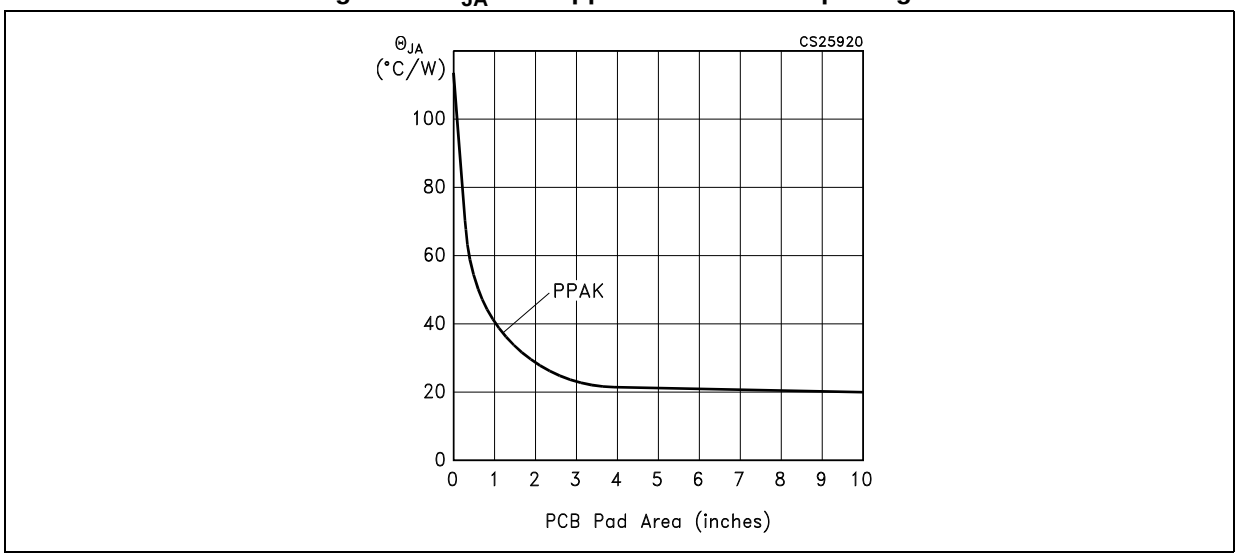
needed since the package can dissipate enough heat to satisfy these requirements. If the allowable θ_{JA} value falls below these limits, a heatsink is required as described below.

8.8 PPAK package heatsinking

The PPAK package uses the copper plane on the PCB as a heatsink. The tab of this package is soldered onto the copper plane for the heatsinking. PCB ground plane can be used as a heatsink. This area can be the inner GND layer of a multi-layer PCB, or, in a dual-layer PCB, it can be an unbroken GND area on the bottom layer, thermally connected to the tab through-via holes.

Figure 23 shows θ_{JA} curve for PPAK package for different copper area sizes, using a typical PCB: thickness 1/16 G10 FR4.

Figure 23. θ_{JA} vs. copper area for PPAK package



8.9 Adjustable regulator design

The LD49150 adjustable version allows the output voltage to be fixed anywhere between 0.8 V and 4.5 V using two resistors as shown in the typical application circuit. For example, to fix R_1 resistor value between V_{OUT} and ADJ pin, the resistor value between ADJ and GND (R_2) is calculated as follows:

$R_2 = R_1 [0.8/(V_{OUT} - 0.8)]$

where V_{OUT} is the desired output voltage.

R_1 values should be lower than 10 kΩ to obtain a better load transient performance. Higher values up to 100 kΩ are suitable.

8.10 Enable

The LD49150 fixed output voltage version features an active high enable input (EN) that allows the on-off control of the regulator. EN input threshold is guaranteed between 0.4 V and 1.4 V. The regulator is in shutdown mode when V_{EN} < 0.4 V and it is in operating mode (V_{OUT} activated) when V_{EN} > 1.4 V. If it is not in use, EN pin has to be tied directly to V_{IN} to keep the regulator continuously activated. En pin has not to be left with high impedance.

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 24. PPAK drawing

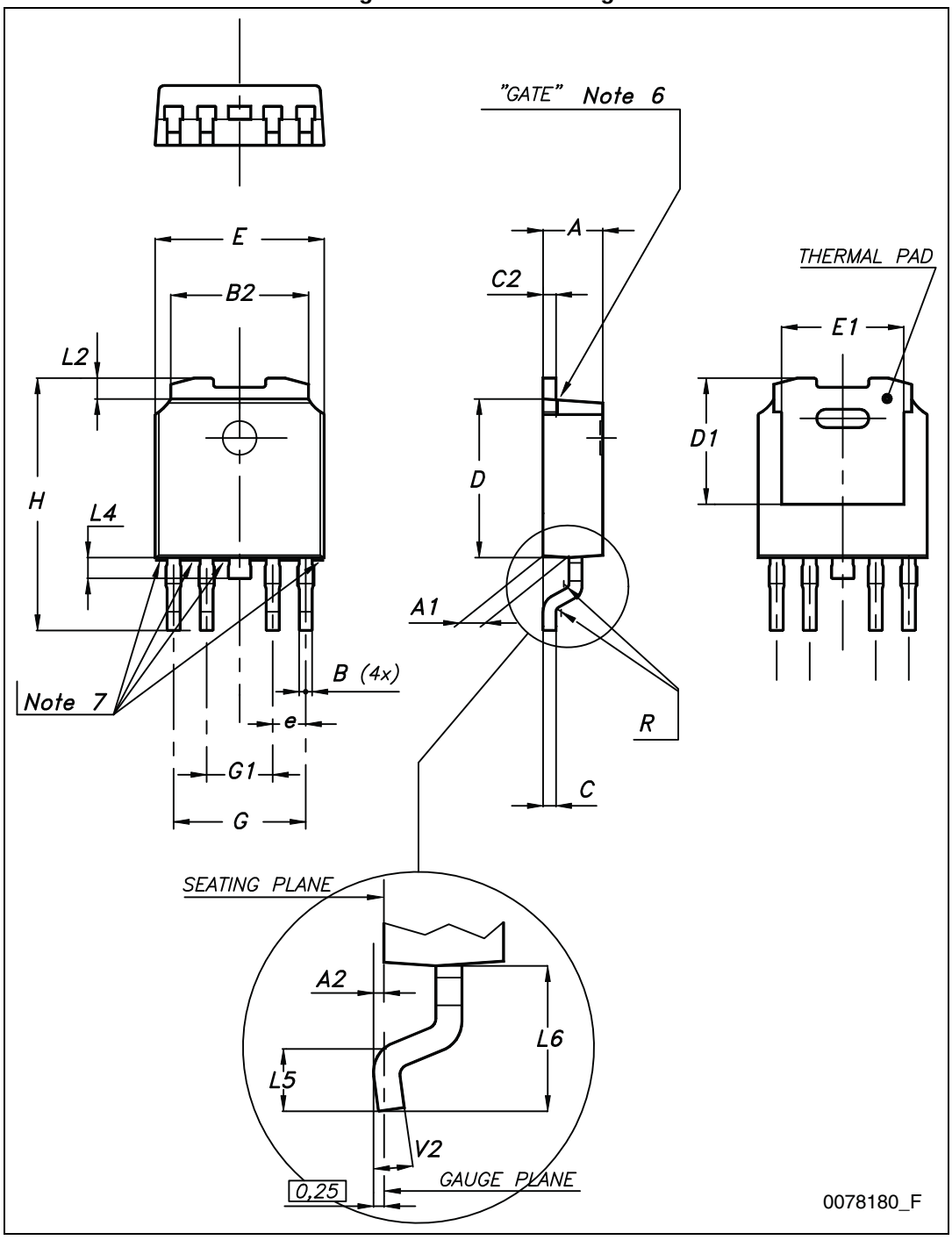


Table 6. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

Figure 25. DFN6 (3x3 mm) drawing

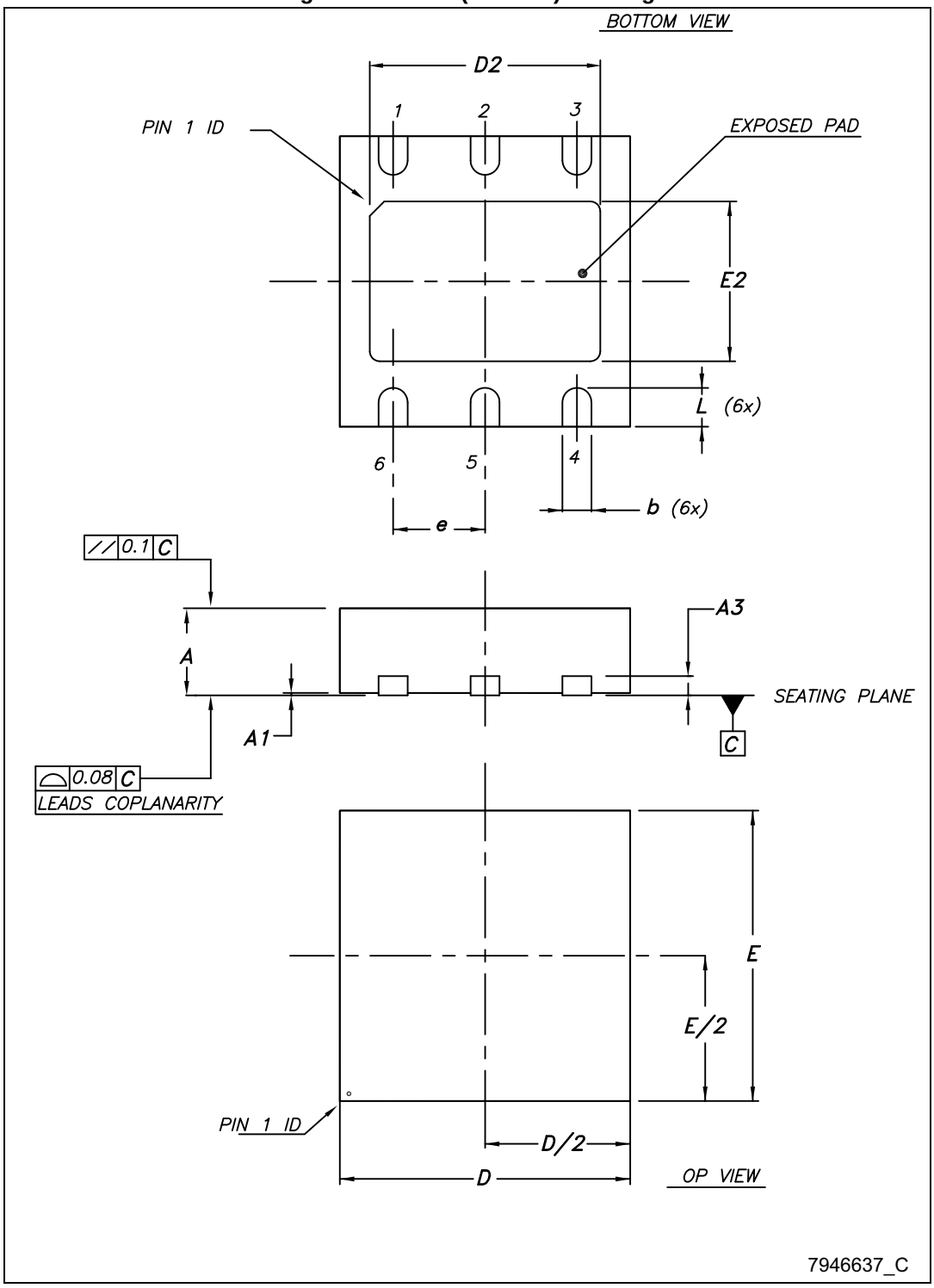
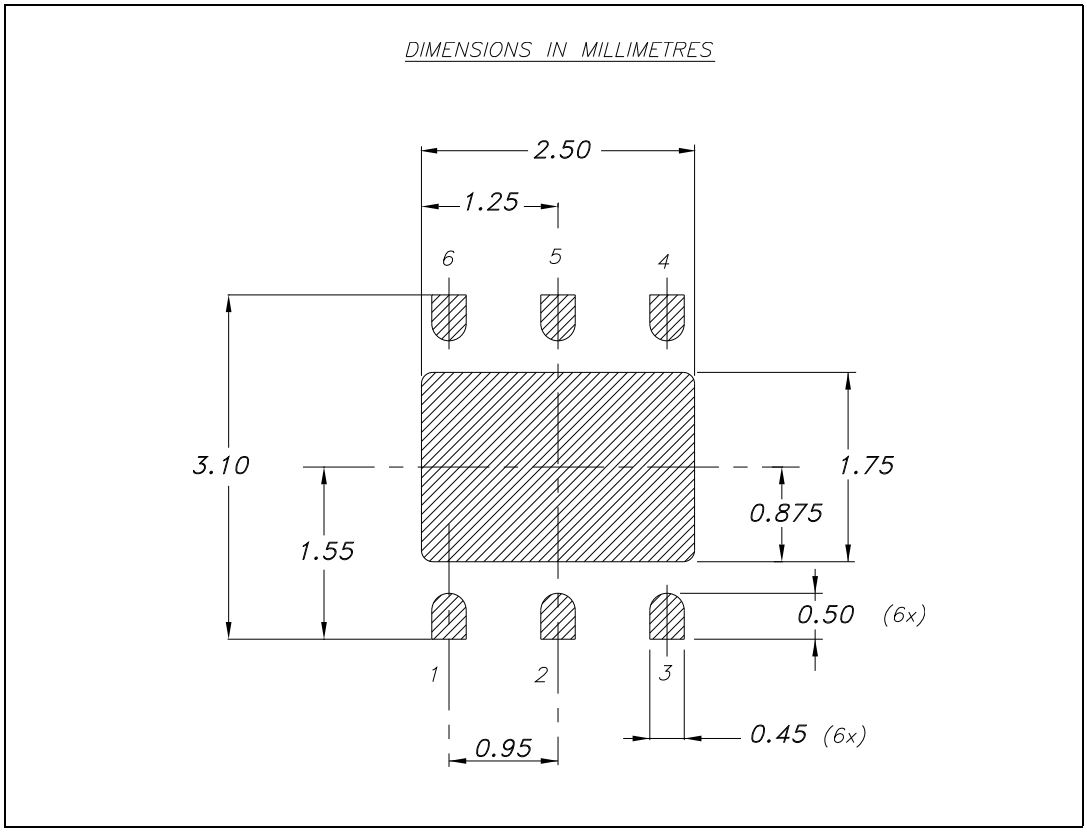


Table 7. DFN6 (3x3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1
A1	0	0.02	0.05
A3		0.20	
b	0.23		0.45
D	2.90	3	3.10
D2	2.23		2.50
E	2.90	3	3.10
E2	1.50		1.75
e		0.95	
L	0.30	0.40	0.50

Figure 26. DFN6 (3x3 mm) footprint recommended data



10 Packaging mechanical data

Figure 27. DFN6 (3x3 mm) tape

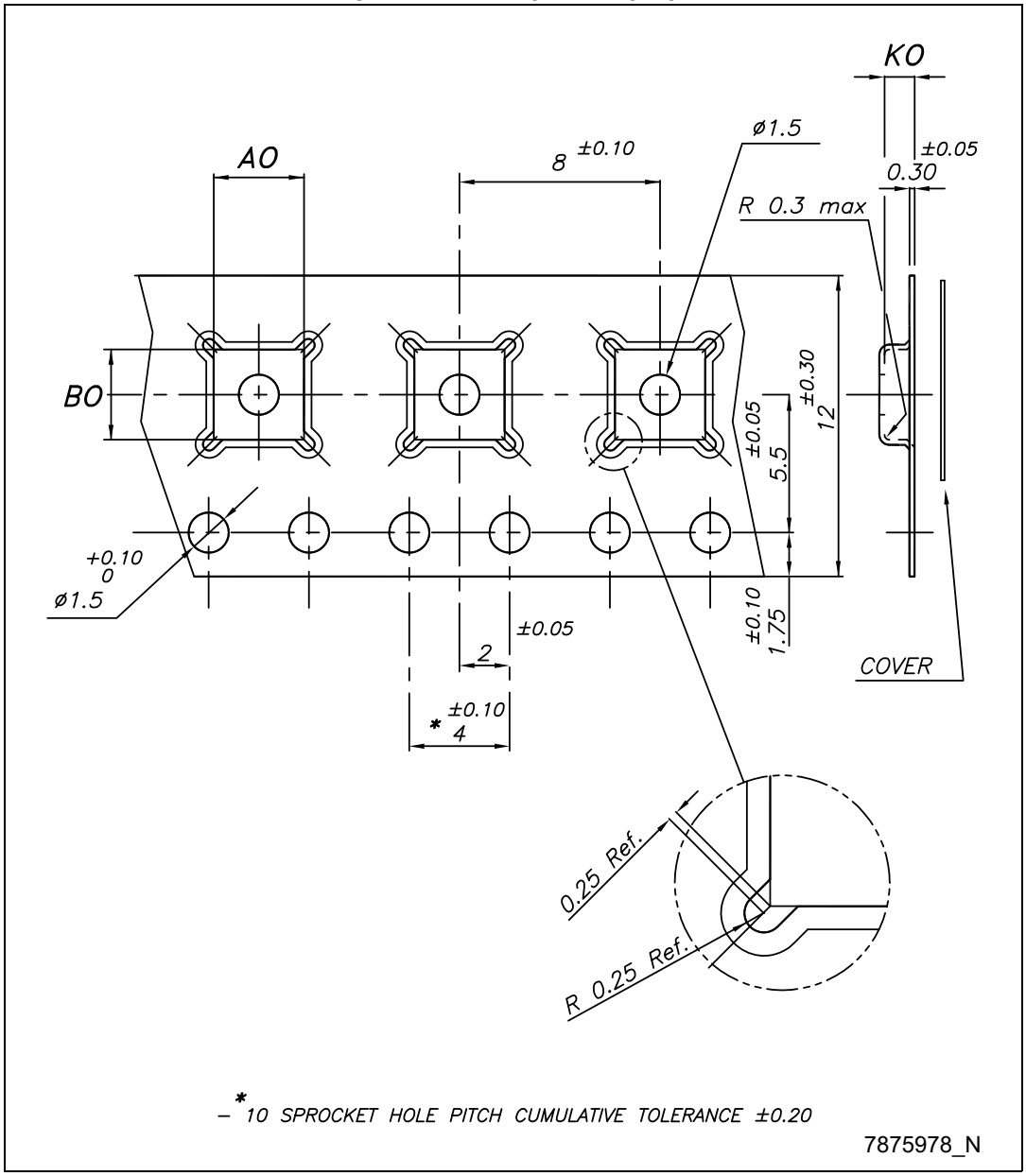


Figure 28. DFN6 (3x3 mm) reel

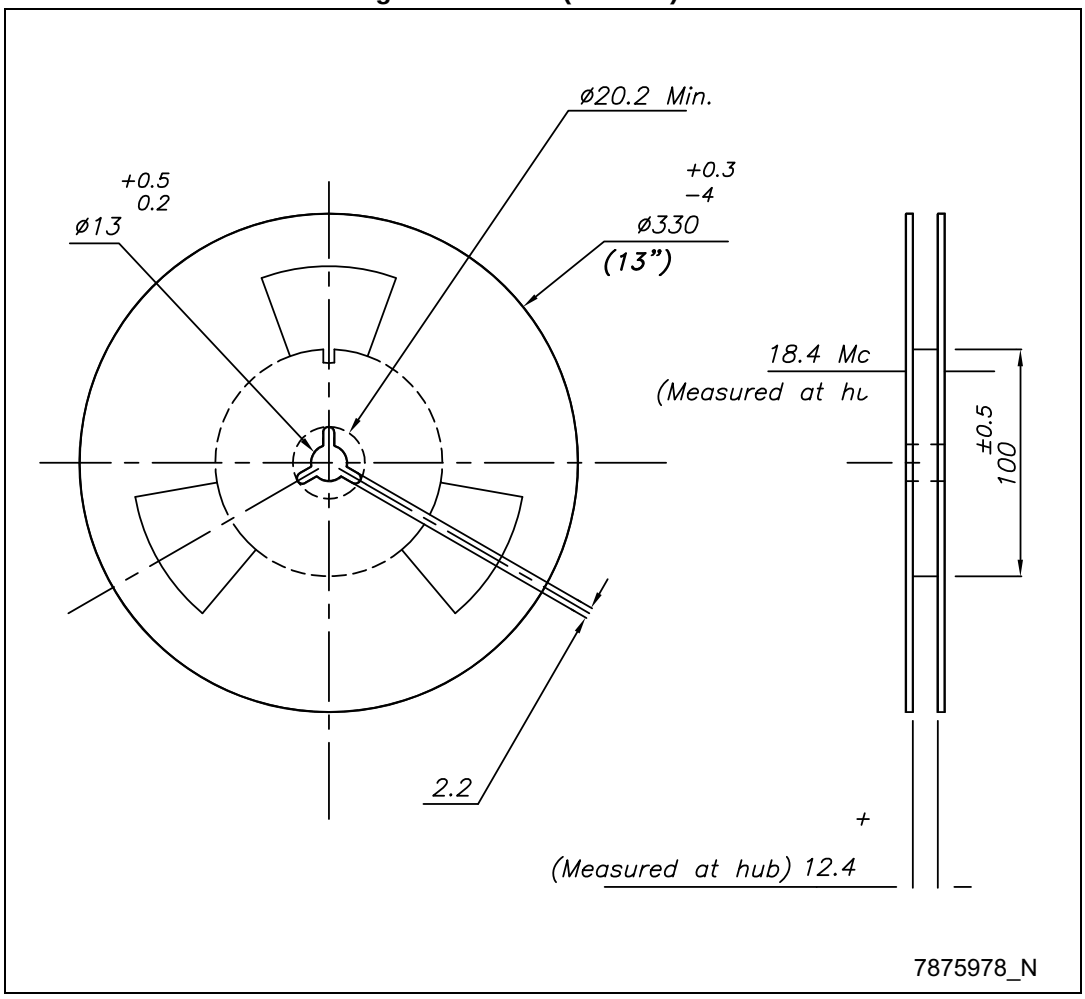


Table 8. DFN6 (3x3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	3.20	3.30	3.40
B0	3.20	3.30	3.40
K0	1	1.10	1.20

11 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Apr-2007	1	Initial release.
12-Jan-2009	2	Added new package DFN6 (3x3 mm) and mechanical data.
29-Jun-2010	3	Modified *Section 8.6: Power sequencing recommendations on page 13*.
26-May-2014	4	Changed the part numbers LD49150xx08, LD49150xx10 and LD49150xx12 to LD49150. Changed the title. Updated the description in cover page, *Table 1: Device summary*, *Section 7: Typical characteristics*, *Section 8: Application hints*, *Section 9: Package mechanical data*. Added *Section 10: Packaging mechanical data*. Minor text changes.

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