# NTD12N10

Preferred Device

# Power MOSFET
# 12 Amps, 100 Volts

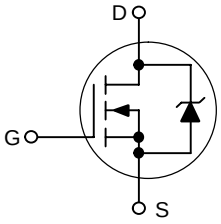
## N−Channel Enhancement−Mode DPAK

ON Semiconductor®

http://onsemi.com

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| 100 V | 165 mΩ @ 10 V | 12 A |

N−Channel




### Features

- Source−to−Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Avalanche Energy Specified
- $I_{DSS}$ and $R_{DS(on)}$ Specified at Elevated Temperature
- Mounting Information Provided for the DPAK Package
- Pb−Free Packages are Available

### Typical Applications

- PWM Motor Controls
- Power Supplies
- Converters

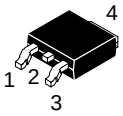
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain−to−Source Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate−to−Source Voltage<br>− Continuous<br>− Non−Repetitive ($t_p \le 10$ ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 30 | <br>Vdc<br>Vpk |
| Drain Current − Continuous @ $T_A$ = 25°C<br>− Continuous @ $T_A$ =100°C<br>− Pulsed (Note 3) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>7.0<br>36 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2) | $P_D$ | 56.6<br>0.38<br>1.76<br>1.28 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +175 | °C |
| Single Pulse Drain−to−Source Avalanche Energy − Starting $T_J$ = 25°C ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 12 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 75 | mJ |
| Thermal Resistance<br>− Junction to Case<br>− Junction to Ambient (Note 1)<br>− Junction to Ambient (Note 2) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.65<br>85<br>117 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8 in from case for 10 seconds | $T_L$ | 260 | °C |

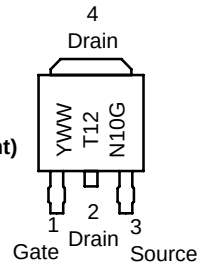
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

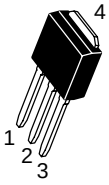
1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.
3. Pulse Test: Pulse Width = 10 μs, Duty Cycle = 2%.

### MARKING DIAGRAMS & PIN ASSIGNMENTS

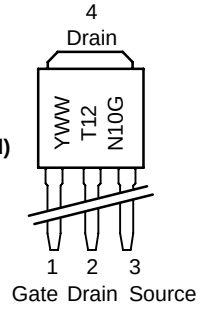



**DPAK**
**CASE 369C**
**(Surface Mount)**
**STYLE 2**




**DPAK**
**CASE 369D**
**(Straight Lead)**
**STYLE 2**




| | |
|---|---|
| Y | = Year |
| WW | = Work Week |
| T12N10 | = Device Code |
| G | = Pb−Free Package |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain−to−Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | 100<br>− | −<br>135 | −<br>− | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0 Vdc, $V_{DS}$ = 100 Vdc, $T_J$ = 25°C)<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = 100 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | −<br>− | −<br>− | 5.0<br>50 | μAdc |
| Gate−Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | − | − | ±100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | 2.0<br>− | 3.1<br>−7.5 | 4.0<br>− | Vdc<br>mV/°C |
| Static Drain−to−Source On−State Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc, $T_J$ = 125°C) | $R_{DS(on)}$ | −<br>− | 0.130<br>0.250 | 0.165<br>0.400 | Ω |
| Drain−to−Source On−Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 12 Adc) | $V_{DS(on)}$ | − | 1.62 | 2.16 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | $g_{FS}$ | − | 7.0 | − | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | − | 390 | 550 | pF |
| Output Capacitance | | $C_{oss}$ | − | 115 | 160 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | − | 35 | 70 | |
| **SWITCHING CHARACTERISTICS** (Notes 4 & 5) | | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = 80 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | − | 11 | 20 | ns |
| Rise Time | | $t_r$ | − | 30 | 60 | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 22 | 40 | |
| Fall Time | | $t_f$ | − | 32 | 60 | |
| Total Gate Charge | ($V_{DS}$ = 80 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc) | $Q_{tot}$ | − | 14 | 20 | nC |
| Gate−to−Source Charge | | $Q_{gs}$ | − | 3.0 | − | |
| Gate−to−Drain Charge | | $Q_{gd}$ | − | 7.0 | − | |
| **BODY−DRAIN DIODE RATINGS** (Note 4) | | | | | | |
| Diode Forward On−Voltage | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | −<br>− | 0.95<br>0.80 | 1.0<br>− | Vdc |
| Reverse Recovery Time | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | − | 85 | − | ns |
| | | $t_a$ | − | 60 | − | |
| | | $t_b$ | − | 28 | − | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | − | 0.3 | − | μC |

4. Indicates Pulse Test: P.W. = 300 μs max, Duty Cycle = 2%.
5. Switching characteristics are independent of operating junction temperature.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTD12N10 | DPAK | 75 Units/Rail |
| NTD12N10G | DPAK (Pb−Free) | 75 Units/Rail |
| NTD12N10−1 | DPAK−3 | 75 Units/Rail |
| NTD12N10−1G | DPAK−3 (Pb−Free) | 75 Units/Rail |
| NTD12N10T4 | DPAK | 2500 Tape & Reel |
| NTD12N10T4G | DPAK (Pb−Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## TYPICAL ELECTRICAL CHARACTERISTICS

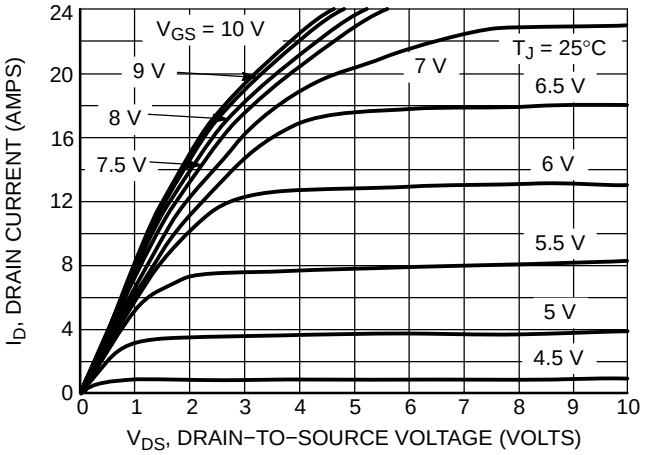



**Figure 1. On−Region Characteristics**

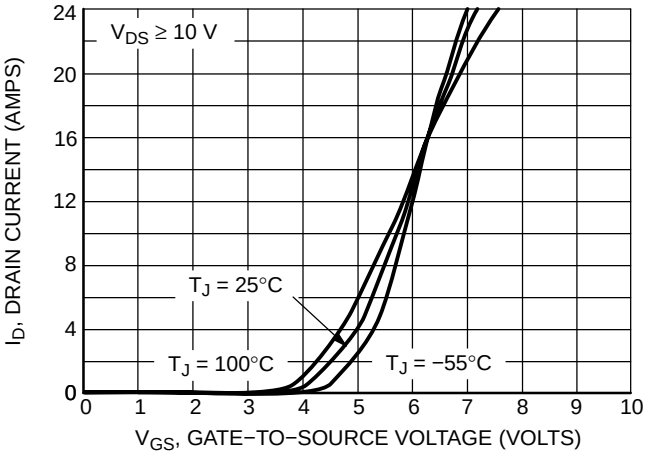



**Figure 2. Transfer Characteristics**

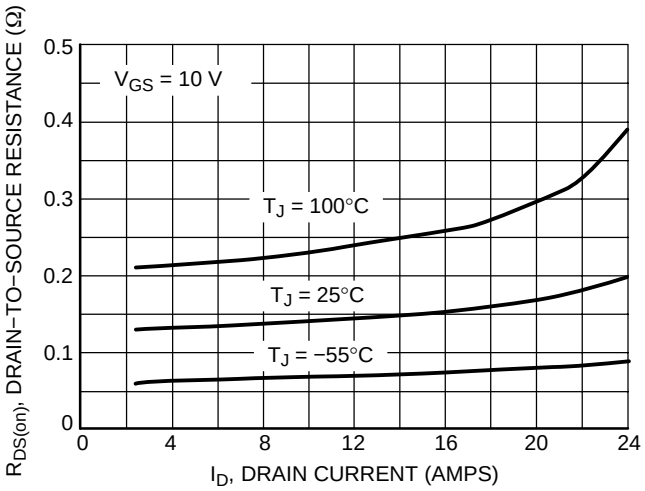



**Figure 3. On−Resistance versus Drain Current and Temperature**

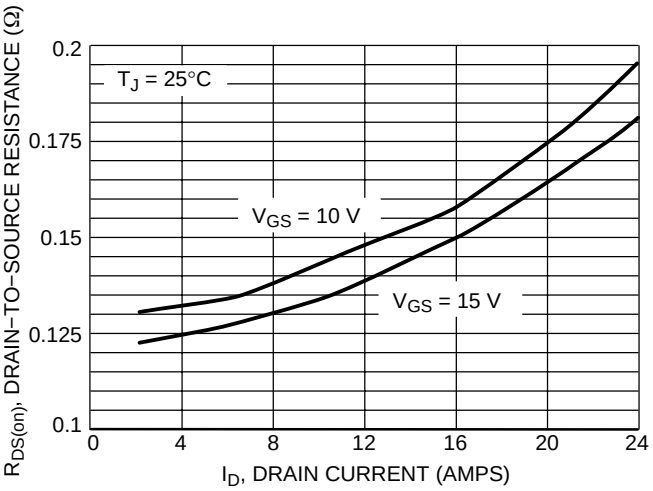



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

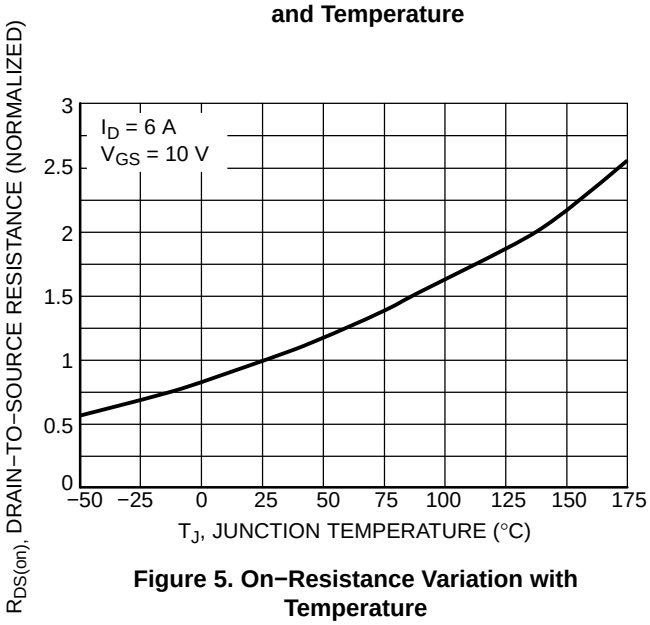



**Figure 5. On−Resistance Variation with Temperature**

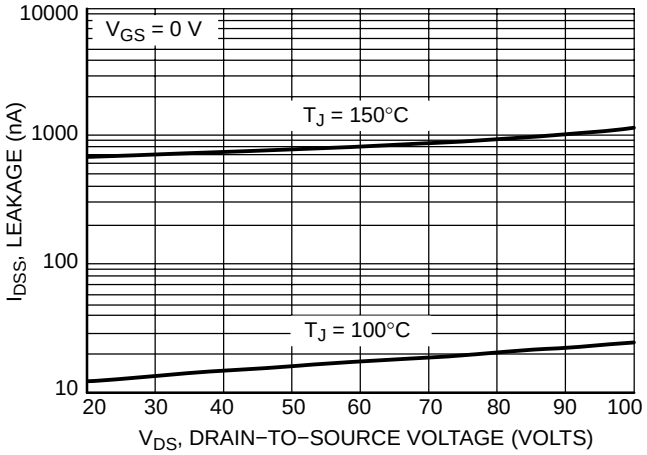



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$

$R_G$ = the gate drive resistance

and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

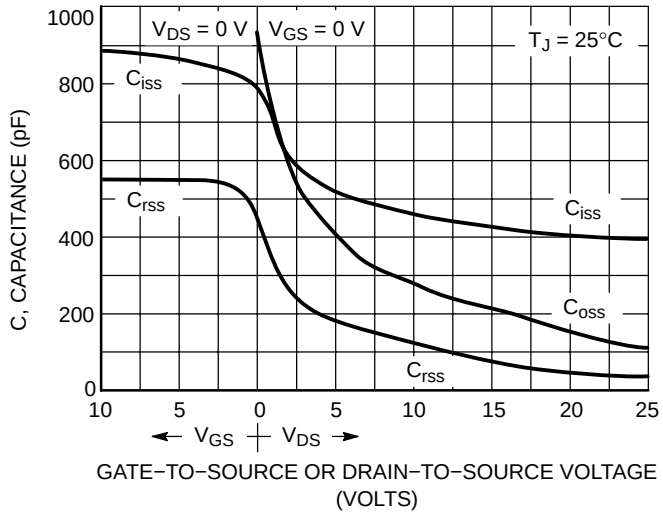



**Figure 7. Capacitance Variation**

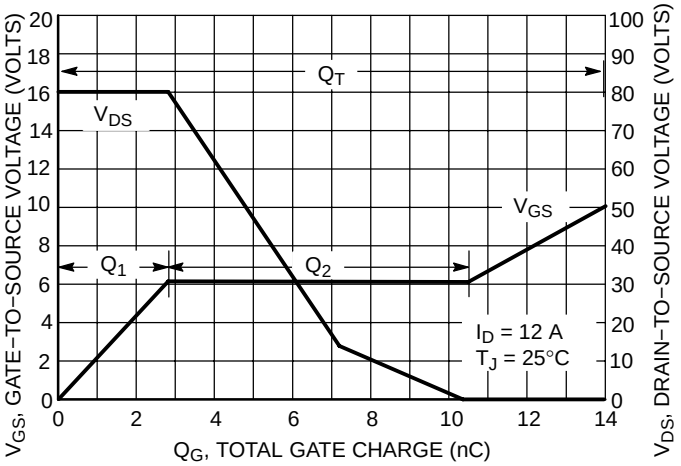



**Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge**

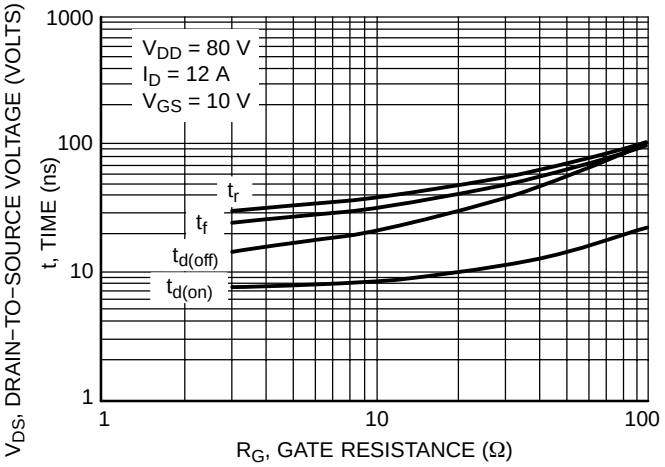



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN−TO−SOURCE DIODE CHARACTERISTICS

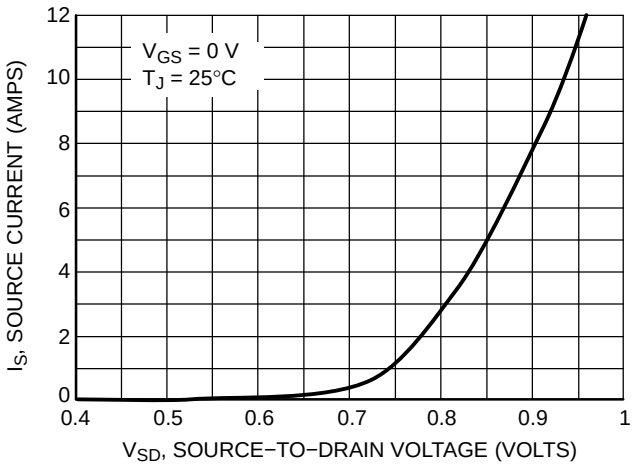



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance−General Data and Its Use.”

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

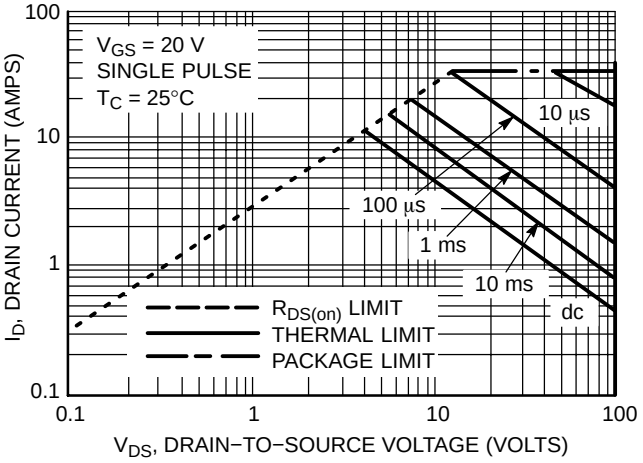



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

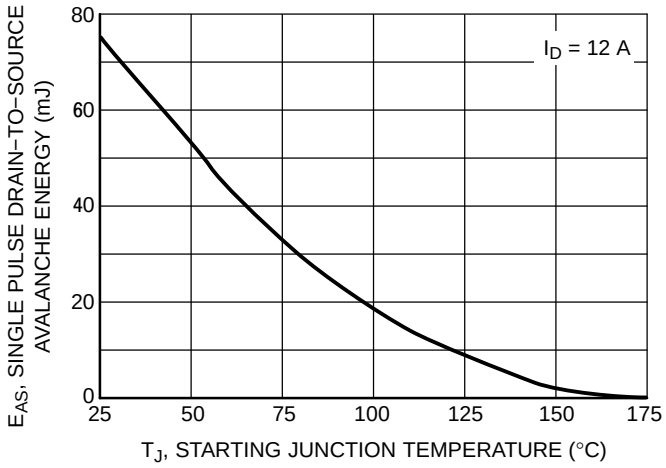



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

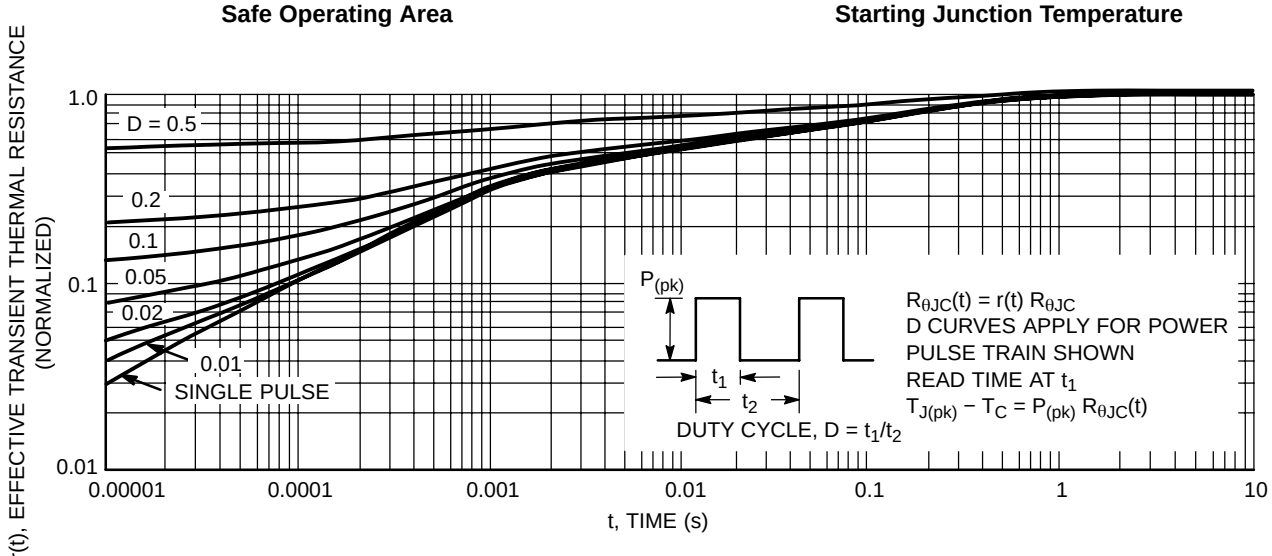



**Figure 13. Thermal Response**

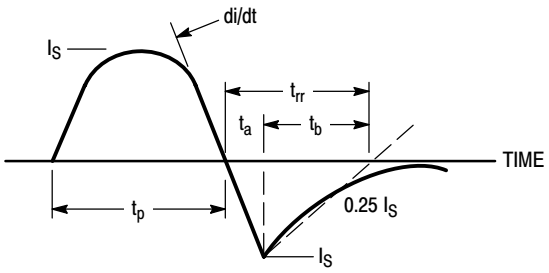
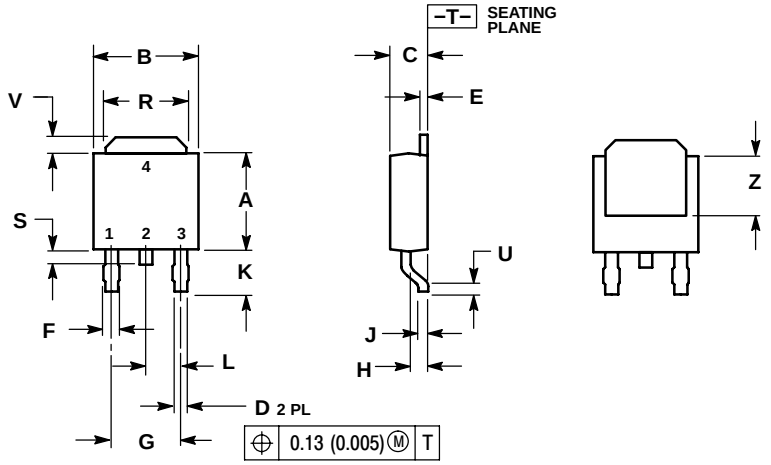



**Figure 14. Diode Reverse Recovery Waveform**

## PACKAGE DIMENSIONS

**DPAK**
CASE 369C−01
ISSUE O

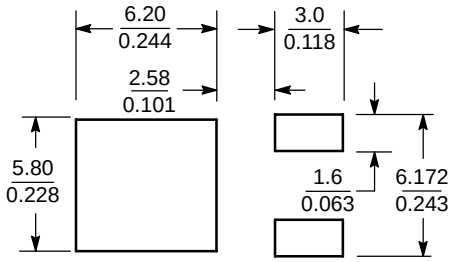



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.180 BSC | | 4.58 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC | | 2.29 BSC | |
| R | 0.180 | 0.215 | 4.57 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | −−− | 0.51 | −−− |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

## SOLDERING FOOTPRINT*

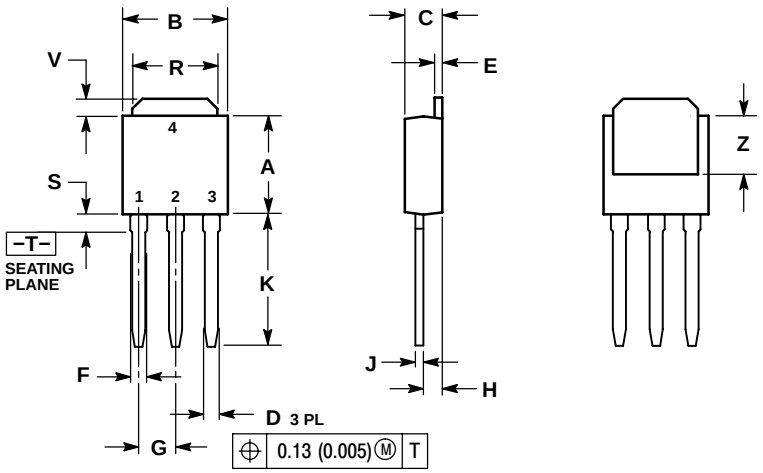



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**DPAK−3**
CASE 369D−01
ISSUE B




NOTES:
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2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



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**NTD12N10/D**