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LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Jeffery Tunstall

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Raj Pithadia

APPROVED BY
Charles F. Saffle

DRAWING APPROVAL DATE
16-01-15

REVISION LEVEL

MICROCIRCUIT, LINEAR, BIPOLAR, POSITIVE, ADJUSTABLE, LOW DROPOUT, VOLTAGE REGULATOR, MONOLITHIC SILICON

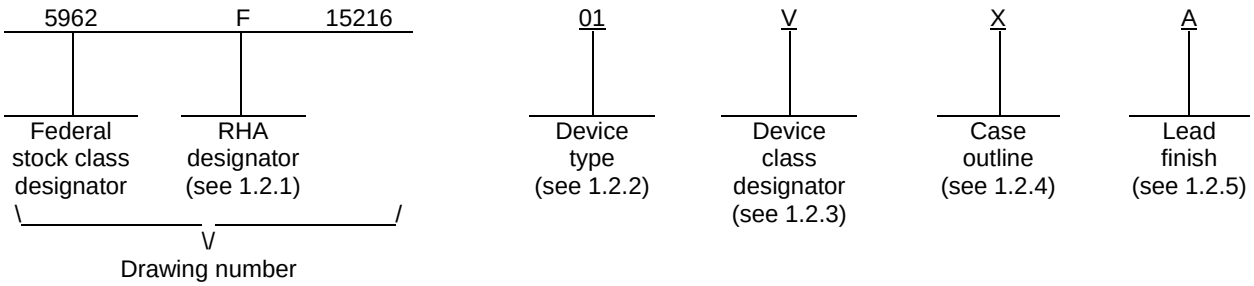
SIZE	CAGE CODE	
A	**67268**	**5962-15216**

SHEET 1 OF 21

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RH-L6000-ADJ	Radiation hardened, positive, adjustable, low drop out voltage regulator with Inhibit access

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16	Flat pack 1/ 2/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1/ AlN ceramic header with metalized bottom side and pullback of 0.01 x 0.02 inches.
2/ Lid is connected to the ground.

1.3 Absolute maximum ratings. 3/

DC input voltage vs. GND	-0.3 to 12 V
DC output voltage vs. GND	-0.3 to (V_{IN} + 0.3 V)
INHIBIT pin vs. GND	-0.3 to 12 V
Overcurrent monitor pin vs. GND	-0.3 to 12 V
Short-circuit current adjustment pin vs. GND	-0.3 to 12 V
Adjustable pin voltage	-0.3 to (FILT C + 0.6 V)
Stability capacitor pin voltage	-0.3 to 2.5 V
Filter capacitor pin voltage	-0.3 to 1.3 V
Output current: Case X	2 A
Power dissipation at T_A < 25°C: Case X	1 W 4/
Power dissipation at T_C = 25°C: Case X	15 W
Thermal resistance, junction-to-case (θ_{JC}): Case X	8.3°C/W
Thermal resistance, junction-to-ambient (θ_{JA}): Case X	125°C/W
Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C 5/
Maximum junction temperature (T_J)	+150°C 6/

1.4 Recommended operating conditions.

Input voltage range (V_{IN})	2.5 V to 12 V
Output voltage range (V_{OUT})	1.245 V to 9 V
Ambient operating temperature range (T_A)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 - 300 rads(Si)/s) ..... 300 krads(Si) 7/
Maximum total dose available (low dose rate = 10 mrads(Si)/s) ..... 300 krads(Si) 7/

Single event phenomenon (SEP):
No SEL occurs at effective LET (see 4.4.4.4)..... ≤ 120 MeV/(mg/cm^2) 8/
SET observed at threshold LET (saturated cross section= 7.99x10^{-6} cm^2)..... = 26 MeV/(mg/cm^2) 8/

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Power dissipation at T_A < 25°C without heatsink.
5/ Distance of not less than 1.5 mm from the device body and the same lead shall not be resoldered until 3 minutes have elapsed.
6/ Internally limited to +175°C by thermal shut down circuit.
7/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 condition A (high dose rate = 50 – 300 rads(Si)/s) and condition D (low dose rate = 10 mrads(Si)/s) to a dose level of 300 krad(Si). Manufacturer also performed accelerated annealing 1.5X over test and observed no time dependent effects. The post-irradiation of HDR and LDR test parametric values falls within the specification limits as specified in Table IA. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and D.
8/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/, 2/, 3/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output voltage	V_{OUT}	2.5 V < V_{IN} < 12 V, I_{OUT} = 400 mA	1, 2, 3	01	1.205	1.285	V
		2.5 V < V_{IN} < 12 V, I_{OUT} = 1 A			1.205	1.285	
Line regulation 4/	K_{VI}	2.5 V < V_{IN} < 12 V, I_{OUT} = 5 mA	1	01		0.4	%
			2			0.35	
			3			0.5	
Load regulation	K_{VO}	V_{IN} = 2.5 V, 5 mA < I_{OUT} < 400 mA	1	01		0.4	%
			2			0.3	
			3			0.5	
		V_{IN} = 2.5 V, 5 mA < I_{OUT} < 1 A	1	01		0.5	
			2, 3			0.6	
Quiescent current (ON state)	Iq	I_{OUT} = 5 mA V_{IN} = 2.5 V	1	01		15	mA
		I_{OUT} = 30 mA V_{IN} = 2.5 V	1, 2, 3			15	
		I_{OUT} = 300 mA V_{IN} = 2.5 V	1, 2			30	
			3			35	
		I_{OUT} = 1 A, V_{IN} = 2.5 V	1	01		60	
			2			50	
			3			80	
Quiescent current (OFF state)	IqOFF	V_{INH} > 2.4 V, V_{IN} = 2.5 V	1, 2, 3	01		1	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/, 2/, 3/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dropout voltage	V_d	I_{OUT} = 400mA, +2.5 V < V_{OUT} < +9V	1	01		0.45	V
			2			0.55	
			3			0.4	
		I_{OUT} = 1A, +2.5 V < V_{OUT} < +9V	1	01		0.8	
			2			0.9	
			3			0.7	
Inhibit voltage	VIN_{HON}	V_{IN} = 2.5 V, I_{OUT} = 5 mA	1, 2, 3	01		0.8	V
	VIN_{HOFF}				2.4		
Supply voltage rejection 5/	SVR	V_{IN} = V_{OUT} + 2.5 V ±0.5V, V_{OUT} = 3V, I_{OUT} = 5 mA, f = 120 Hz, T_A = +25°C	4	01	60		dB
		V_{IN} = V_{OUT} + 2.5 V ±0.5V, V_{OUT} = 3 V, I_{OUT} = 5 mA, f = 33kHz, T_A = +25°C			30		
Inhibit propagation delay 5/	t_{PLH}	V_{INH} = from 0 V to 2.4 V, V_{IN} = V_{OUT} + 2.5V, V_{OUT} = 3 V, I_{OUT} = 400 mA, C_{IN} = C_{OUT} = 10 µF, see figure 3	9	01		30	µs
	t_{PHL}					100	

1/ Device type 01 has been characterized through all levels M, D, P, L, R, F of irradiation. However, this device is tested at the "F" level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ V_{IN} = 2.5 V, V_{OUT} = 1.245 V, T_A = 25°C, C_{IN} = 10 µF, C_{OUT} = 10 µF.

3/ These parts have been characterization tested at low dose rate, see 1.5.

4/ $K_{VI} = (V_{rline}) \times 100/V_{OUT1}$ where $V_{rline} = V_{OUT1} - V_{OUT'1}$,
V_{OUT1} = V_{OUT} when V_{IN} = 2.5 V and I_{OUT} = 5 mA,
$V_{OUT'1}$ = V_{OUT} when V_{IN} = V_{MAX} = 12 V and I_{OUT} = 5 mA

5/ Characterized on initial manual test via design or process controlled but not ATE production test due to complexity of the devices parametric nature. However, design or process changes will affect this parameter. This parameter is not tested to post irradiation.

TABLE IB. SEP test limits. 1/ 2/

Device types	V_{CC} = 3V 4/		Bias for Latch-up test V_{CC} = 12 V no latch-up (SEL) occurs effective LET 3/
	SET observed threshold LET]	Maximum device cross section	
01	LET =.26 MeV/(mg/cm^2)	7.99x 10^{-6} cm^2/device	LET ≤ 120 MeV/(mg/cm^2)

1/ For SEP test conditions, see 4.4.4.2 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature is T_A = +125°C ± 10°C for SEL.

4/ SET testing was performed at supply voltages of 3.0V to 12 V and resulted an SET observed at threshold LET 26 MeV/(mg/cm^2) with saturated cross section= 7.99x10^{-6} cm^2/device.

Device type	01
Case outline	X
Terminal number	Terminal Symbol
1	V_{OUT2}
2	V_{OUT2}
3	V_{IN}
4	V_{IN}
5	V_{IN}
6	V_{OUT1}
7	V_{OUT1}
8	ISC
9	FILT C
10	OCM
11	STAB
12	GND
13	GND
14	INH
15	ADJ
16	NC

NC = No connect

FIGURE 1. Terminal connections.

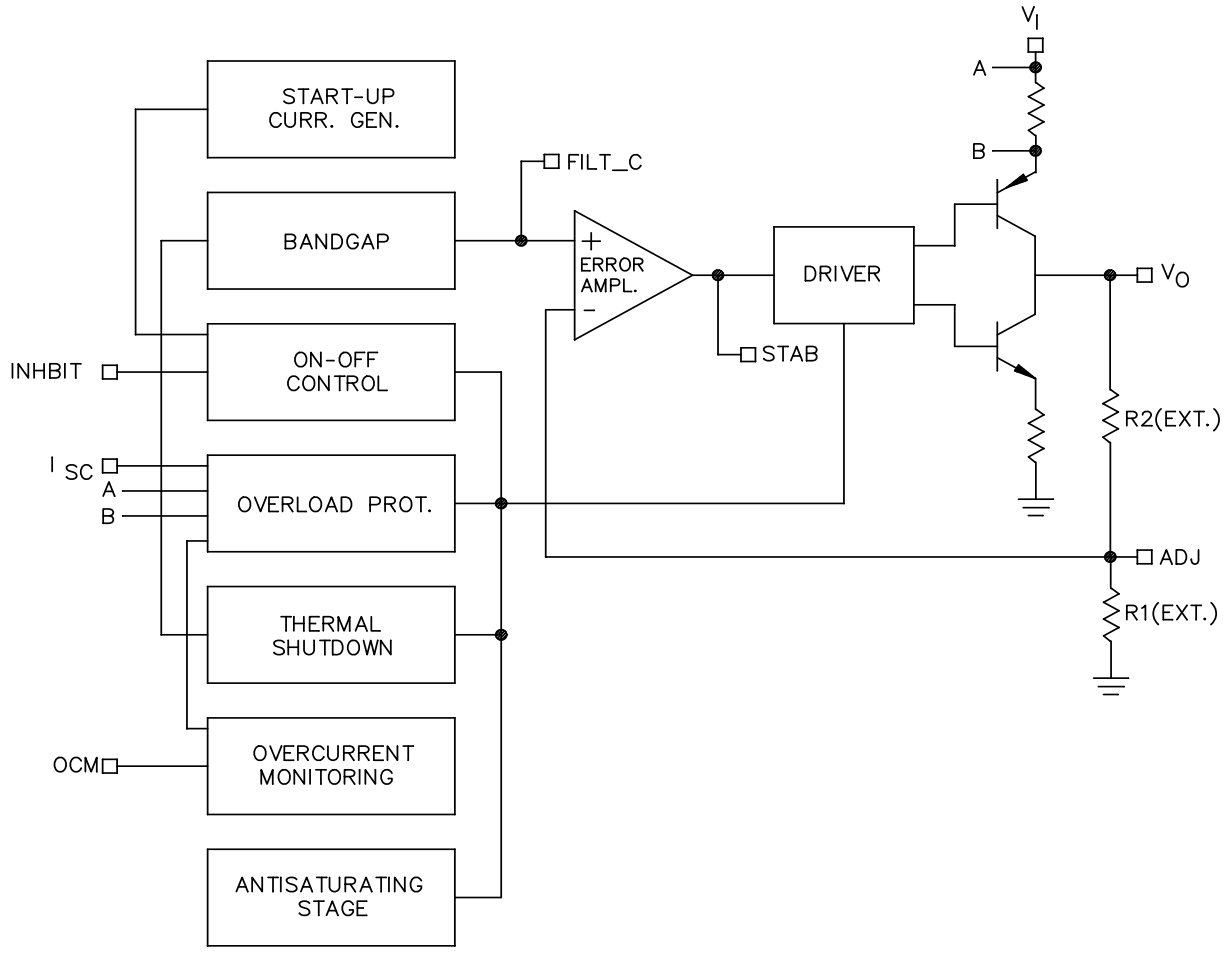


FIGURE 2. Block diagram.

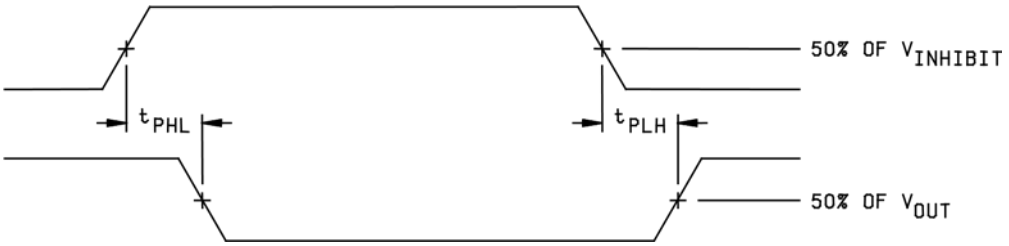


FIGURE 3. Inhibit propagation delay waveform.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5, 6, 7, 8, 10 and 11 in table IA, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1
Final electrical parameters (see 4.2)	1, 2, 3, 4, 9, 1/	1, 2, 3, 4, 9, 1/, 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 9,	1, 2, 3, 4, 9,
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 4, 9,	1, 2, 3, 4, 9 2/
Group D end-point electrical parameters (see 4.4)	1, 2, 3, 4, 9	1, 2, 3, 4, 9
Group E end-point electrical parameters (see 4.4)	1, 4, 9	1, 9

1/ PDA applies to subgroup 1.

2/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be computed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test. Delta parameters (+25°C).

Parameters	Symbol	Test Conditions	Delta Limits
Change in output voltage	$\Delta V_{OUT}/V_{OUT}$	2.5 V < V_{IN} < 12 V at 400 mA	±1%
Change in input regulation coefficient	ΔV_{rline}	2.5 V < V_{IN} < 12 V at 5 mA	±6 mV
Change in standby current	ΔIQ/IQ	I_{OUT} = 300 mA, V_{IN} = 2.5 V	±20% or ±3.5 mA 1/

1/ Whichever is greater.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C +5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, test method 1019, condition A and condition D as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon. However, the particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip volume. In order to detect latch-up the ion range shall be sufficient to penetrate well beyond the deepest part of the sensitive volume of the devices.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEL test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions (SEP).

b. Occurrence of latch-ups (SEL).

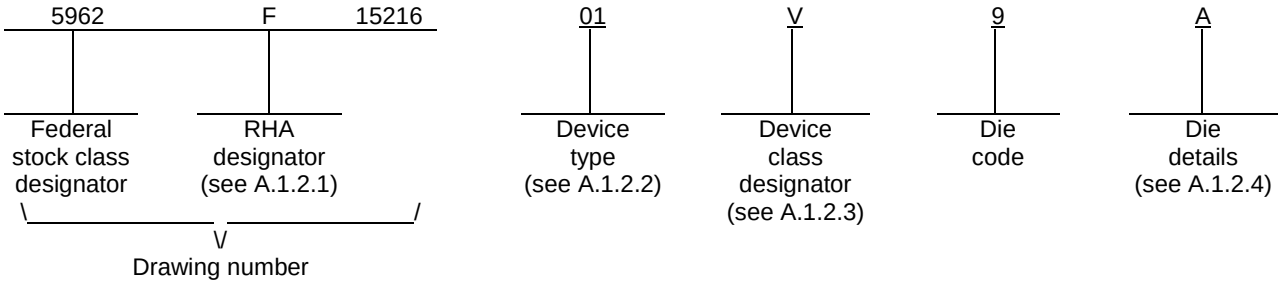
c. Number of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-15216

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function
01	RH-L6000-ADJ	Radiation hardened, positive, adjustable, 2 A, low dropout voltage regulator with inhibit access

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.1.1 and 4.4.4.2 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

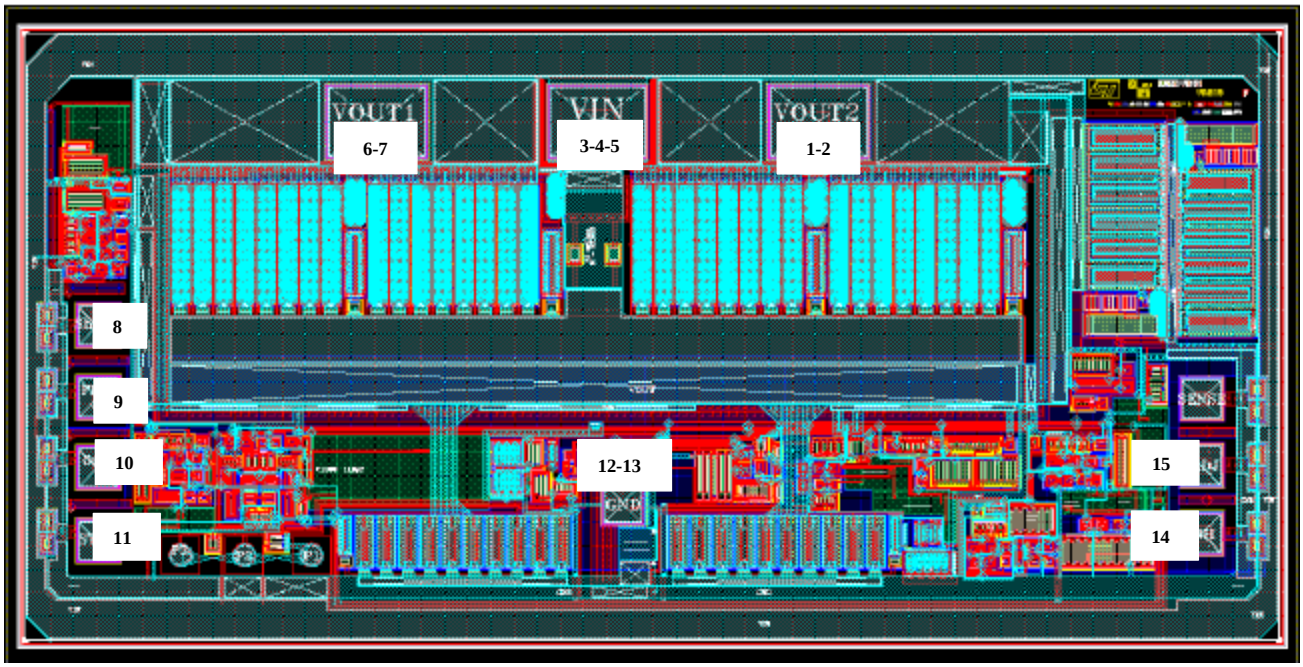
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime-VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime VA and have agreed to this drawing.



Pad number	Pad name	Pad coordinates	
		X	Y
1, 2	V_{OUT2}	773	998
3, 4, 5	V_{IN}	-255	998
6, 7	V_{OUT1}	-1281.6	998
9	FILT C	-2575	-285
10	OCM	-2575	-609.3
11	STAB	-2575	-947.3
12, 13	GND	-135.6	775.1
14	INH	2552.6	-917.1
15	ADJ	2552.6	-597.7

NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 230 mils x 111 mils
Die thickness: 375 µm ± 25 µm (14.8 mils ± 1 mil)

Pad size: V_{IN}, V_{OUT} pads: 450 µm x 330 µm
Control pads: 184 µm x 184 µm

Interface materials.
Top metallization: Metal 1 Al/Si/Cu, 0.6 µm ± 0.10 µm
Metal 2 Al/Si/Cu 1.05 µm ± 0.15 µm
Backside metallization: None

Glassivation.
Type: P. Vapox + Nitride
Thickness: 0.5 µm ± 0.1 µm + 0.6 µm ± 0.08 µm

Substrate: Silicon

Assembly related information.
Substrate potential: Floating if tied to V_{SS}
Special assembly instructions: Pad sense not used

FIGURE A-1. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-01-15

Approved sources of supply for SMD 5962-15216 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F1521601VXC	F8859	RHFL6000AKP01V
5962F1521601VXA	F8859	RHFL6000AKP02V
5962F1521601QXC	F8859	RHFL6000AKP01Q
5962F1521601QXA	F8859	RHFL6000AKP02Q
5962F1521601V9A	F8859	RHFL6000AD2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F8859	STMicroelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.