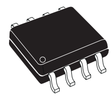
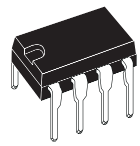
L6384

HIGH-VOLTAGE HALF BRIDGE DRIVER

- HIGH VOLTAGE RAIL UP TO 600 V
- dV/dt IMMUNITY +- 50 V/nsec IN FULL TEMPERATURE RANGE
- DRIVER CURRENT CAPABILITY: 400 mA SOURCE, 650 mA SINK
- SWITCHING TIMES 50/30 nsec RISE/FALL WITH 1nF LOAD
- CMOS/TTL SCHMITT TRIGGER INPUTS WITH HYSTERESIS AND PULL DOWN
- SHUT DOWN INPUT
- DEAD TIME SETTING
- UNDER VOLTAGE LOCK OUT
- INTEGRATED BOOTSTRAP DIODE
- CLAMPING ON Vcc
- SO8/MINIDIP PACKAGES



SO8



Minidip

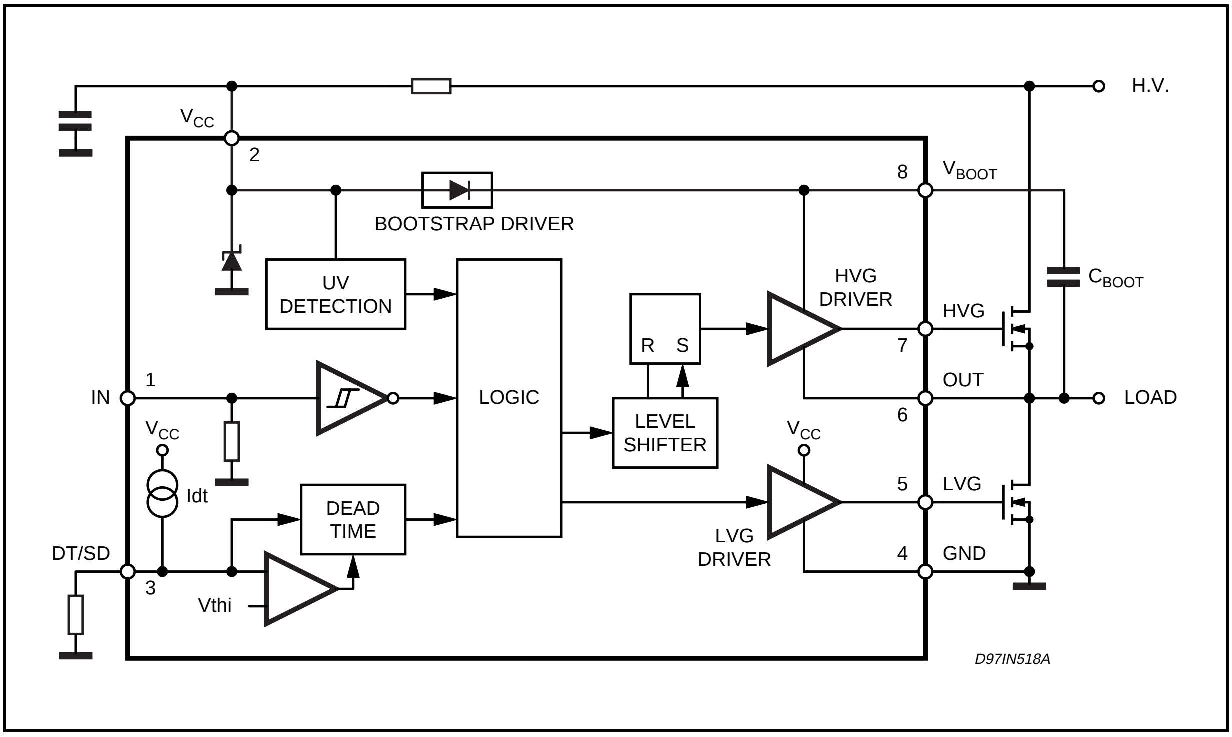
ORDERING NUMBERS:

L6384D L6384

DESCRIPTION

The L6384 is an high-voltage device, manufactured with the BCD"OFF-LINE" technology. It has an Half - Bridge Driver structure that enables to drive N Channel Power MOS or IGBT. The Upper (Floating) Section is enabled to work with voltage Rail up to 600V. The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices. Matched delays between Lower and Upper Section simplify high frequency operation. Dead time setting can be readily accomplished by means of an external resistor.

BLOCK DIAGRAM

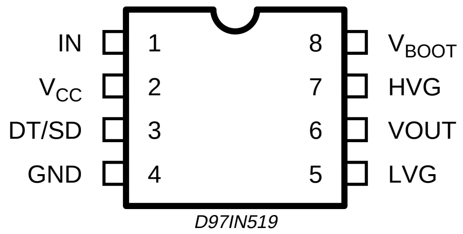


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
Vout	Output Voltage	-3 to Vboot -18	V
Vcc	Supply Voltage (*)	- 0.3 to 14.6	V
Is	Supply Current (*)	25	mA
Vboot	Floating Supply Voltage	-1 to 618	V
Vhvg	Upper Gate Output Voltage	-1 to Vboot	V
Vlvg	Lower Gate Output Voltage	-0.3 to Vcc +0.3	V
Vi	Logic Input Voltage	-0.3 to Vcc +0.3	V
Vsd	Shut Down/Dead Time Voltage	-0.3 to Vcc +0.3	V
dVout/dt	Allowed Output Slew Rate	50	V/ns
Ptot	Total Power Dissipation (Tj = 85 °C)	750	mW
Tj	Junction Temperature	150	°C
Ts	Storage Temperature	-50 to 150	°C

(*) The device has an internal Clamping Zener between GND and the Vcc pin, It must not be supplied by a Low Impedence Voltage Source.
Note: ESD immunity for pins 6, 7 and 8 is guaranteed up to 900 V (Human Body Model)

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	SO8	Minidip	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	150	100	°C/W

PIN DESCRIPTION

N.	Name	Type	Function
1	IN	I	Logic Input: it is in phase with HVG and in opposition of phase with LGV. It is compatible to V_{CC} voltage. [Vil Max = 1.5V, Vih Min = 3.6V]
2	Vcc	I	Supply input voltage: there is an internal clamp [Typ. 15.6V]
3	DT/SD	I	High impedance pin with two functionalities. When pulled lower than Vdt [Typ. 0.5V] the device is shut down. A voltage higher than Vdt sets the dead time between high side gate driver and low side gate driver. The dead time value can be set forcing a certain voltage level on the pin or connecting a resistor between pin 3 and ground. Care must be taken to avoid below threshold spikes on pin 3 that can cause undesired shut down of the IC. For this reason the connection of the components between pin 3 and ground has to be as short as possible. This pin can not be left floating for the same reason. The pin has not be pulled through a low impedance to V_{CC}, because of the drop on the current source that feeds Rdt. The operative range is: Vdt....270K · Idt, that allows a dt range of 0.4 - 3.1µs.
4	GND		Ground

PIN DESCRIPTION (continued)

N.	Name	Type	Function
5	LVG	O	Low Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit guarantees 0.3V max on the pin (@ I_{sink} = 10mA) with V_{CC} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedance also in SD conditions.
6	Vout	O	Upper Driver Floating Reference: layout care has to be taken to avoid below ground spikes on this pin.
7	HVG	O	High Side Driver Output: the output stage can deliver 400mA source and 650mA sink [Typ. Values]. The circuit gurantees 0.3V max between this pin and Vout (@ I_{sink} = 10mA) with V_{CC} > 3V and lower than the turn on threshold. This allows to omit the bleeder resistor connected between the gate and the source of the external mosfet normally used to hold the pin low; the gate driver ensures low impedance also in SD conditions.
8	Vboot		Bootstrap Supply Voltage: it is the upper driver floating supply. The bootstrap capacitor connected between this pin and pin 6 can be fed by an internal structure named "bootstrap driver" (a patented structure). This structure can replace the external bootstrap diode.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vout	6	Output Voltage		Note1		580	V
Vboot - Vout	8	Floating Supply Voltage		Note1		17	V
fsw		Switching Frequency	HVG,LVG load CL = 1nF			400	kHz
Vcc	2	Supply Voltage				Vclamp	V
T_j		Junction Temperature		-45		125	°C

Note 1: If the condition Vboot - Vout < 18V is guaranteed, Vout can range from -3 to 580V.

ELECTRICAL CHARACTERISTICS
AC Operation (V_{CC} = 14.4V; Tj = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ton	1 vs 5,7	High/Low Side Driver Turn-On Propagation Delay	Vout = 0V R_{dt} = 47kΩ		200+dt		ns
tonsd	3 vs 5,7	Shut Down Input Propagation Delay			220	280	ns
toff	1 vs 5,7	High/Low Side Driver Turn-Off Propagation Delay	Vout = 0V R_{dt} = 47kΩ		250	300	ns
			Vout = 0V R_{dt} = 146kΩ		200	250	ns
			Vout = 0V R_{dt} = 270kΩ		170	200	ns
tr	7,5	Rise Time	CL = 1000pF		70		ns
tf	7,5	Fall Time	CL = 1000pF		30		ns

DC Operation (V_{CC} = 14.4V; Tj = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage Section							
Vclamp	2	Supply Voltage Clamping	Is = 5mA	14.6	15.6	16.6	V
Vccth1	2	Vcc UV Turn On Threshold		11.5	12	12.5	V
Vccth2	2	Vcc UV Turn Off Threshold		9.5	10	10.5	V

DC Operation (continued)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Vcchys	2	Vcc UV Hysteresis			2		V
Iqccu	2	Undervoltage Quiescent Supply Current	Vcc ≤ 11V		150		µA
Iqcc	2	Quiescent Current	Vin = 0		380	500	µA
Bootstrapped supply Voltage Section							
Vboot	8	Bootstrap Supply Voltage				17	V
IQBS		Quiescent Current	Vout = Vboot; IN = HIGH			200	µA
ILK		High Voltage Leakage Current	VHVG = Vout = Vboot = 600V			10	µA
Rdson		Bootstrap Driver on Resistance (*)	Vcc ≥ 12.5V; IN = LOW		125		Ω
High/Low Side Driver							
Iso	5,7	Source Short Circuit Current	VIN = Vih (tp < 10µs)	300	400		mA
Isi		Sink Short Circuit Current	VIN = Vil (tp < 10µs)	500	650		mA
Logic Inputs							
Vil	2,3	Low Level Logic Threshold Voltage				1.5	V
Vih		High Level Logic Threshold Voltage		3.6			V
Iih		High Level Logic Input Current	VIN = 15V		50	70	µA
Iil		Low Level Logic Input Current	VIN = 0V			1	µA
Iref	3	Dead Time Setting Current			28		µA
dt	3 vs 5,7	Dead Time Setting Range (**)	Rdt = 47k Rdt = 146 Rdt = 270k	0.4	0.5 1.5 2.7	 3.1	µs µs µs
Vdt	3	Shutdown Threshold			0.5		V

(*) R_{DSON} is tested in the following way: $R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$

where I_1 is pin 8 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$

(**) Pin 3 is a high impedence pin. Therefore dt can be set also forcing a certain voltage V_3 on this pin. The dead time is the same obtained with a Rdt if it is: $Rdt \cdot Iref = V_3$.

Figure 1. Input/Output Timing Diagram

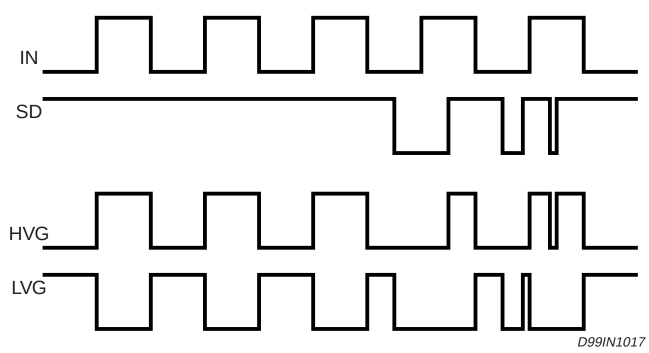
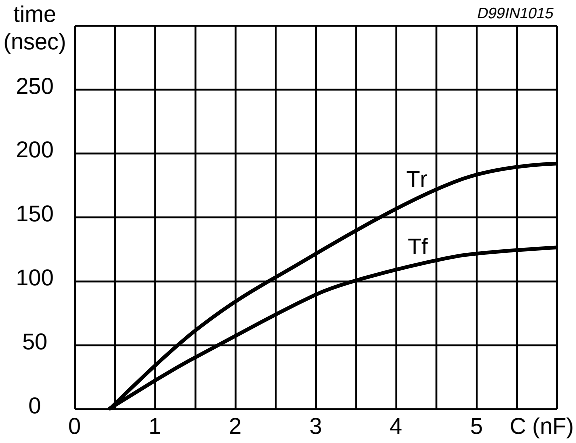
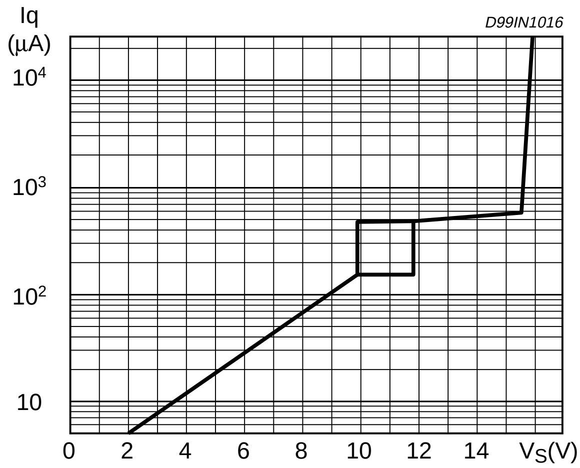


Figure 2. Typical Rise and Fall Times vs. Load Capacitance



For both high and low side buffers @25˚C Tamb

Figure 3. Quiescent Current vs. Supply Voltage



BOOTSTRAP DRIVER

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (fig. 4a). In the L6384 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 4b

An internal charge pump (fig. 4b) provides the DMOS driving voltage .

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

CBOOT selection and charging:

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge :

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss .

It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30nC and V_{gate} is 10V, C_{EXT} is 3nF. With C_{BOOT} = 100nF the drop would be 300mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200μA, so if HVG T_{ON} is 5ms, C_{BOOT} has to supply 1μC to C_{EXT}. This charge on a 1μF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current). This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSON} (typical value: 125 Ohm). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1V, if the T_{charge} is 5μs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap Driver

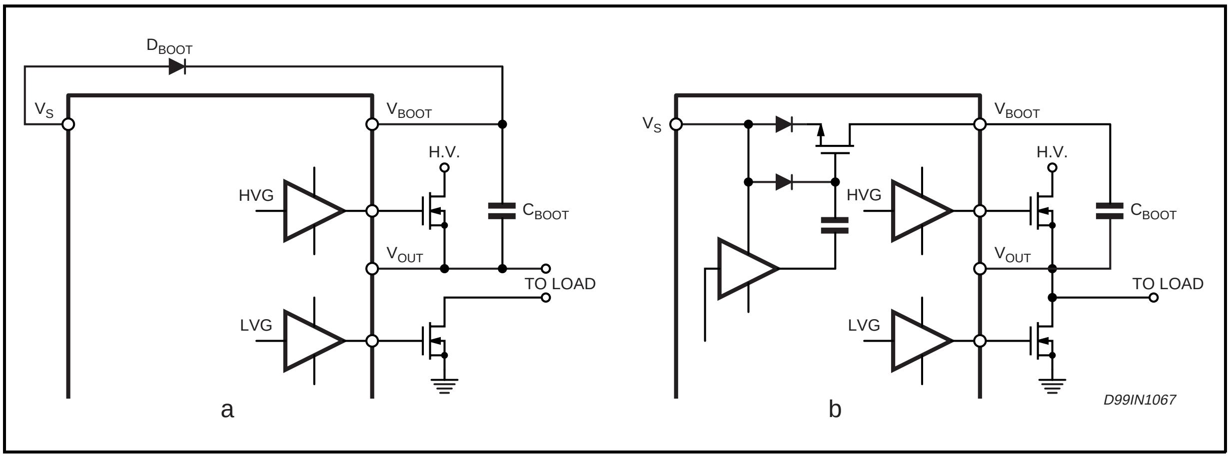


Figure 5. Dead Time vs. Resistance.

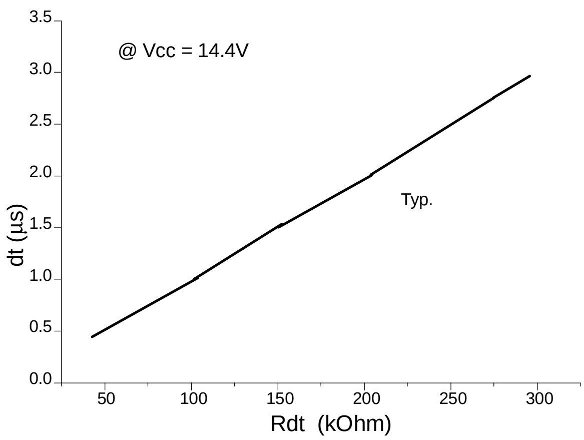


Figure 7. Driver Propagation Delay vs. Temperature.

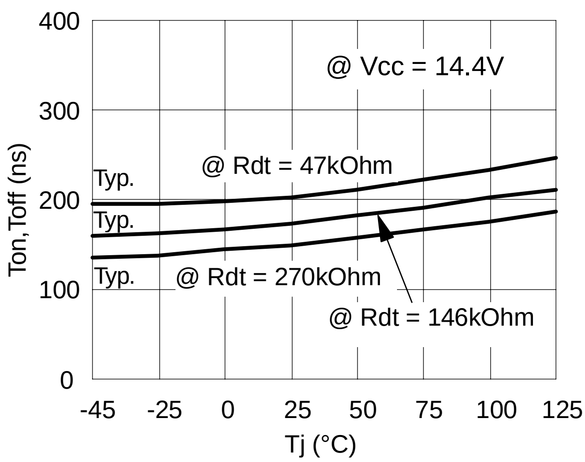


Figure 6. Dead Time vs. Temperature.

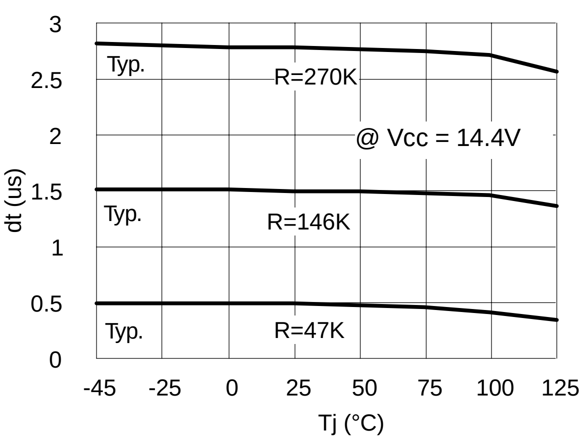


Figure 8. Shutdown Threshold vs. Temperature

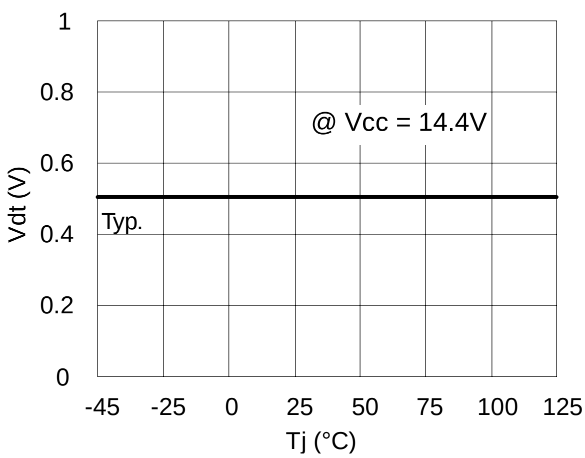


Figure 9. Vcc UV Turn On vs. Temperature

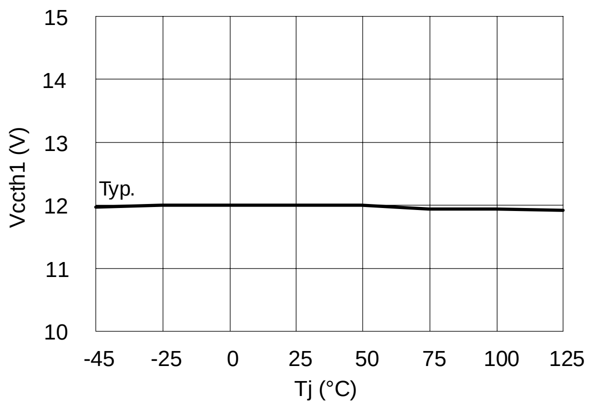


Figure 10. Vcc UV Turn Off vs. Temperature

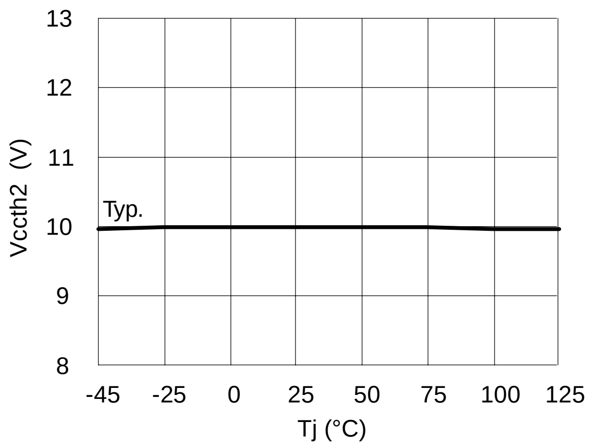


Figure 11. Output Source Current vs. Temperature.

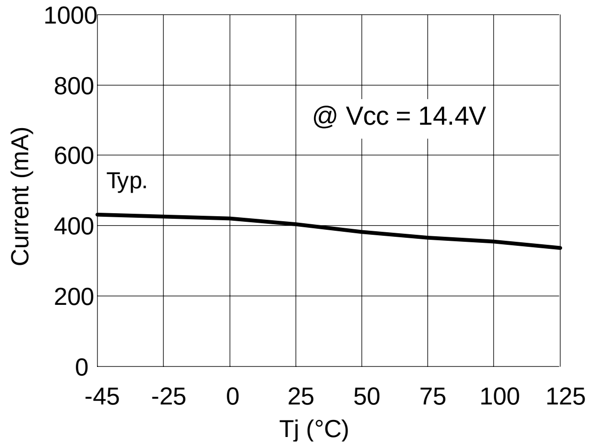
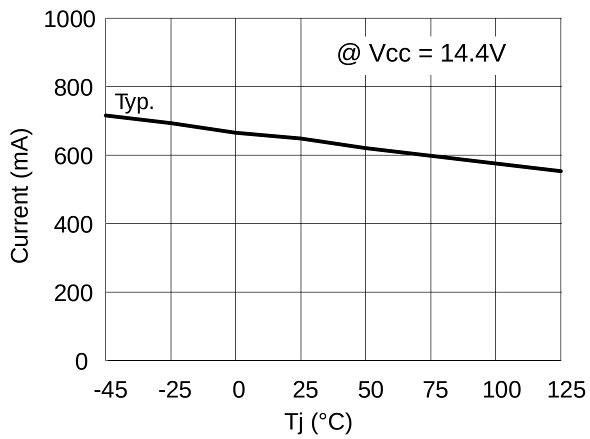
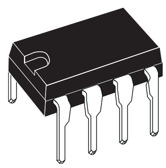


Figure 12. Output Sink Current vs.Temperature

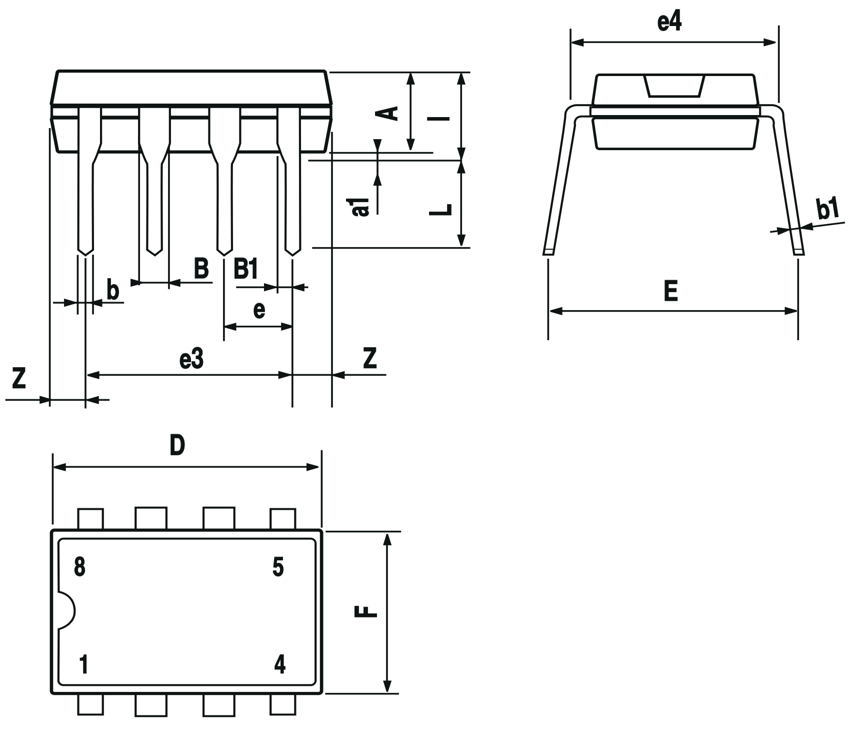


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA



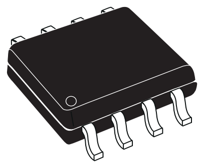
Minidip



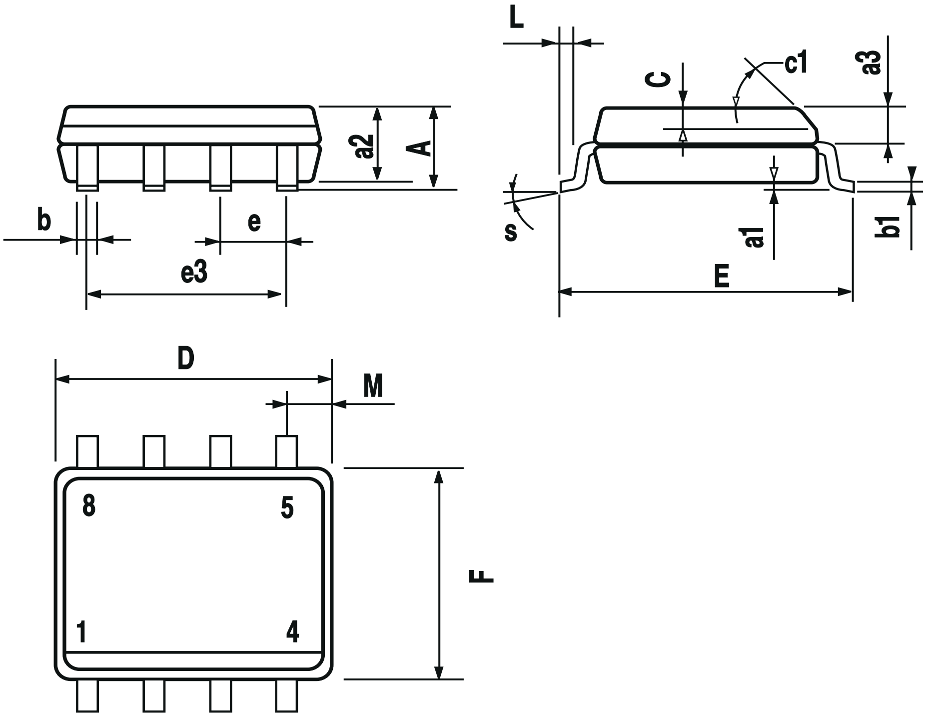
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D (1)	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F (1)	3.8		4.0	0.15		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

(1) D and F do not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch).

OUTLINE AND MECHANICAL DATA



SO8



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