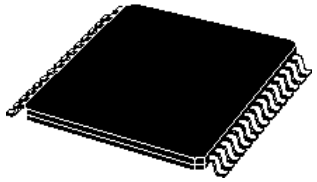
VNH3SP30-E

Automotive fully integrated H-bridge motor driver

Datasheet - production data



MultiPowerSO-30™

Features

Type	$R_{DS(on)}$	I_{out}	V_{ccmax}
VNH3SP30-E	45 mΩ max (per leg)	30 A	40 V

- AEC-Q100 qualified
- Output current: 30 A
- 5 V logic level compatible inputs
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shut down
- Cross-conduction protection
- Linear current limiter
- Very low standby power consumption
- PWM operation up to 10 kHz
- Protection against loss of ground and loss of V_{CC}
- Package: ECOPACK®

Description

The VNH3SP30-E is a full-bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver (HSD) and two low-side switches. The HSD switch is designed using STMicroelectronics proprietary VIPower™ M0-3 technology that efficiently integrates a true Power MOSFET with an intelligent signal/protection circuit on the same die.

The low-side switches are vertical MOSFETs manufactured using STMicroelectronics proprietary EHD ("STripFET™") process. The three circuits are assembled in a MultiPowerSO-30 package on electrically isolated lead frames. This package, specifically designed for the harsh automotive environment, offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design provides superior manufacturability at board level. The input signals IN_A and IN_B can directly interface with the microcontroller to select the motor direction and the brake condition. Pins $DIAG_A/EN_A$ or $DIAG_B/EN_B$, when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The normal operating conditions are explained in the truth table. The speed of the motor can be controlled in all possible conditions by the PWM up to kHz. In all cases, a low level state on the PWM pin will turn off both the LS_A and LS_B switches. When PWM rises to a high level, LS_A or LS_B will turn on again depending on the state of the input pin.

Table 1. Device summary

Package	Order codes
	Tape & reel
MultiPowerSO-30	VNH3SP30TR-E

This is information on a product in full production. www.st.com

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1 Block diagram and pins description

Figure 1. Block diagram

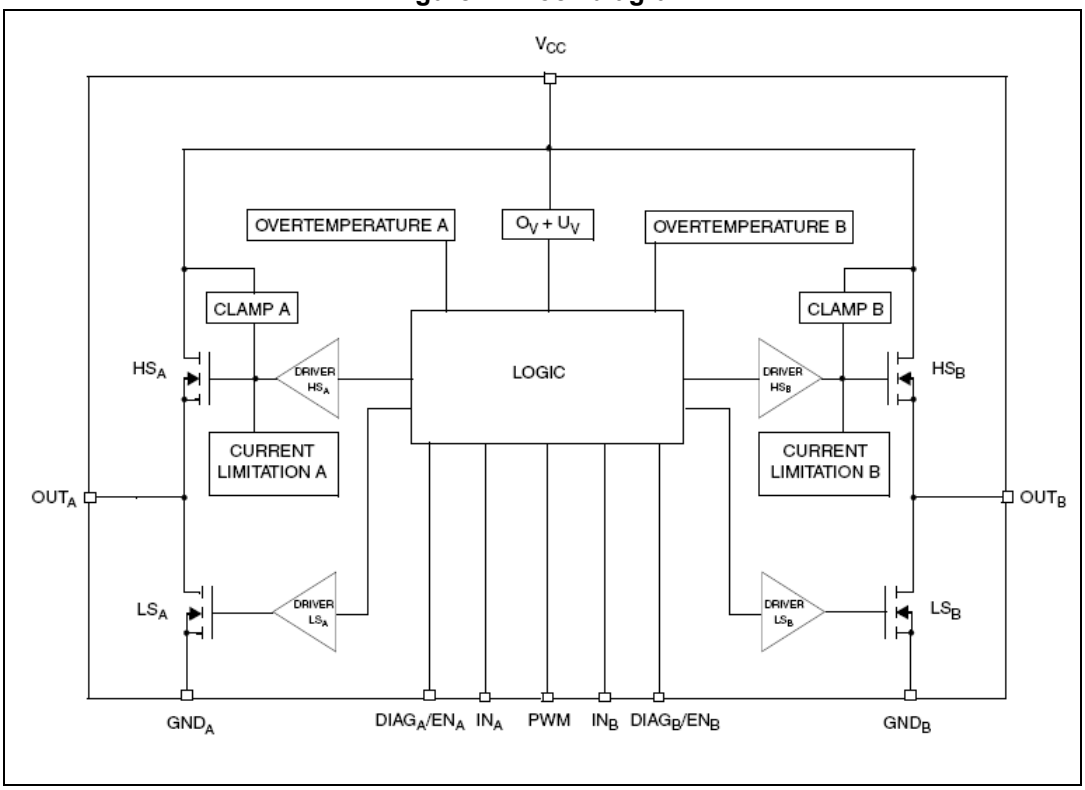


Table 2. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high side and the low side switches according to the truth table
Overvoltage + undervoltage	Shuts down the device outside the range [5.5 V..36 V] for the battery voltage
High side and low side clamp voltage	Protects the high side and the low side switches from the high voltage on the battery line in all configurations for the motor
High side and low side driver	Drives the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge
Linear current limiter	Limits the motor current by reducing the high side switch gate-source voltage when short-circuit to ground occurs
Overtemperature protection	In case of short-circuit with an increase in the junction temperature, shuts down the concerned high side to prevent its degradation and to protect the die
Fault detection	Signals abnormal behavior of the switches in the half-bridge A or B by pulling low the concerned EN_x/$DIAG_x$ pin

Figure 2. Configuration diagram (top view)

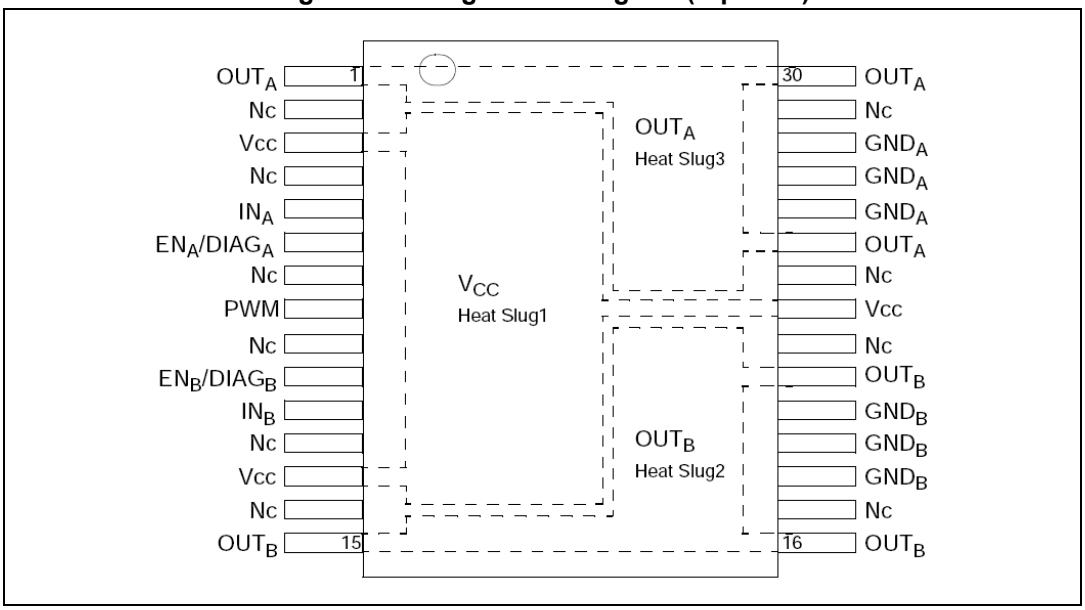


Table 3. Pin definitions and functions

Pin No	Symbol	Function
1, 25, 30	OUT_A, Heat Slug3	Source of high side switch A / Drain of low side switch A
2, 4, 7, 9, 12, 14, 17, 22, 24, 29	NC	Not connected
3, 13, 23	V_{CC}, Heat Slug1	Drain of high side switches and power supply voltage
6	$EN_A/DIAG_A$	Status of high side and low side switches A; open drain output
5	IN_A	Clockwise input
8	PWM	PWM input
11	IN_B	Counter clockwise input
10	$EN_B/DIAG_B$	Status of high side and low side switches B; open drain output
15, 16, 21	OUT_B, Heat Slug2	Source of high side switch B / Drain of low side switch B
26, 27, 28	GND_A	Source of low side switch A(1)
18, 19, 20	GND_B	Source of low side switch B(1)

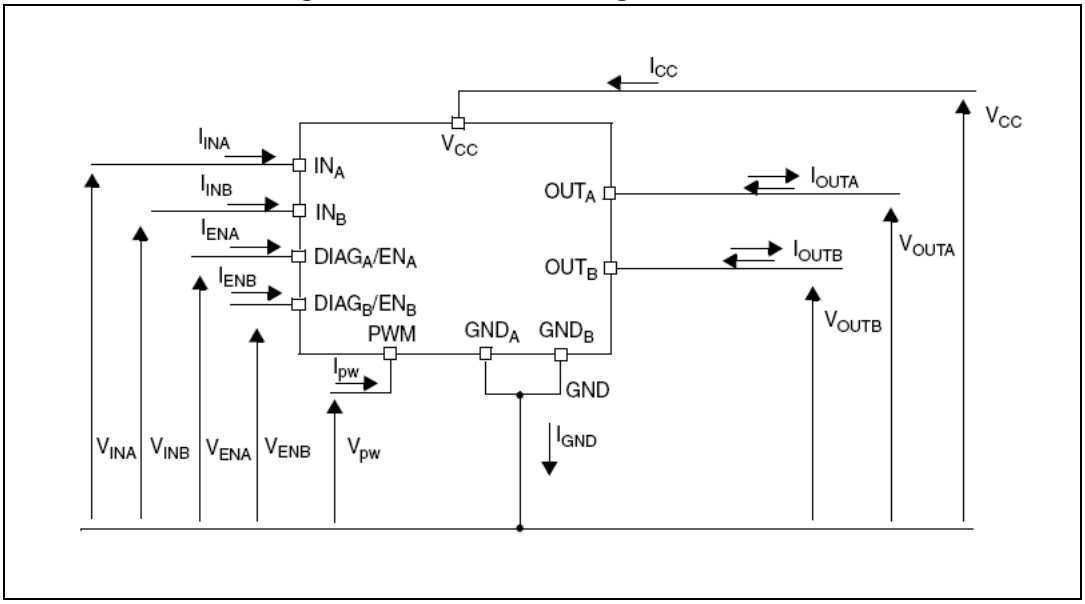
1. GND_A and GND_B must be externally connected together.

Table 4. Pin functions description

Name	Description
V_{CC}	Battery connection
GND_A, GND_B	Power grounds; must always be externally connected together
OUT_A, OUT_B	Power connections to the motor
IN_A, IN_B	Voltage controlled input pins with hysteresis, CMOS compatible. These two pins control the state of the bridge in normal operation according to the truth table (brake to V_{CC}, brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low side FETs are modulated by the PWM signal during their ON phase allowing speed control of the motor.
$EN_A/DIAG_A$, $EN_B/DIAG_B$	Open drain bidirectional logic pins. These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a high side FET or excessive ON state voltage drop across a low side FET), these pins are pulled low by the device (see truth table in fault condition).

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	-0.3...40	V
I_{max1}	Maximum output current (continuous)	30	A
I_R	Reverse output current (continuous)	-30	
I_{IN}	Input current (IN_A and IN_B pins)	±10	mA
I_{EN}	Enable input current ($DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	±10	
I_{pw}	PWM input current	±10	
V_{ESD}	Electrostatic discharge (R = 1.5kΩ, C = 100pF) – logic pins – output pins: OUT_A, OUT_B, V_{CC}	 4 5	 kV kV
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	
T_{STG}	Storage temperature	-55 to 150	

2.2 Electrical characteristics

Vcc = 9 V up to 18 V; -40 °C < T_j < 150 °C, unless otherwise specified.

Table 6. Power section

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		**5.5**		**36**	**V**
I_S	Supply current	Off state: IN_A = IN_B = PWM = 0; T_j = 25°C; V_{CC} = 13V IN_A = IN_B = PWM = 0		20	30 40	µA µA
		On state: IN_A or IN_B = 5V, no PWM			15	mA
R_{ONHS}	Static high side resistance	I_{OUT} = 12A; T_j = 25°C I_{OUT} = 12A; T_j = -40 to 150°C		23	30 60	mΩ
R_{ONLS}	Static low side resistance	I_{OUT} = 12A; T_j = 25°C I_{OUT} = 12A; T_j = -40 to 150°C		11	15 30	
V_f	High side free-wheeling diode forward voltage	I_f = 12 A		0.8	1.1	V
$I_{L(off)}$	High side off state output current (per channel)	T_j = 25°C; V_{OUTX} = EN_X = 0V; V_{CC} = 13V T_j = 125°C; V_{OUTX} = EN_X = 0V; V_{CC} = 13V			3 5	µA

Table 7. Logic inputs (IN_A, IN_B, EN_A, EN_B)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage	Normal operation ($DIAG_X$/EN_X pin acts as an input pin)			1.5	V
V_{IH}	Input high level voltage		3.25			
V_{IHYST}	Input hysteresis voltage		0.5			
V_{ICL}	Input clamp voltage	I_{IN} = 1mA	6	6.8	8	
		I_{IN} = -1mA	-1	-0.7	-0.3	
I_{INL}	Input low current	V_{IN} = 1.5V	1			µA
I_{INH}	Input high current	V_{IN} = 3.25V			10	
V_{DIAG}	Enable output low level voltage	Fault operation ($DIAG_X$/EN_X pin acts as an output pin); I_{EN} = 1mA			0.4	V

Table 8. PWM

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{pwl}	PWM low level voltage				1.5	V
I_{pwl}	PWM low level pin current	V_{pw} = 1.5V	1			µA

Table 8. PWM (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{pwh}	PWM high level voltage		3.25			V
I_{pwh}	PWM high level pin current	V_{pw} = 3.25V			10	µA
$V_{pwhhyst}$	PWM hysteresis voltage		0.5			V
V_{pwcl}	PWM clamp voltage	I_{pw} = 1mA	V_{CC} + 0.3	V_{CC} + 0.7	V_{CC} + 1	
		I_{pw} = -1mA	-5	-3.5	-2	
V_{pwtest}	Test mode PWM pin voltage		-3.5	-2	-0.5	V
I_{pwtest}	Test mode PWM pin current	V_{IN} = -2 V	-2000	-500		µA

Table 9. Switching (V_{CC} = 13 V, R_{LOAD} = 1.1 Ω, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f	PWM frequency		0		10	kHz
$t_{d(on)}$	Turn-on delay time	Input rise time < 1µs (see *Figure 6*)		100	300	µs
$t_{d(off)}$	Turn-off delay time	Input rise time < 1µs (see *Figure 6*)		85	255	
t_r	Rise time	(see *Figure 5*)		1.5	3	
t_f	Fall time	(see *Figure 5*)		2	5	
t_{DEL}	Delay time during change of operating mode	(see *Figure 4*)		600	1800	

Table 10. Protection and diagnostic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{USD}	Undervoltage shut-down				5.5	V
V_{OV}	Overvoltage shut-down		36	43		
I_{LIM}	Current limitation		30	45		A
T_{TSD}	Thermal shut-down temperature	V_{IN} = 3.25V	150	170	200	°C
T_{TR}	Thermal reset temperature		135			
T_{HYST}	Thermal hysteresis		7	15		

Figure 4. Definition of the delay time measurement

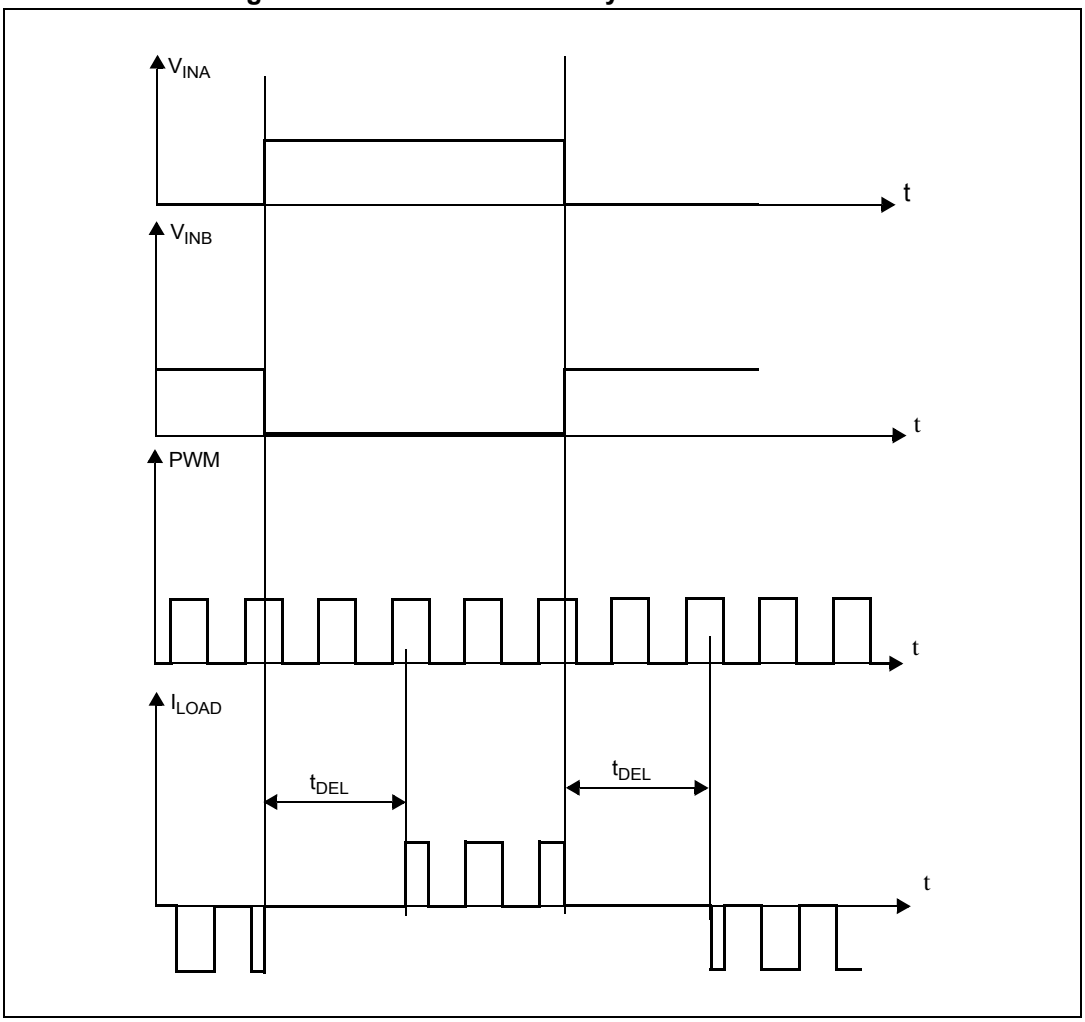


Figure 5. Definition of the low side switching times

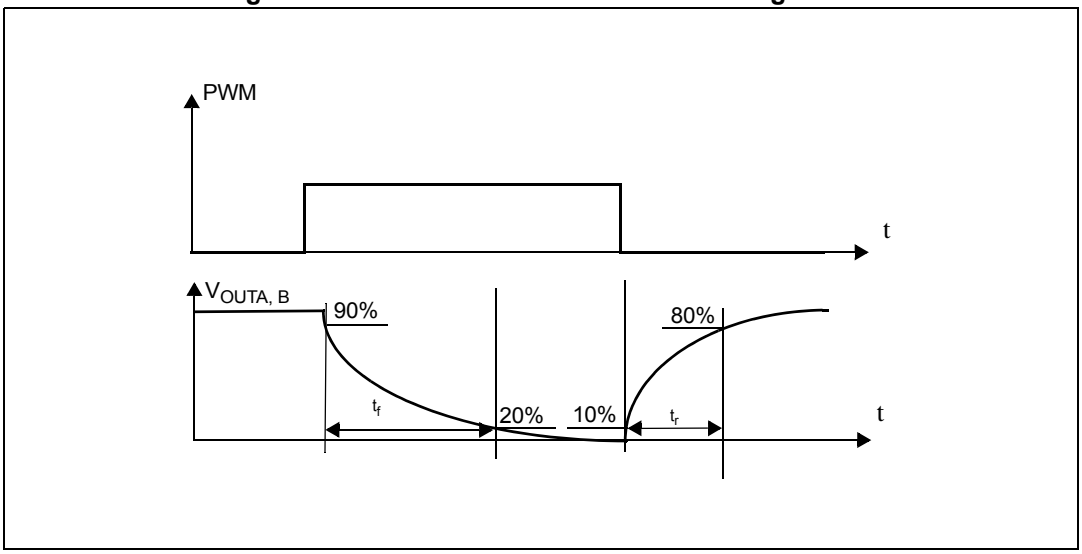


Figure 6. Definition of the high side switching times

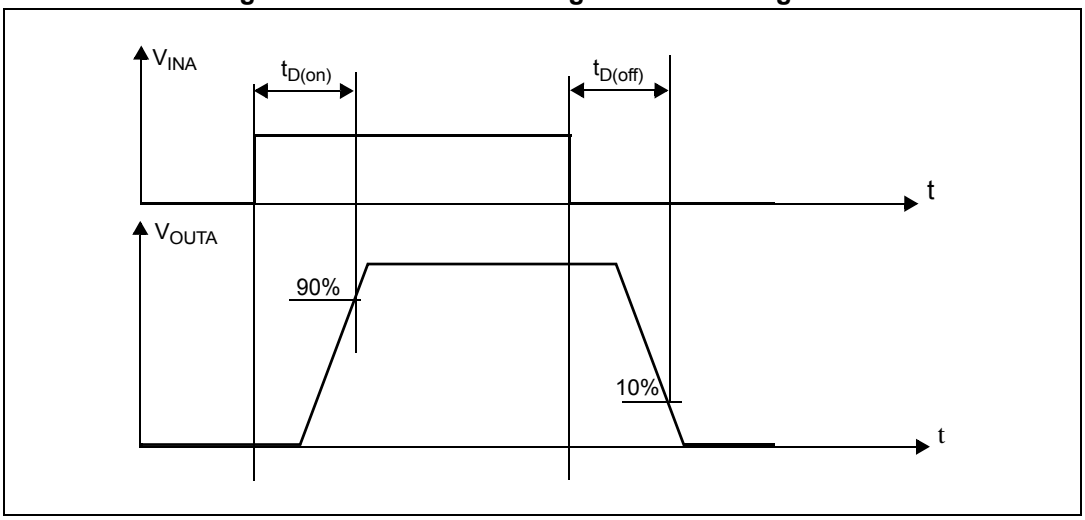


Table 11. Truth table in normal operating conditions

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B	Operating mode
1	1	1	1	H	H	Brake to V_{CC}
	0				L	Clockwise (CW)
0	1			L	H	Counterclockwise (CCW)
	0				L	Brake to GND

Table 12. Truth table in fault conditions (detected on OUT_A)

IN_A	IN_B	$DIAG_A/EN_A$	$DIAG_B/EN_B$	OUT_A	OUT_B
1	1	0	1	OPEN	H
	0				L
0	1				H
	0				L
X	X		0		OPEN
	1		1		H
	0				L
		Fault Information		Protection Action	

Note: Note that saturation detection on the low side power MOSFET is possible only if the impedance of the short-circuit from the output to the battery is less than 100 mΩ when the device is supplied with a battery voltage of 13.5 V.

Table 13. Electrical transient requirements (part 1)

ISO T/R - 7637/1 Test pulse	Test level I	Test level II	Test level III	Test level IV	Test level delays and impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1µs, 50Ω
3b	+25V	+50V	+75V	+100V	
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

Table 14. Electrical transient requirements (part 2)

ISO T/R - 7637/1 Test pulse	Test level results I	Test level results II	Test level results III	Test level results IV
1	C	C	C	C
2				
3a				
3b				
4				
5(1)		E	E	E

1. For load dump exceeding the above value a centralized suppressor must be adopted

Table 15. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.3 Electrical characteristics curves

Figure 7. On state supply current

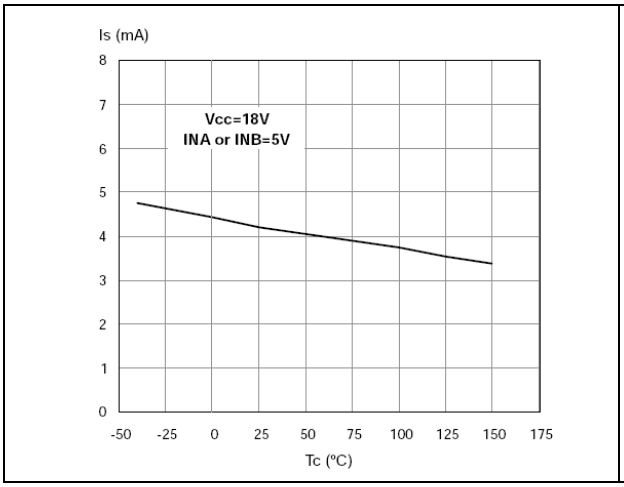


Figure 8. Off state supply current

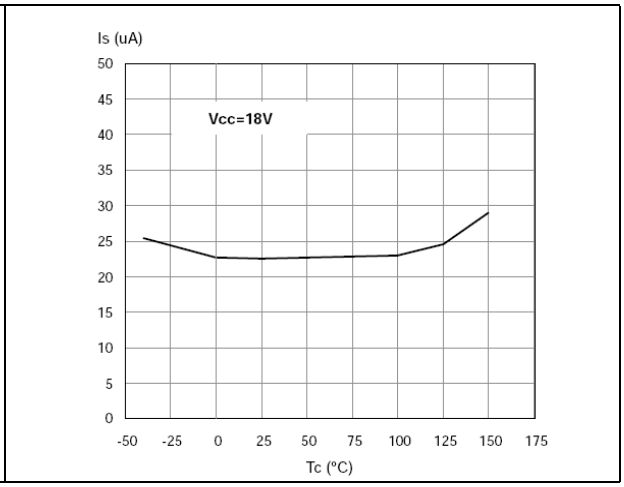


Figure 9. High level input current

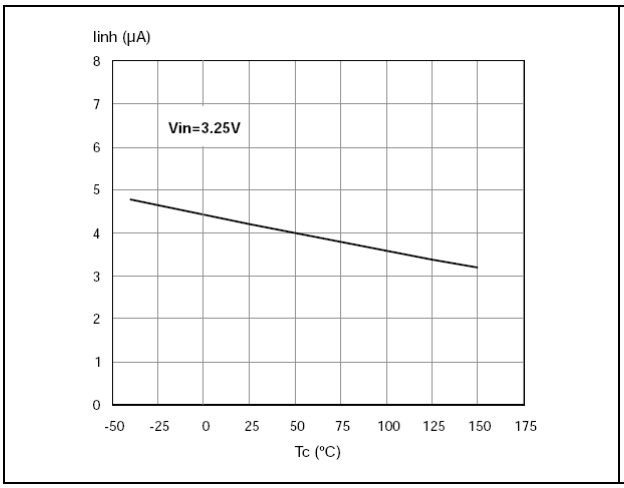


Figure 10. Input clamp voltage

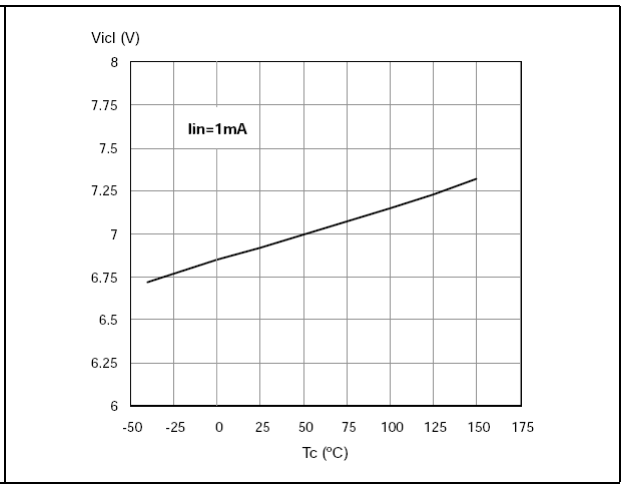


Figure 11. Input high level voltage

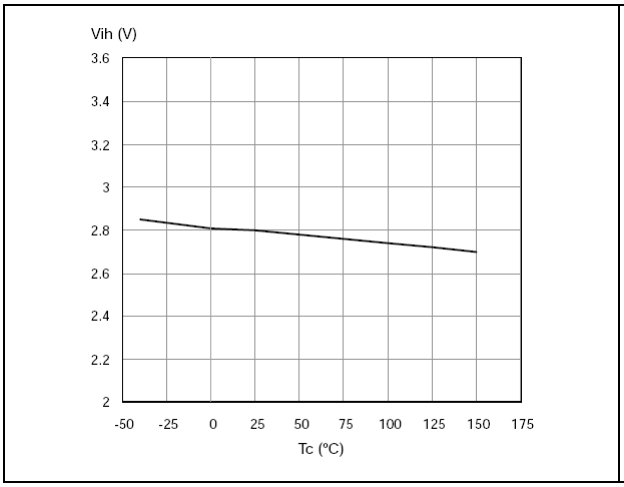


Figure 12. Input low level voltage

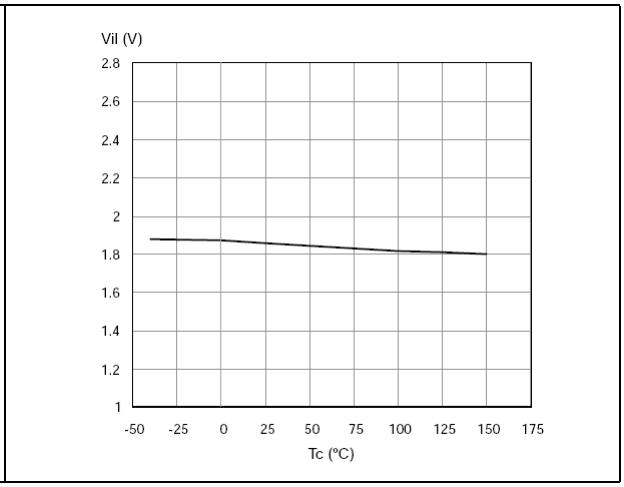


Figure 13. Input hysteresis voltage

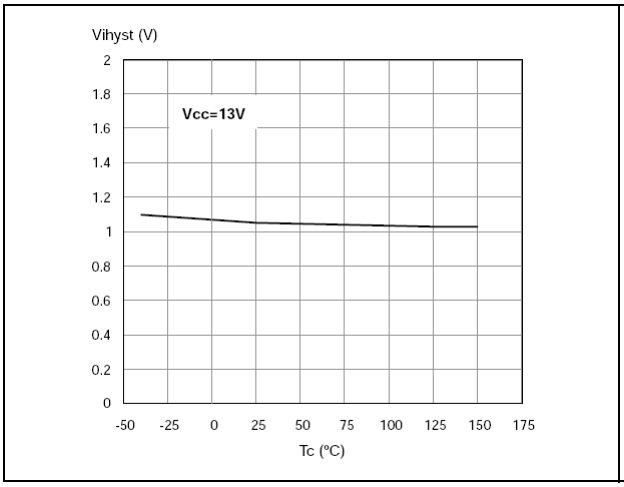


Figure 14. High level enable pin current

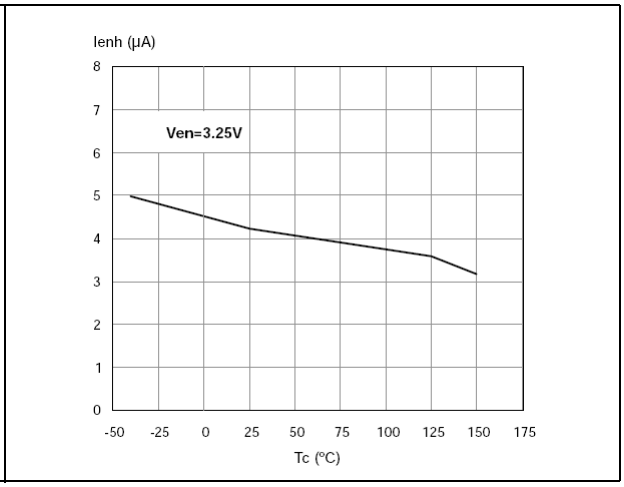


Figure 15. Delay time during change of operation mode

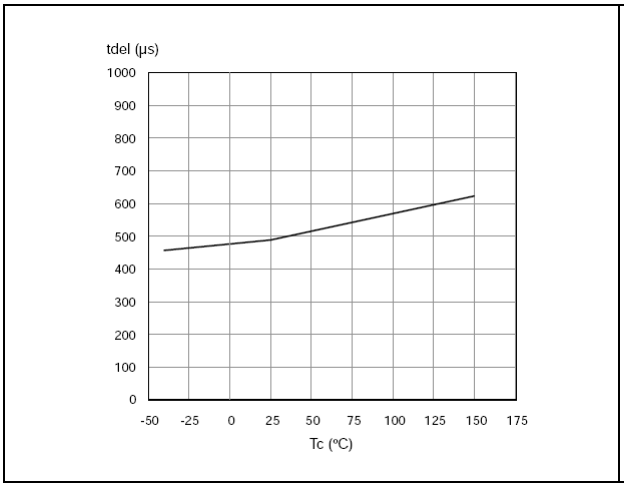


Figure 16. Enable clamp voltage

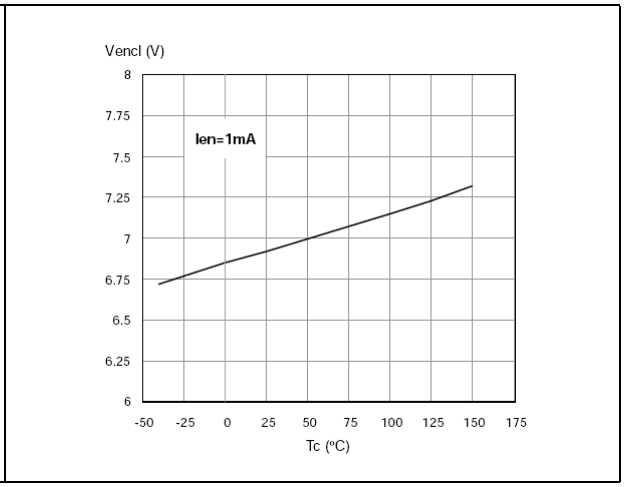


Figure 17. High level enable voltage

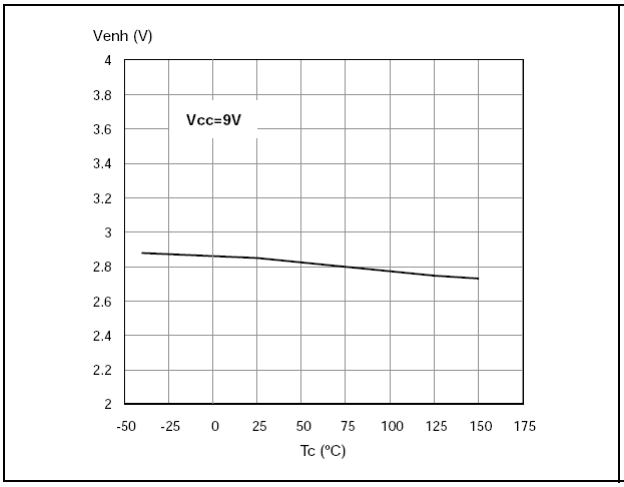


Figure 18. Low level enable voltage

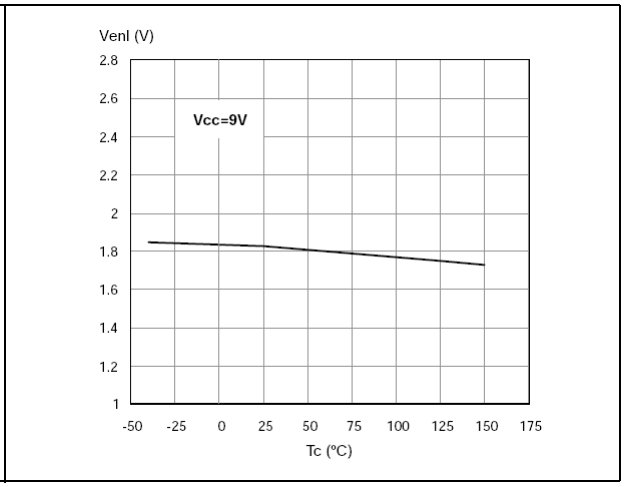


Figure 19. PWM high level voltage

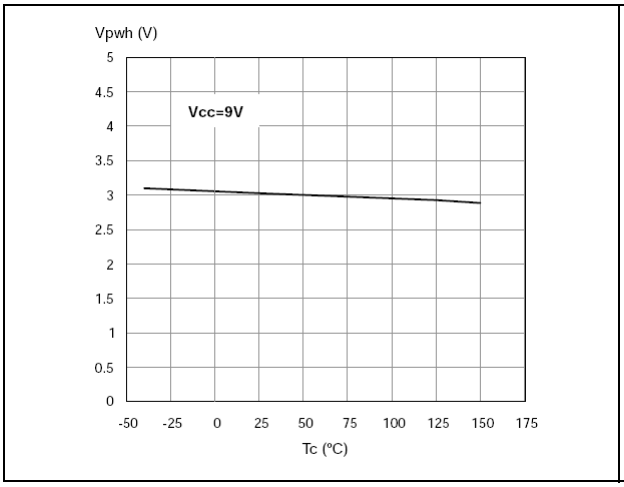


Figure 20. PWM low level voltage

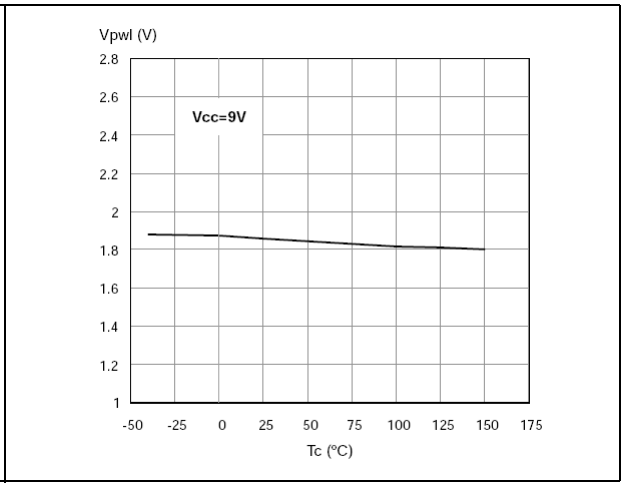


Figure 21. PWM high level current

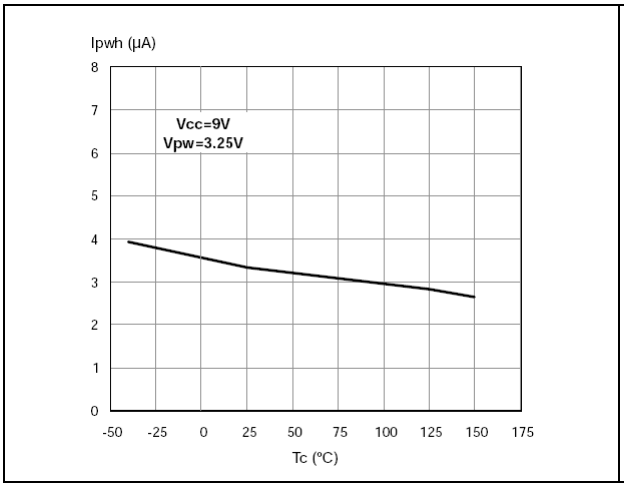


Figure 22. Overvoltage shutdown

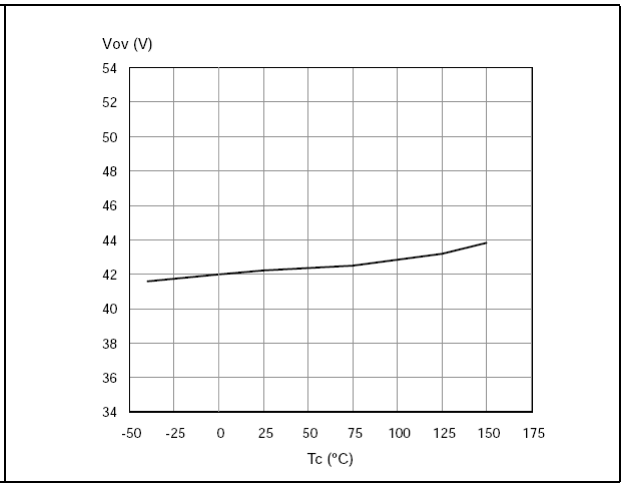


Figure 23. Undervoltage shutdown

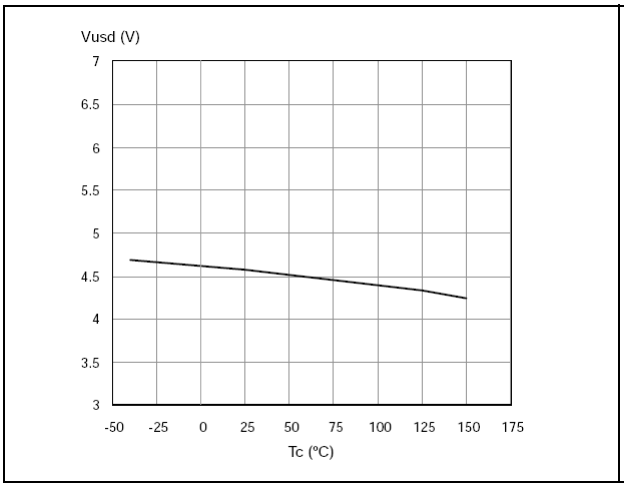


Figure 24. Current limitation

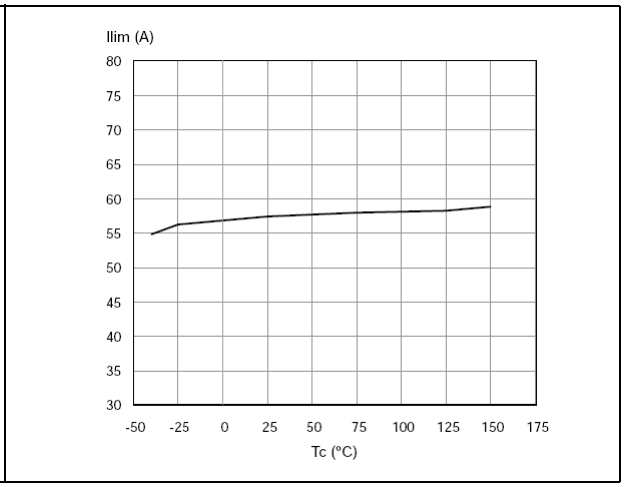


Figure 25. On state high side resistance vs T_{case}

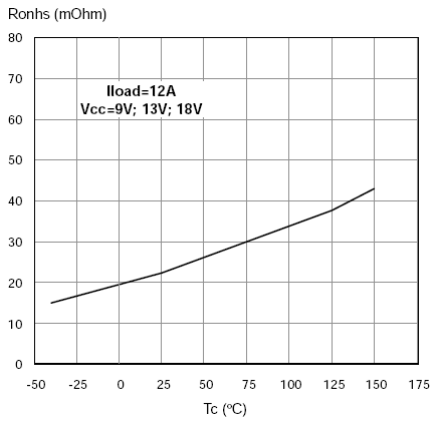


Figure 26. On state low side resistance vs T_{case}

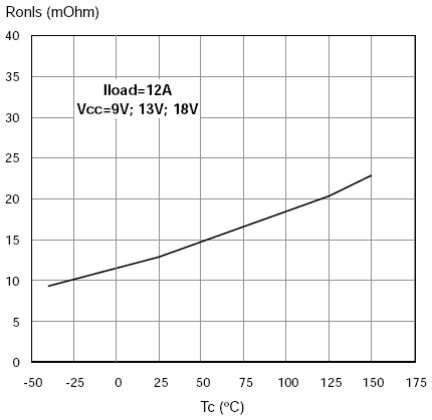


Figure 27. On state high side resistance vs Vcc

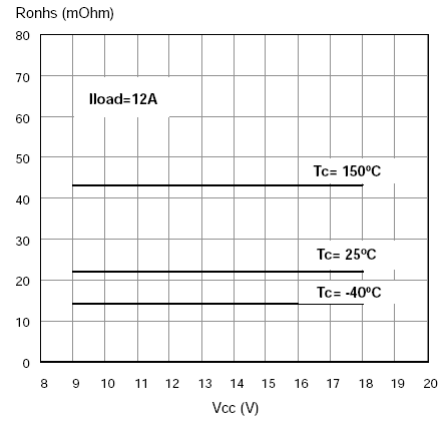


Figure 28. On state low side resistance vs Vcc

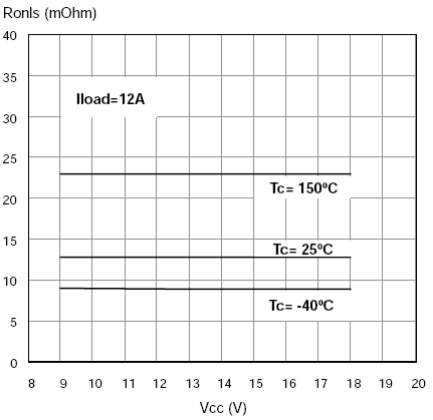


Figure 29. Output voltage rise time

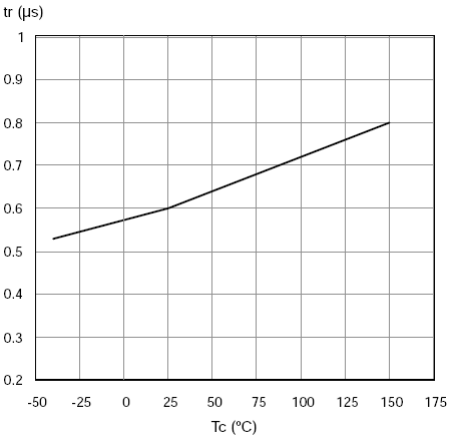


Figure 30. Output voltage fall time

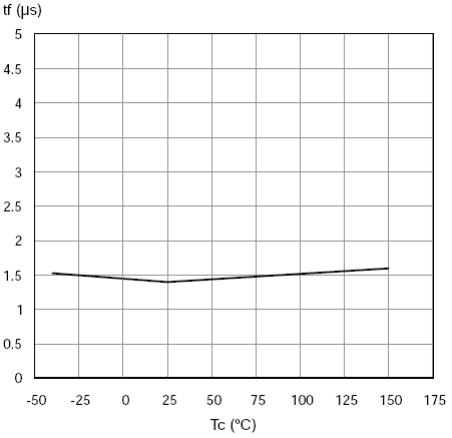


Figure 31. Enable output low level voltage

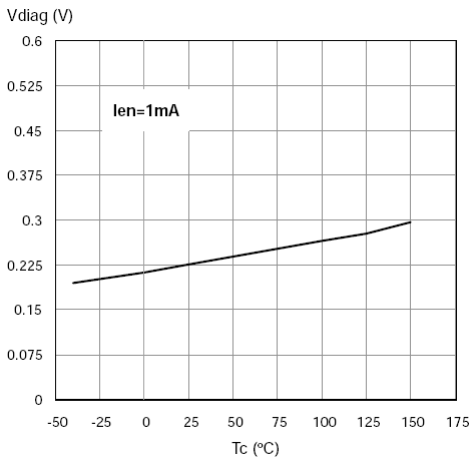
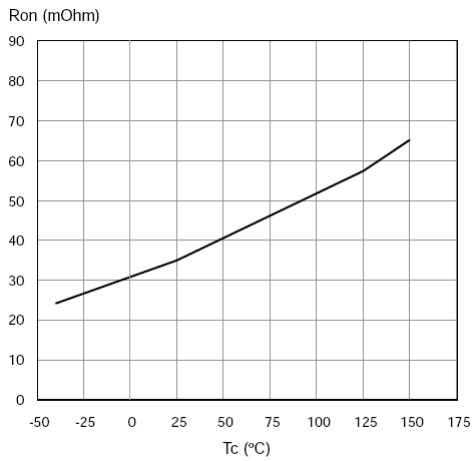


Figure 32. ON state leg resistance

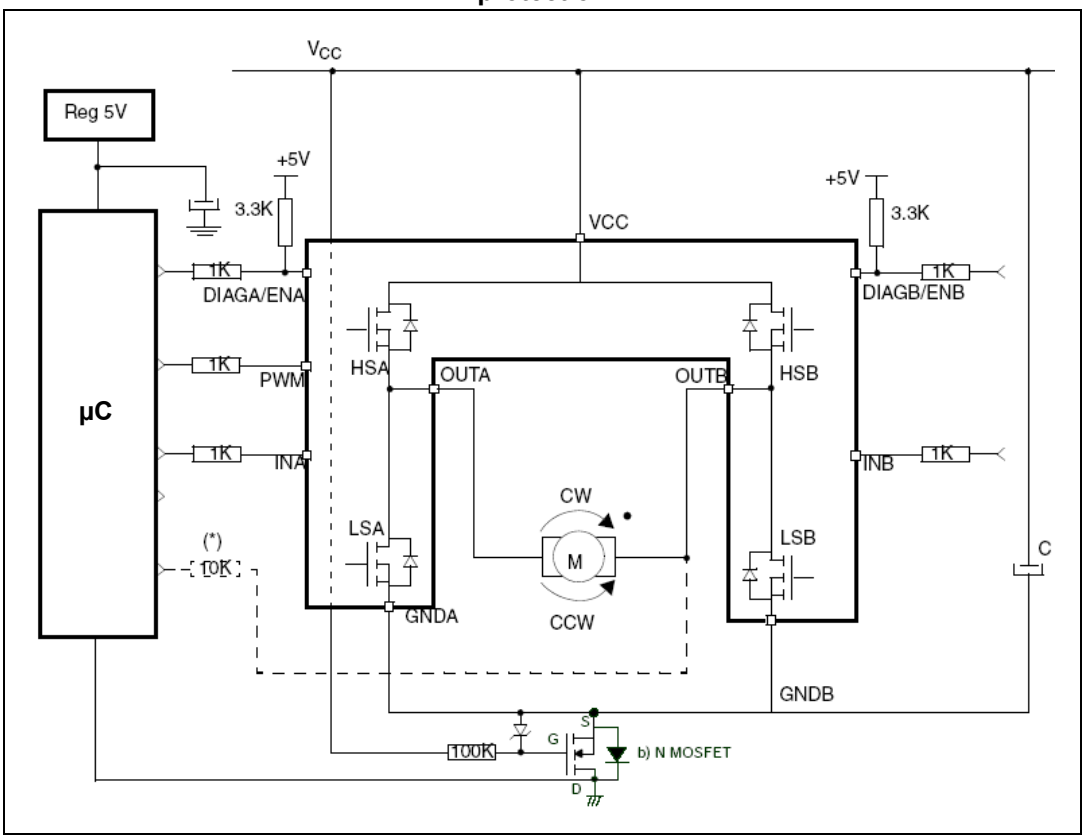


3 Application information

In normal operating conditions the $DIAG_X/EN_X$ pin is considered as an input pin by the device. This pin must be externally pulled high.

PWM pin usage: In all cases, a “0” on the PWM pin will turn off both LS_A and LS_B switches. When PWM rises back to “1”, LS_A or LS_B turn on again depending on the input pin state.

Figure 33. Typical application circuit for DC to 10 kHz PWM operation short circuit protection



Note: The value of the blocking capacitor (C) depends on the application conditions and defines voltage and current ripple onto the supply line at PWM operation. Stored energy of the motor inductance may fly back into the blocking capacitor, if the bridge driver goes into tri-state. This causes a hazardous overvoltage if the capacitor is not big enough. As a basic orientation, 500 µF per 10 A load current is recommended.

In case of a fault condition, the $DIAG_X/EN_X$ pin is considered an output pin by the device.

The fault conditions are:

- overtemperature on one or both high sides
- short to battery condition on the output (saturation detection on the low side power MOSFET)

Possible origins of fault conditions may be:

- OUT_A is shorted to ground → overtemperature detection on high side A.
- OUT_A is shorted to V_{CC} → low side power MOSFET saturation detection[(a)].

When a fault condition is detected, the user can know which power element is in fault by monitoring the IN_A, IN_B, $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn on the respective output (OUT_X) again, the input signal must rise from low to high level.

3.1 Reverse battery protection

Three possible solutions can be considered:

1. a Schottky diode D connected to V_{CC} pin
2. an N-channel MOSFET connected to the GND pin (see *Figure 33: Typical application circuit for DC to 10 kHz PWM operation short circuit protection on page 19*)
3. a P-channel MOSFET connected to the V_{CC} pin

The device sustains no more than -30 A in reverse battery conditions because of the two body diodes of the power MOSFETs. Additionally, in reverse battery condition the I/Os of VNH3SP30-E will be pulled down to the V_{CC} line (approximately -1.5 V). A series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If I_{Rmax} is the maximum target reverse current through µC I/Os, the series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

3.2 Open load detection in Off mode

It is possible for the microcontroller to detect an open load condition by adding a simply resistor (for example, 10 kΩ) between one of the outputs of the bridge (for example, OUT_B) and one microcontroller input. A possible sequence of inputs and enable signals is the following: IN_A = 1, IN_B = X, EN_A = 1, EN_B = 0.

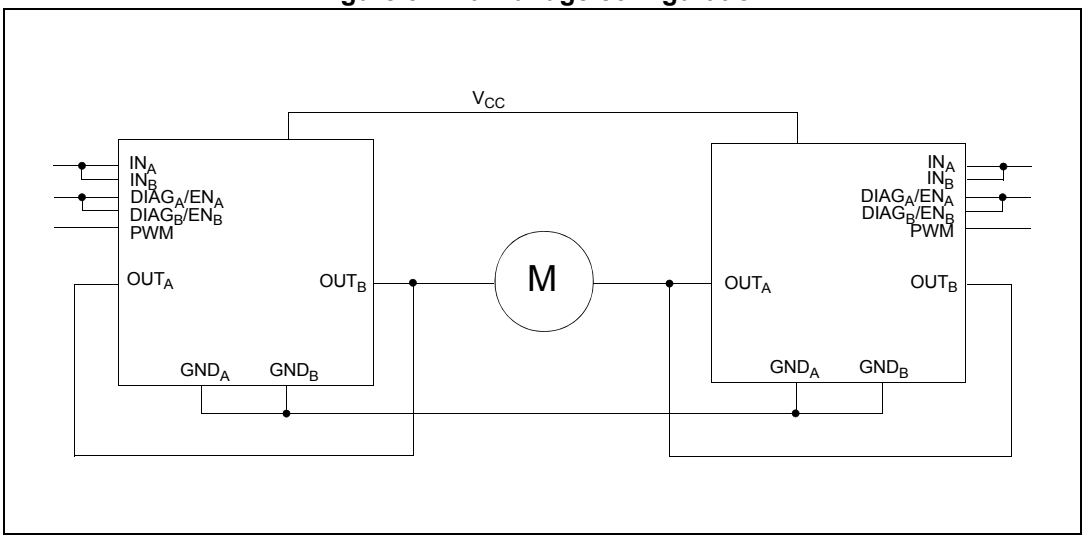
- normal condition: OUT_A = H and OUT_B = H
- open load condition: OUT_A = H and OUT_B = L: In this case the OUT_B pin is internally pulled down to GND. This condition is detected on OUT_B pin by the microcontroller as an open load fault.

a. An internal operational amplifier compares the drain-source MOSFET voltage with the internal reference (2.7 V typ.). The relevant low side power MOS is switched off when its drain-source voltage exceeds the reference voltage.

3.3 Test mode

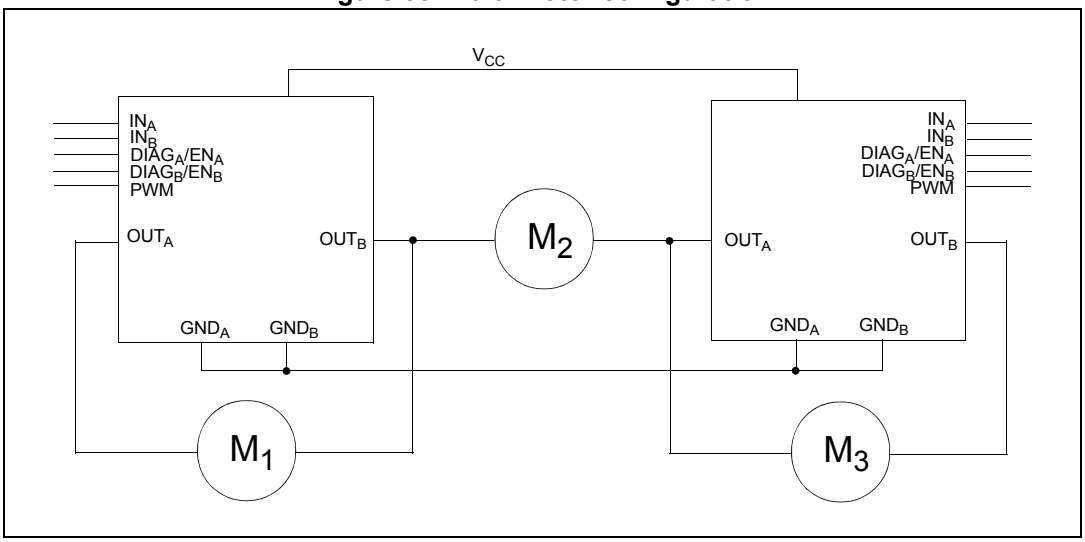
The PWM pin can be used to test the load connection between two half-bridges. In the Test mode (V_{pwm} = -2 V) the internal power MOS gate drivers are disabled. The IN_A or IN_B inputs can be used to turn on the high side A or B, respectively, in order to connect one side of the load at V_{CC} voltage. The check of the voltage on the other side of the load can be used to verify the continuity of the load connection. In case of load disconnection, the DIADx/ENx pin corresponding to the faulty output is pulled down.

Figure 34. Half-bridge configuration



Note: The VNH3SP30-E can be used as a high power half-bridge driver achieving an On resistance per leg of 22.5 mΩ.

Figure 35. Multi-motor configuration



Note: The VNH3SP30-E can easily be designed in multi-motor driving applications such as seat positioning systems, where only one motor must be driven at a time. The $DIAG_X/EN_X$ pins allow the unused half-bridges to be put into high impedance.

Figure 36. Waveforms in full bridge operation (part 1)

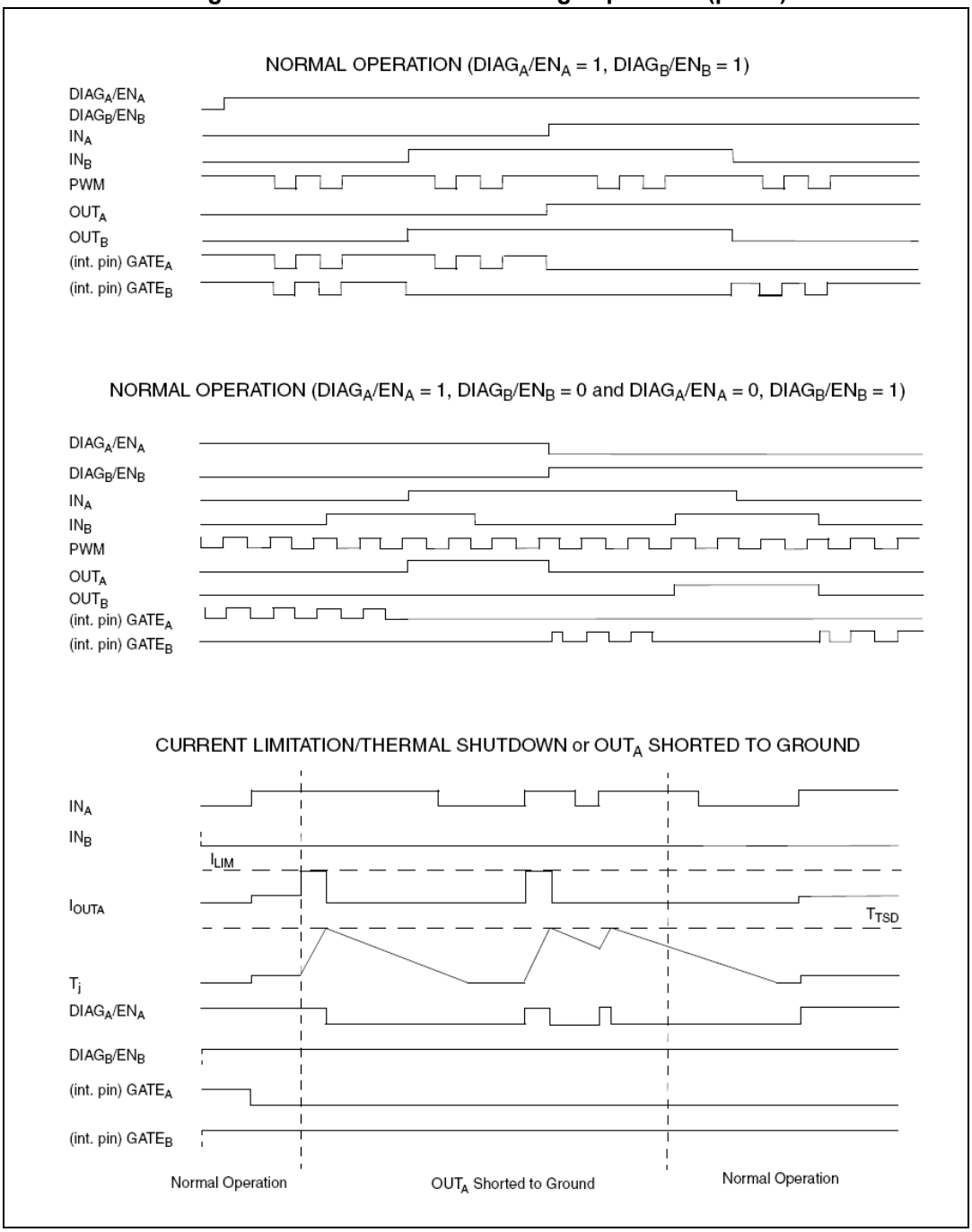
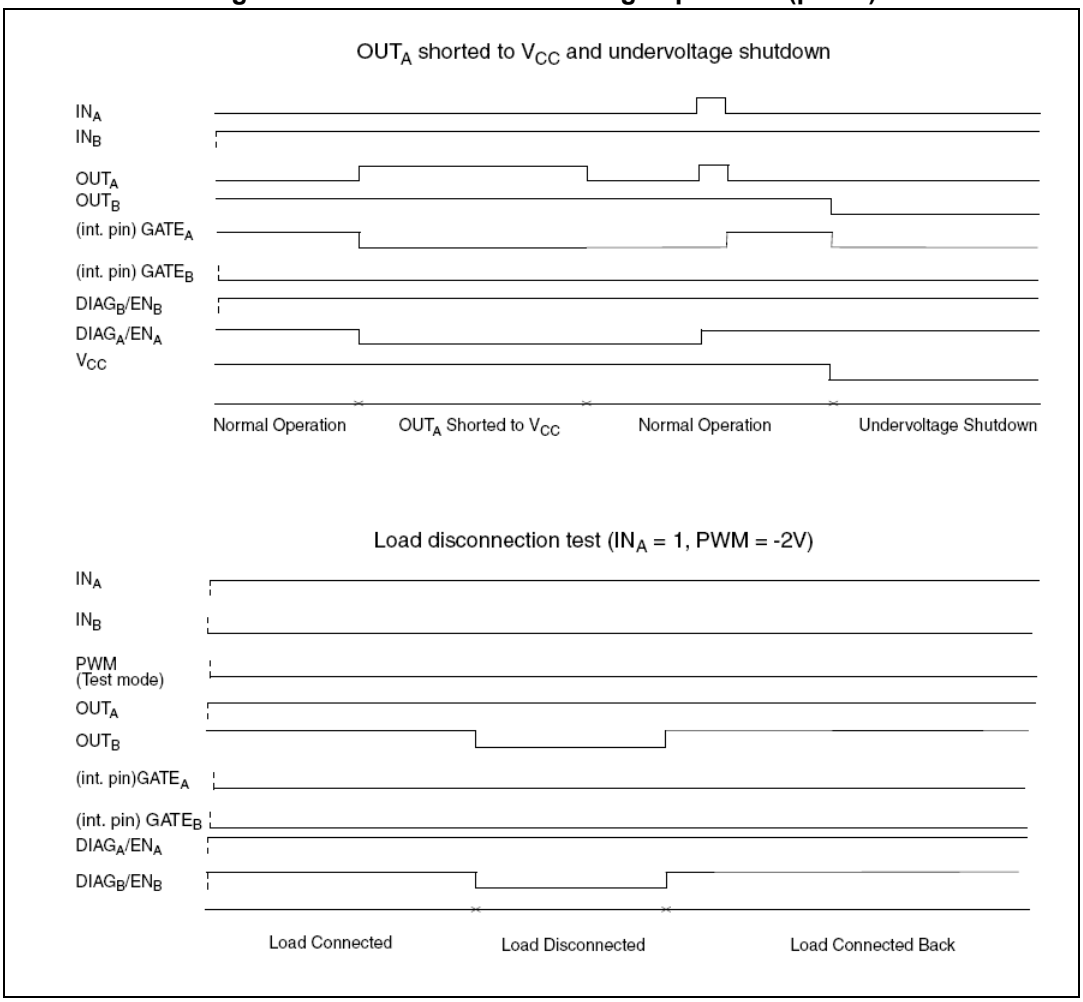


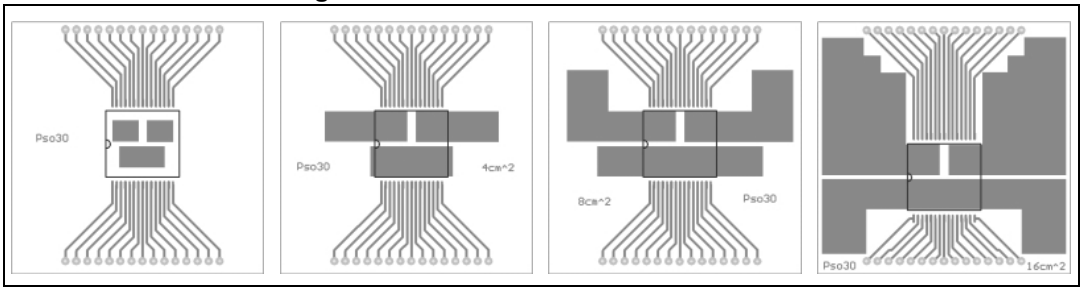
Figure 37. Waveforms in full bridge operation (part 2)



4 Package and PCB thermal data

4.1 MultiPowerSO-30 thermal data

Figure 38. MultiPowerSO-30™ PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 µm, Copper areas: from minimum pad layout to 16 cm^2).

Figure 39. Chipset configuration

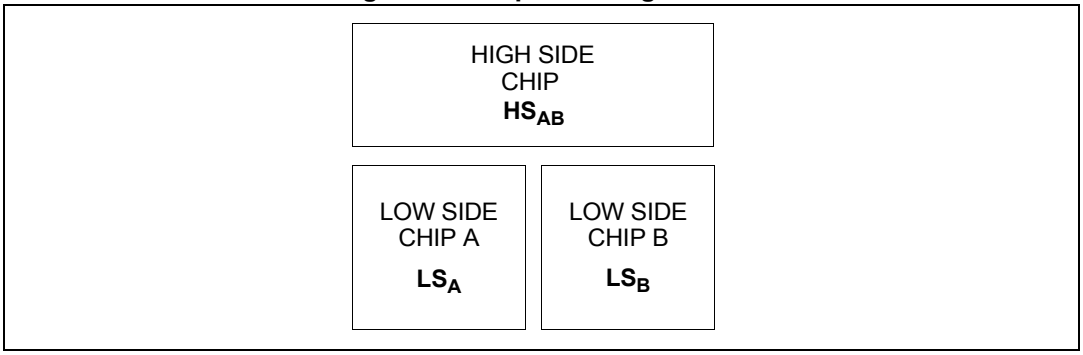
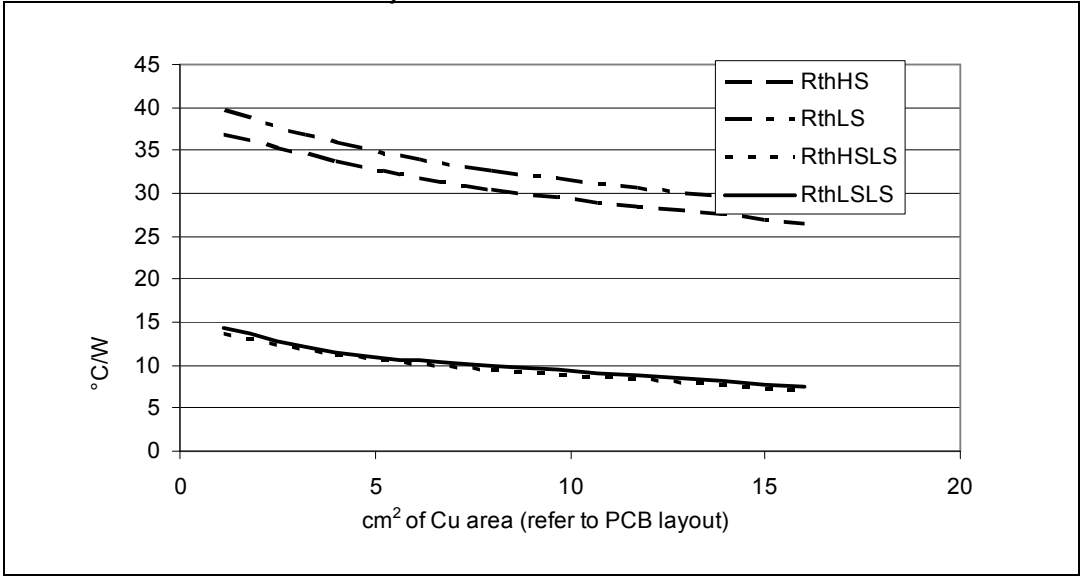


Figure 40. Auto and mutual $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition



4.1.1 Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

Table 16. Thermal calculation in clockwise and anti-clockwise operation in steady-state mode

HS_A	HS_B	LS_A	LS_B	T_{jHSAB}	T_{jLSA}	T_{jLSB}
ON	OFF	OFF	ON	$P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLSLS} + T_{amb}$	$P_{dHSA} \times R_{thHSLS} + P_{dLSB} \times R_{thLS} + T_{amb}$
OFF	ON	ON	OFF	$P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLS} + T_{amb}$	$P_{dHSB} \times R_{thHSLS} + P_{dLSA} \times R_{thLSLS} + T_{amb}$

4.1.2 Thermal resistances definition (values according to the PCB heatsink area)

R_{thHS} = R_{thHSA} = R_{thHSB} = High Side Chip Thermal Resistance Junction to Ambient (HS_A or HS_B in ON state)

R_{thLS} = R_{thLSA} = R_{thLSB} = Low Side Chip Thermal Resistance Junction to Ambient

R_{thHSLS} = $R_{thHSALSB}$ = $R_{thHSBLSA}$ = Mutual Thermal Resistance Junction to Ambient between High Side and Low Side Chips

R_{thLSLS} = $R_{thLSALSB}$ = Mutual Thermal Resistance Junction to Ambient between Low Side Chips

4.1.3 Thermal calculation in transient mode[(b)]

T_{jHSAB} = $Z_{thHS} \times P_{dHSAB} + Z_{thHSLS} \times (P_{dLSA} + P_{dLSB}) + T_{amb}$

T_{jLSA} = $Z_{thHSLS} \times P_{dHSAB} + Z_{thLS} \times P_{dLSA} + Z_{thLSLS} \times P_{dLSB} + T_{amb}$

T_{jLSB} = $Z_{thHSLS} \times P_{dHSAB} + Z_{thLSLS} \times P_{dLSA} + Z_{thLS} \times P_{dLSB} + T_{amb}$

4.1.4 Single pulse thermal impedance definition (values according to the PCB heatsink area)

Z_{thHS} = High Side Chip Thermal Impedance Junction to Ambient

Z_{thLS} = Z_{thLSA} = Z_{thLSB} = Low Side Chip Thermal Impedance Junction to Ambient

Z_{thHSLS} = $Z_{thHSABLSA}$ = $Z_{thHSABLSB}$ = Mutual Thermal Impedance Junction to Ambient between High Side and Low Side Chips

Z_{thLSLS} = $Z_{thLSALSB}$ = Mutual Thermal Impedance Junction to Ambient between Low Side Chips

b. Calculation is valid in any dynamic operating condition. P_d values set by user.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_p / T$

Figure 41. MultiPowerSO-30 HSD thermal impedance junction ambient single pulse

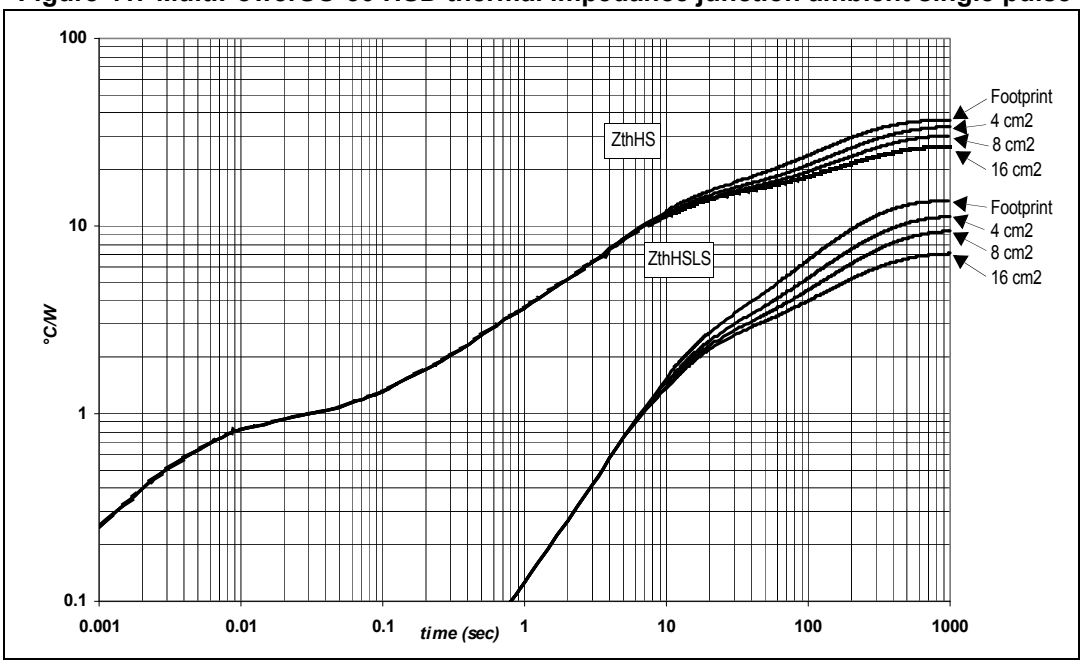


Figure 42. MultiPowerSO-30 LSD thermal impedance junction ambient single pulse

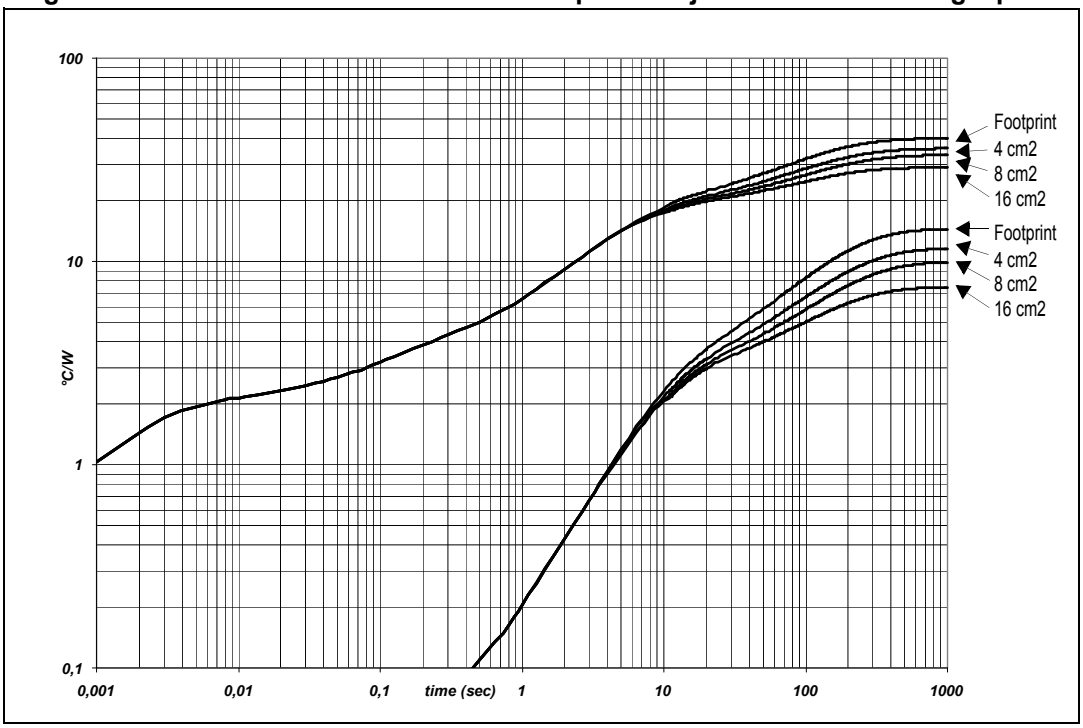


Figure 43. Thermal fitting model of an H-bridge in MultiPowerSO-30

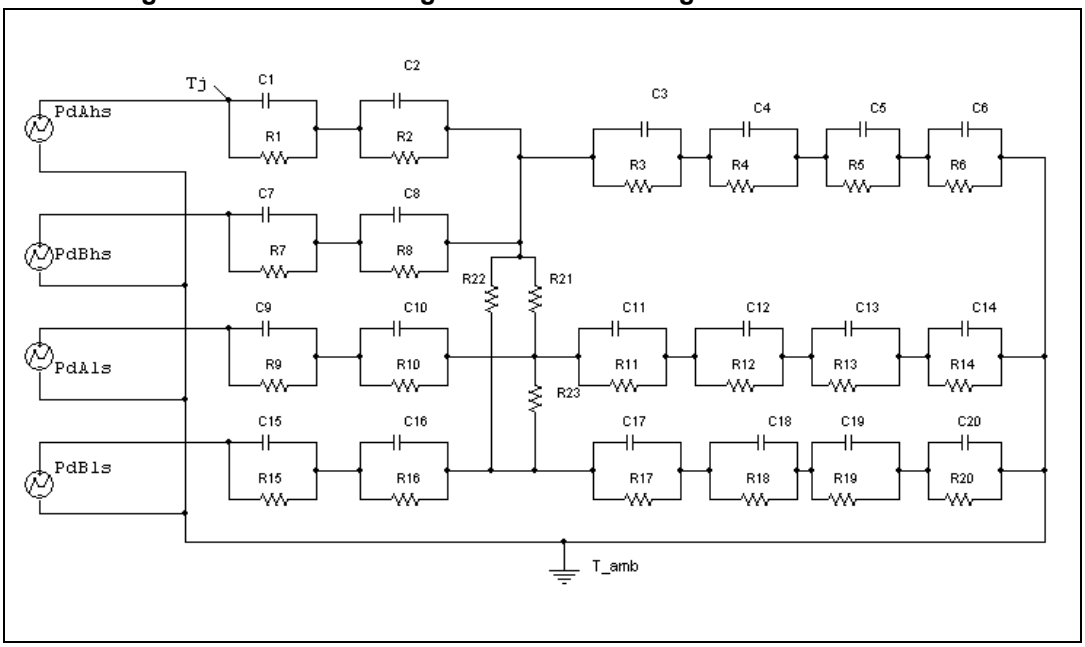


Table 17. Thermal parameters(1)

Area/island (cm^2)	Footprint	4	8	16
R1 = R7 (°C/W)	0.05			
R2 = R8 (°C/W)	0.3			
R3 (°C/W)	0.5			
R4 (°C/W)	1.3			
R5 (°C/W)	14			
R6 (°C/W)	44.7	39.1	31.6	23.7
R9 = R10= R15= R16 (°C/W)	0.6			
R11 = R17 (°C/W)	0.8			
R12 = R18 (°C/W)	1.5			
R13 = R19 (°C/W)	20			
R14 = R20 (°C/W)	46.9	36.1	30.4	20.8
R21 = R22 = R23 (°C/W)	115			
C1 = C7 = C9 = C15 (W.s/°C)	0.001			
C2 = C8 (W.s/°C)	0.005			
C3 = (W.s/°C)	0.02			
C4 = C13 = C19 (W.s/°C)	0.3			
C5 (W.s/°C)	0.6			
C6 (W.s/°C)	5	7	9	11
C10 = C11= C16 = C17 (W.s/°C)	0.003			

Table 17. Thermal parameters[1] (continued)

Area/island (cm^2)	Footprint	4	8	16
C12 = C18 (W.s/°C)	0.075			
C14 = C20 (W.s/°C)	2.5	3.5	4.5	5.5

1. A blank space means that the value is the same as the previous one.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 MultiPowerSO-30 package information

Figure 44. MultiPowerSO-30 package outline

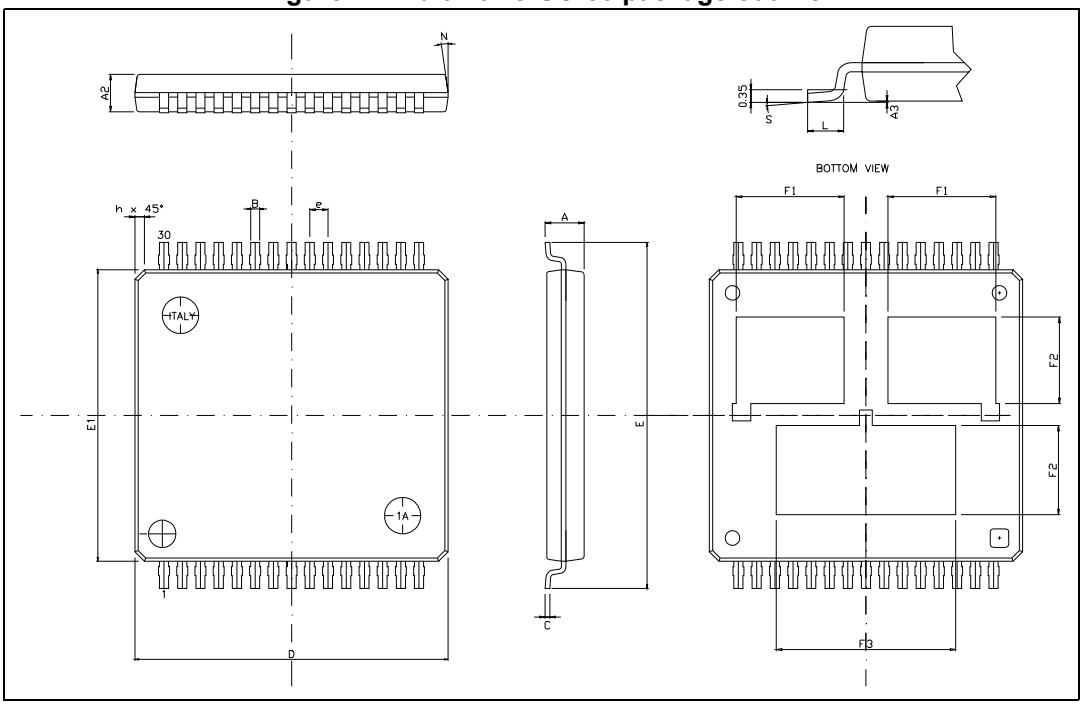
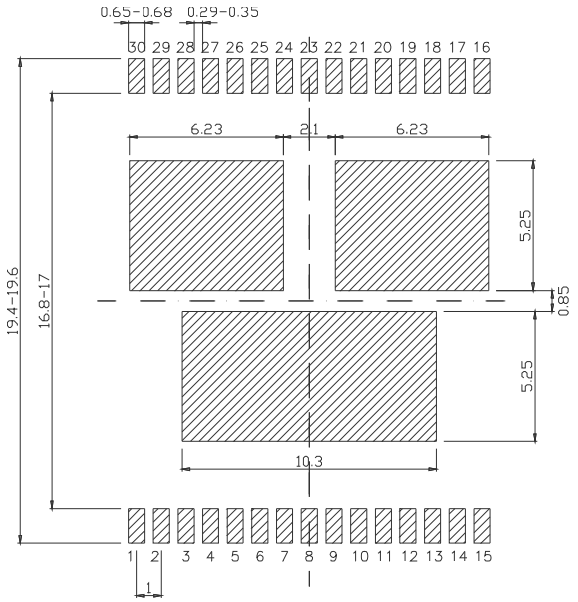


Table 18. MultiPowerSO-30 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10deg
S	0deg		7deg

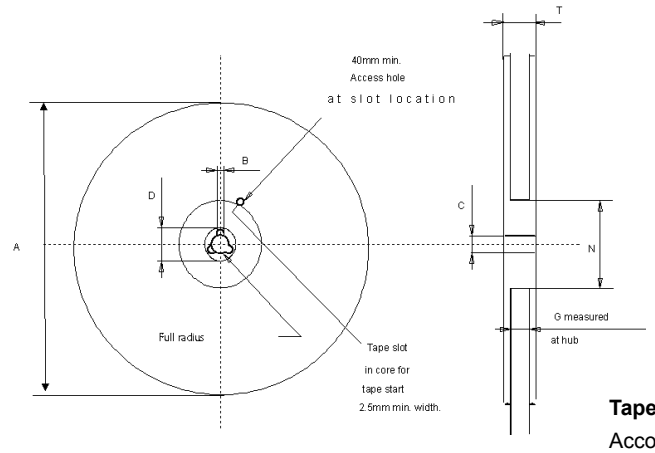
Figure 45. MultiPowerSO-30 suggested pad layout



5.2 Packing information

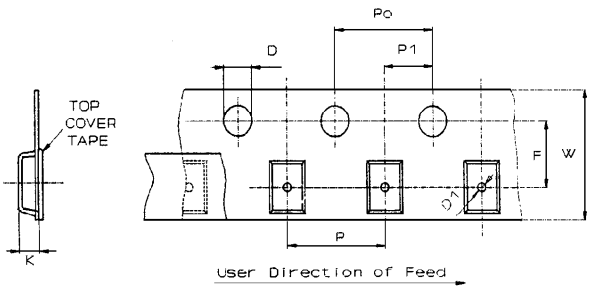
Note: The devices are packed in tape and reel shipments (see Table 1: Device summary on page 1).

Figure 46. MultiPowerSO-30 tape and reel shipment (suffix “TR”)



Reel dimensions

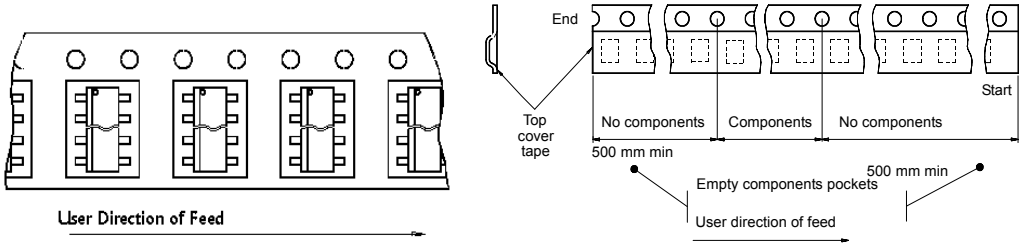
Dimension	mm
A (max)	330
B (min)	1.5
C (± 0.2)	13
D (min)	20.2
G (+ 2 / -0)	32
N (min)	100
T (max)	38.4



Tape dimensions

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Description	Dimension	mm
Tape width	W	32
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	24
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	2
Hole Position	F (± 0.1)	14.2
Compartment Depth	K (max)	2.2
Hole Spacing	P1 (± 0.1)	2



6 Revision history

Table 19. Document revision history

Date	Revision	Changes
Aug-2004	1	Initial release of lead-free version based on the VNH3SP30 datasheet (May 2004 - Rev.1)
Aug- 2005	2	Modified figure 5
20-Dec-2006	3	Document converted into new ST corporate template. Changed document title . Changed features on page 1 to add ECOPACK® package. Added section 1: device block description on page 5. Added section 2: pinout description on page 6. Added section 3: maximum ratings on page 8. Added section 4: electrical characteristics on page 9. Added “low” and “high” to parameters for I_{INL} and I_{INH} in Table 6 on page 9. Added section 5: Waveforms and truth table on page 12. Changed first of two fault conditions in section 5 on page 12. Inserted note in Figure 4 on page 12. Added vertical limitation line to left side arrow of $t_{D(off)}$ to Figure 7 on page 17. Added section 6: thermal data on page 26. Added section 7: package characteristics on page 30. Added section 8: packaging information on page 32. Updated disclaimer (last page) to include a mention about the use of ST products in automotive applications.
20-Jun-2007	4	Document reformatted. Changed *Table 6: Power section on page 9* : supply current and static resistance values. Added *Table 7: Logic inputs (INA, INB, ENA, ENB) on page 9* : V_{DIAG} ROW · Deleted Enable (Logic I/O pin) Table.
13-Sep-2007	5	Updated *Table 2: Block description on page 5*.
15-Nov-2007	6	Corrected *Figure 34* note : changed On resistance per leg from 9.5 mΩ to 22.5 mΩ .
06-Feb-2008	7	Corrected Heat Slug numbers in *Table 3: Pin definitions and functions*.
24-Sep-2013	8	Updated disclaimer.
17-Jan-2017	9	– Removed all information relative to tube packing of the product – Modified *Section 5: Package information.* – Added AEC-Q100 qualified in the Features section – Minor text edits throughout the document

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