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MOSFET - Power, Single N-Channel

40 V, 1.1 mΩ, 277 A



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NVMTS1D1N04C

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- New Power 88 Package
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|--|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 40 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 277 | A |
| | | $T_C = 100^\circ\text{C}$ | 196 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | Steady State | $T_C = 25^\circ\text{C}$ | P_D 153 | W |
| | | $T_C = 100^\circ\text{C}$ | 76.5 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 48.8 | A |
| | | $T_A = 100^\circ\text{C}$ | 34.5 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 4.7 | W |
| | | $T_A = 100^\circ\text{C}$ | 2.4 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 900 | A | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 128 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 22 \text{ A}$) | E_{AS} | 721 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

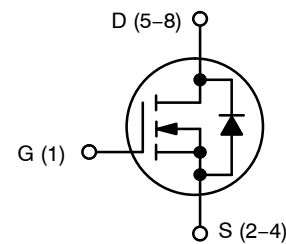
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

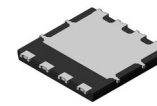
| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case - Steady State | $R_{\theta JC}$ | 0.98 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient - Steady State (Note 2) | $R_{\theta JA}$ | 31.6 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 40 V | 1.1 mΩ @ 10 V | 277 A |

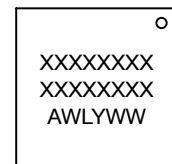


N-CHANNEL MOSFET



DFNW8
CASE 507AP

MARKING DIAGRAM



XXXX = Specific Device Code
 A = Assembly Location
 WL = Wafer Lot Code
 Y = Year Code
 WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 2 of this data sheet.

NVMTS1D1N04C

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|-------------------|---|---------------------------|-----|-----------|---------------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 40 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | 21 | | mV/°C |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$ | $T_J = 25^\circ\text{C}$ | | 10 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 250 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|-----------------------------------|------------------|---|-----|------|-----|------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 210\ \mu\text{A}$ | 2.0 | 2.8 | 4.0 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | -7.4 | | mV/°C |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ | | 0.87 | 1.1 | m Ω |
| Forward Transconductance | g_{FS} | $V_{DS} = 5\text{ V}, I_D = 50\text{ A}$ | | 136 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|------------------------------|--------------|---|--|------|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$ | | 5410 | | pF |
| Output Capacitance | C_{OSS} | | | 3145 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 82 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}; I_D = 50\text{ A}$ | | 86 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 10 | | |
| Gate-to-Source Charge | Q_{GS} | | | 24 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 24 | | |
| Plateau Voltage | V_{GP} | | | 4.8 | | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|--------------|--|--|----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 20\text{ V}, I_D = 50\text{ A}, R_G = 6\ \Omega$ | | 23 | | ns |
| Rise Time | t_r | | | 27 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 60 | | |
| Fall Time | t_f | | | 32 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|--|---------------------------|-----|------|-----|---|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V}, I_S = 50\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.79 | 1.2 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.65 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$ | | 81 | | ns | |
| Charge Time | t_a | | | 43 | | | |
| Discharge Time | t_b | | | 38 | | | |
| Reverse Recovery Charge | Q_{RR} | | | 100 | | nC | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|-----------------|---------|--------------------|--------------------|
| NVMTS1D1N04CTXG | 1D1N04C | POWER 88 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

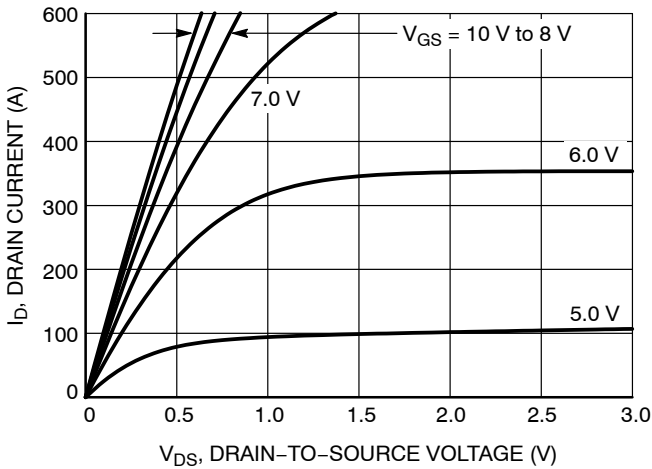


Figure 1. On-Region Characteristics

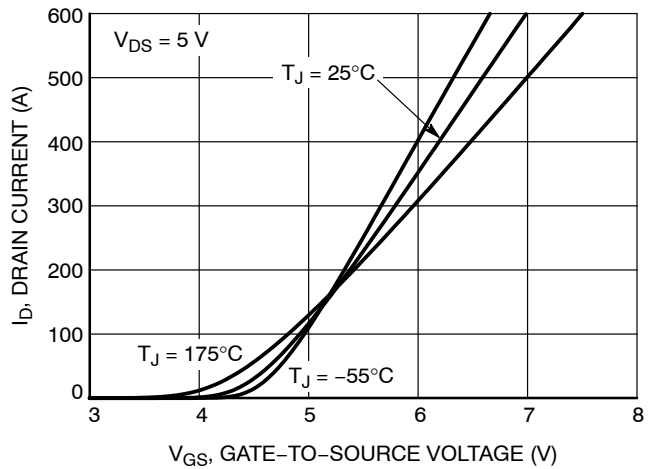


Figure 2. Transfer Characteristics

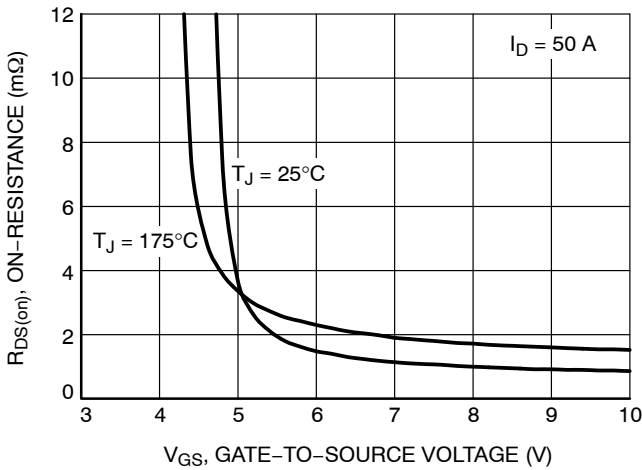


Figure 3. On-Resistance vs. Gate-to-Source Voltage

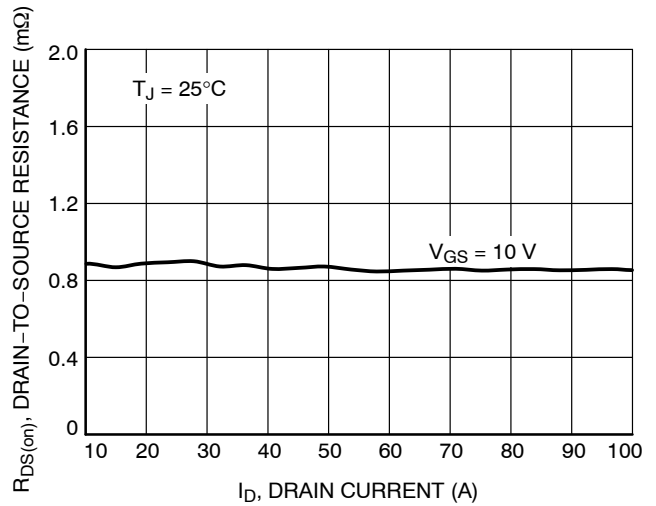


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

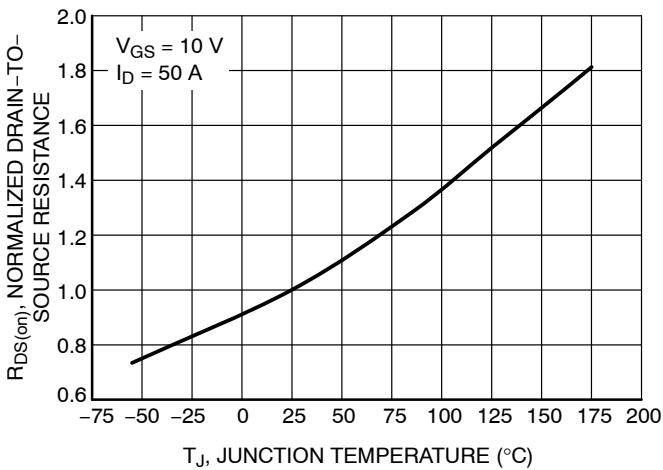


Figure 5. On-Resistance Variation with Temperature

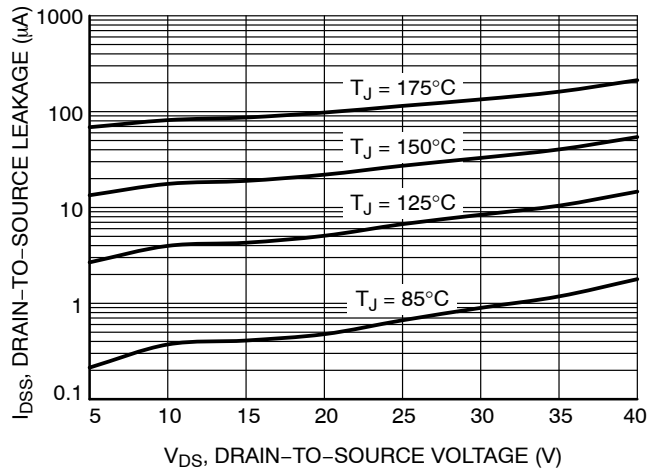


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

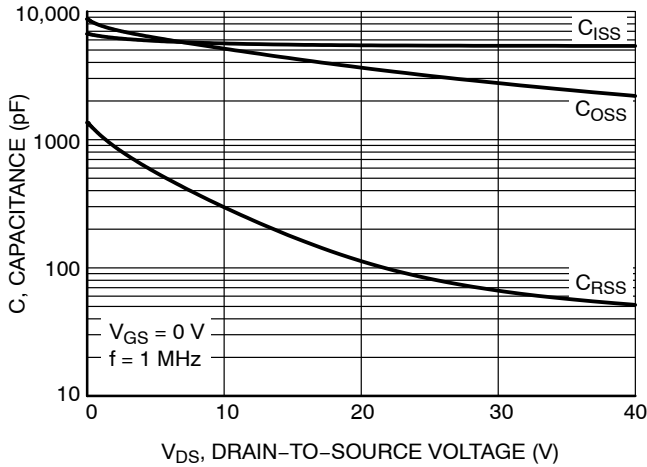


Figure 7. Capacitance Variation

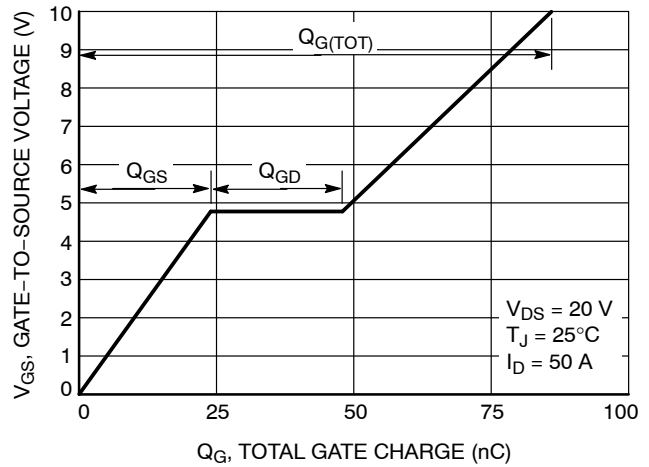


Figure 8. Gate-to-Source Voltage vs. Total Charge

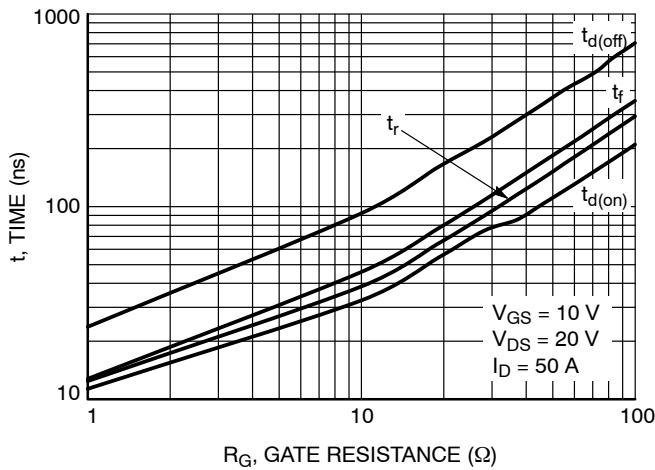


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

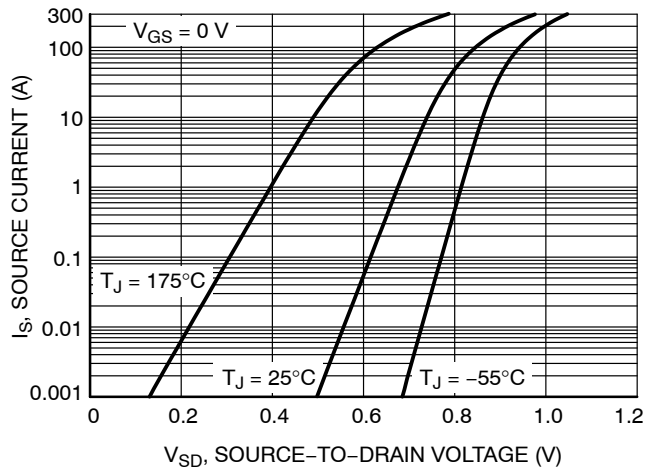


Figure 10. Diode Forward Voltage vs. Current

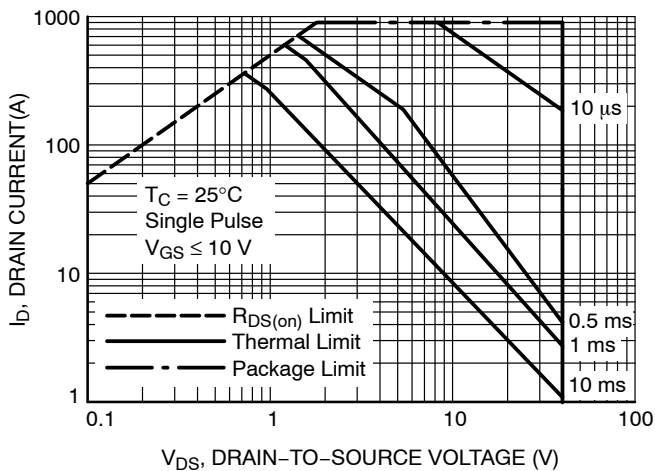


Figure 11. Maximum Rated Forward Biased Safe Operating Area

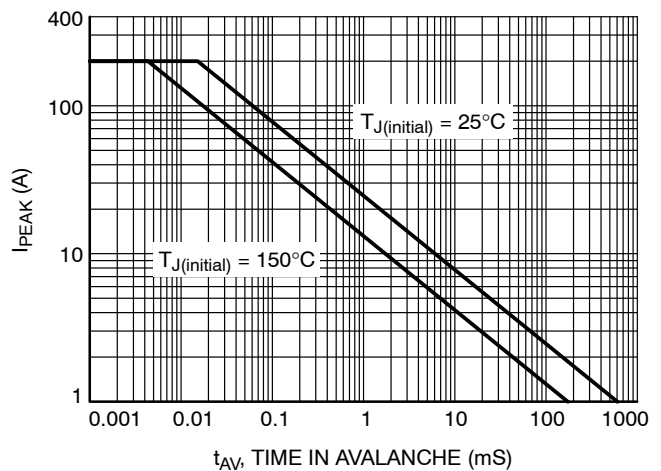


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

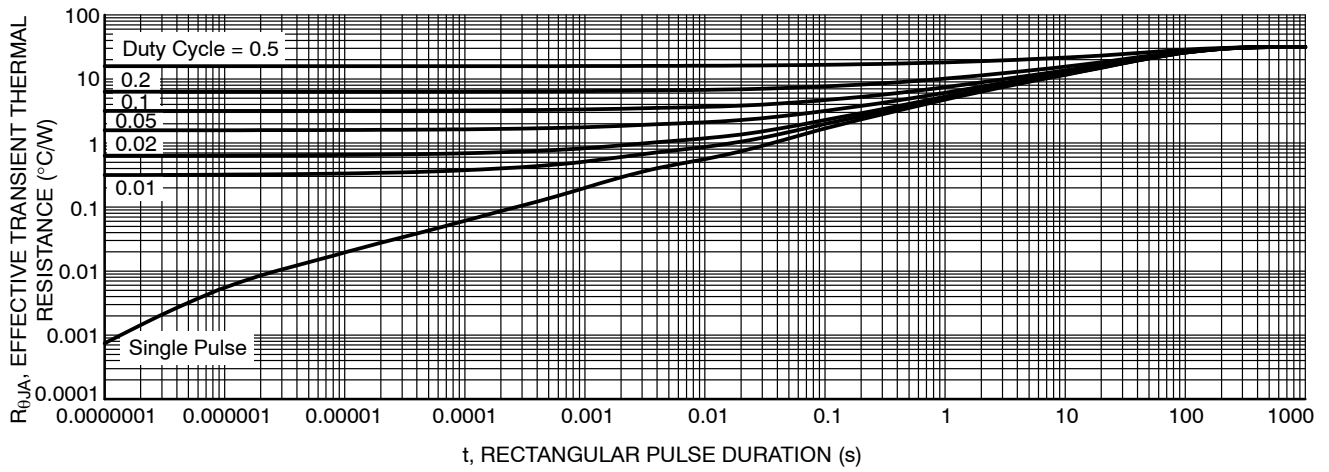
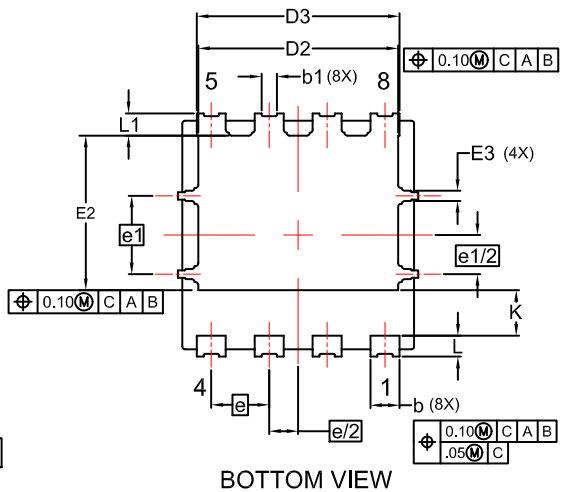
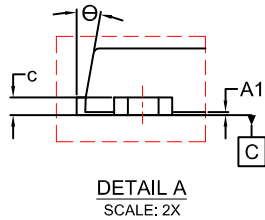
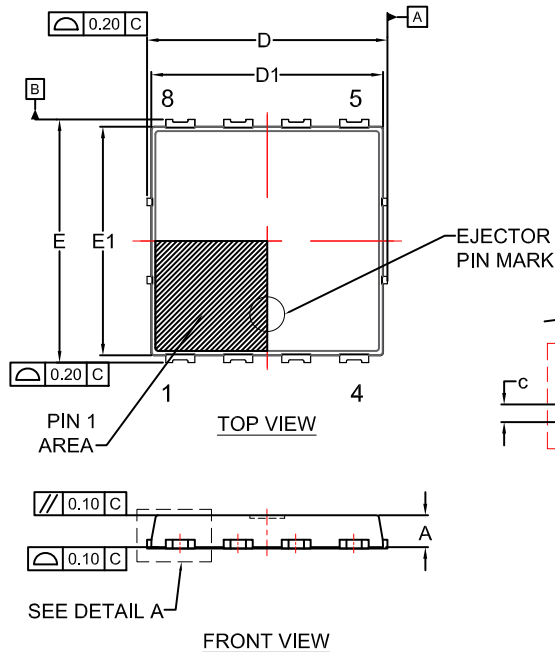


Figure 13. Thermal Characteristics

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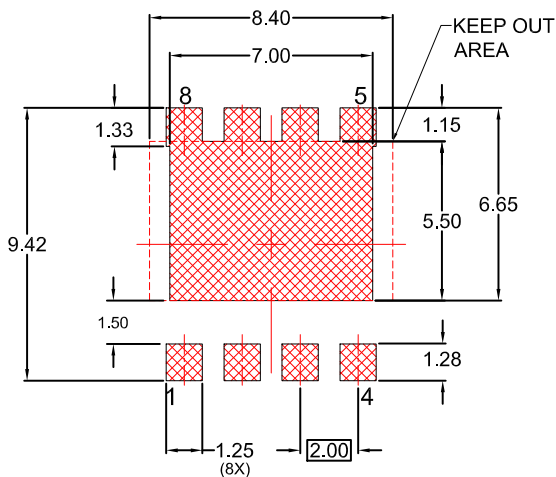
PACKAGE DIMENSIONS

DFNW8 8.3x8.4, 2P
CASE 507AP
ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

| DIM | MILLIMETERS | | |
|------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 1.00 | 1.10 | 1.20 |
| A1 | 0.00 | -- | 0.05 |
| b | 0.90 | 1.00 | 1.10 |
| b1 | 0.43 | 0.53 | 0.63 |
| c | 0.23 | 0.28 | 0.33 |
| D | 8.20 | 8.30 | 8.40 |
| D1 | 7.90 | 8.00 | 8.10 |
| D2 | 6.80 | 6.90 | 7.00 |
| D3 | 6.90 | 7.00 | 7.10 |
| E | 8.30 | 8.40 | 8.50 |
| E1 | 7.80 | 7.90 | 8.00 |
| E2 | 5.24 | 5.34 | 5.44 |
| E3 | 0.25 | 0.35 | 0.45 |
| e | 2.00 BSC | | |
| e/2 | 1.00 BSC | | |
| e1 | 2.70 BSC | | |
| e1/2 | 1.35 BSC | | |
| K | 1.50 | 1.57 | 1.70 |
| L | 0.64 | 0.74 | 0.84 |
| L1 | 0.67 | 0.77 | 0.87 |
| θ | 0° | -- | 12° |

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