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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

100A, 55V, 0.008 Ohm, N-Channel, Power MOSFETs

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

NOTE: Calculated continuous current based on maximum allowable junction temperature. Package limited to 75A continuous, see Figure 9.

Ordering Information

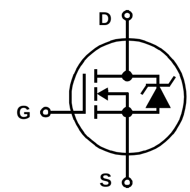
PART NUMBER	PACKAGE	BRAND
HRF3205	TO-220AB	HRF3205
HRF3205S	TO-263AB	HRF3205S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HRF3205ST.

Features

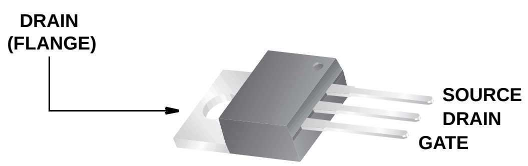
- 100A, 55V (See Note)
- Low On-Resistance, $r_{DS(ON)} = 0.008\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- UIS Rating Curve
- Related Literature
  - TB334, “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol

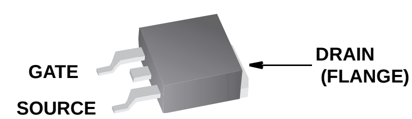


Packaging

JEDEC TO-220AB



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Othewise Specified

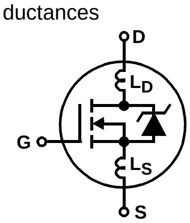
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	55	V
Gate to Source Voltage	V_{GS}	±20V	V
Drain Current			
Continuous	I_D	100	A
Pulsed Drain Current (Note 2)	I_{DM}	390	A
Pulsed Avalanche Rating	E_{AS}	Figure 10	
Power Dissipation	P_D	175	W
Derate Above 25^oC		1.17	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

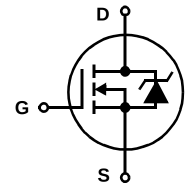
NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$	55	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 55V$, $V_{GS} = 0V$	-	-	25	μA
		$V_{DS} = 44V$, $V_{GS} = 0V$, $T_C = 150^oC$	-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	-	-	100	nA
Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25^oC, $I_D = 250\mu A$	-	0.057	-	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 59A$, $V_{GS} = 10V$ (Figure 4)	-	0.0065	0.008	Ω
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 28V$, $I_D \cong 59A$, $R_L = 0.47\Omega$, $V_{GS} = 10V$, $R_{GS} = 2.5\Omega$	-	14	-	ns
Rise Time	t_r		-	100	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	43	-	ns
Fall Time	t_f		-	70	-	ns
Total Gate Charge	Q_g	$V_{DD} = 44V$, $I_D \cong 59A$, $V_{GS} = 10V$, $I_{g(REF)} = 3mA$ (Figure 6)	-	-	170	nC
Gate to Source Charge	Q_{gs}		-	-	32	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	-	74	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 5)	-	4000	-	pF
Output Capacitance	C_{OSS}		-	1300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	480	-	pF
Internal Source Inductance	L_S	Measured From the Contact Screw on Tab to Center of Die Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	7.5	-	nH
Internal Drain Inductance	L_D	Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad	-	4.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.85	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220	-	-	62	$^oC/W$
		TO-263 (PCB Mount, Steady State)	-	-	40	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	MOSFET Symbol Showing The Integral Reverse P-N Junction Diode 	-	-	100 (Note 1	A
Pulsed Source to Drain Current (Note 2)	I_{SDM}		-	-	390	A
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 59A (Note 4)	-	-	1.3	V
Reverse Recovery Time	t_{rr}	I_{SD} = 59A, dI_{SD}/dt = 100A/µs (Note 4)	-	110	170	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 59A, dI_{SD}/dt = 100A/µs (Note 4)	-	450	680	nC

NOTE:

2. Repetitive rating; pulse width limited by maximum junction temperature (See Figure 11)

Typical Performance Curves

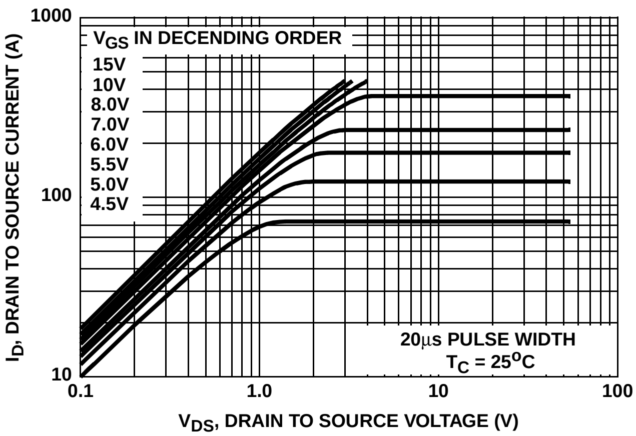


FIGURE 1. OUTPUT CHARACTERISTICS

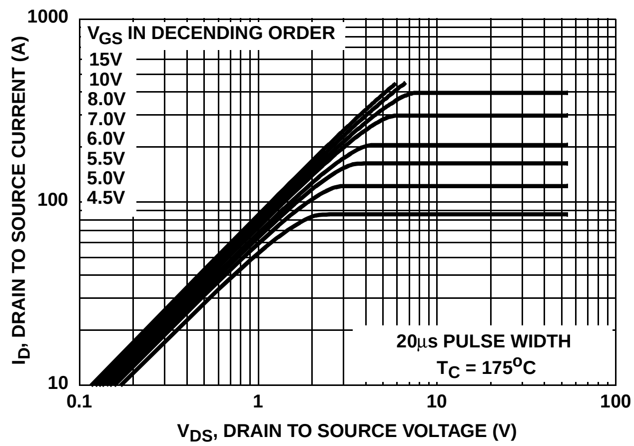


FIGURE 2. OUTPUT CHARACTERISTICS

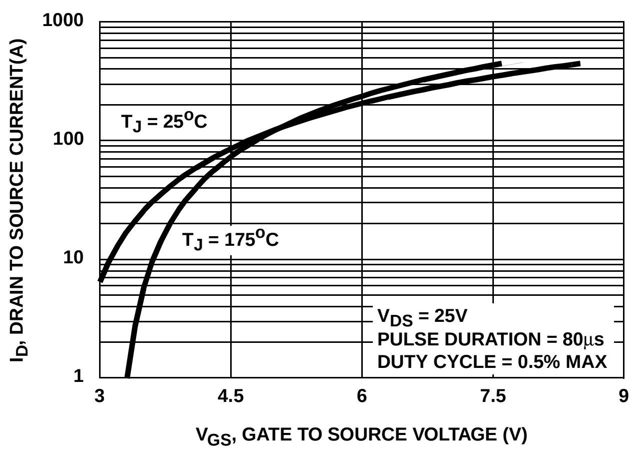


FIGURE 3. TRANSFER CHARACTERISTICS

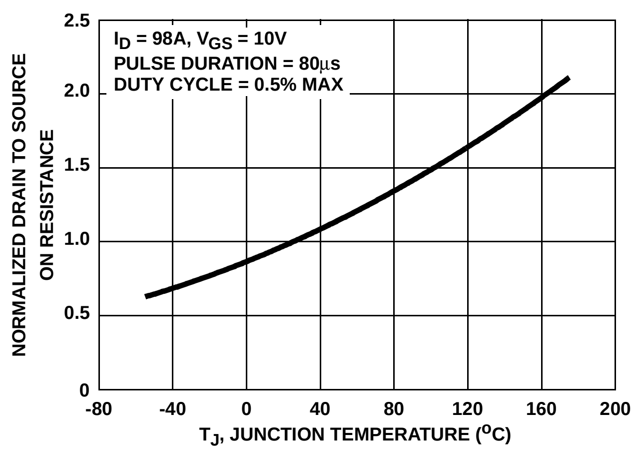


FIGURE 4. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

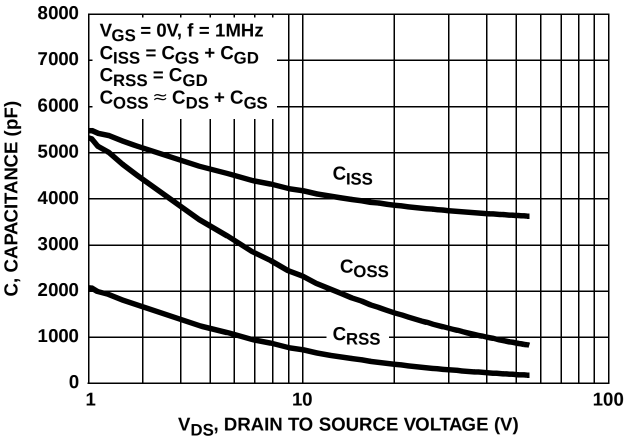


FIGURE 5. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

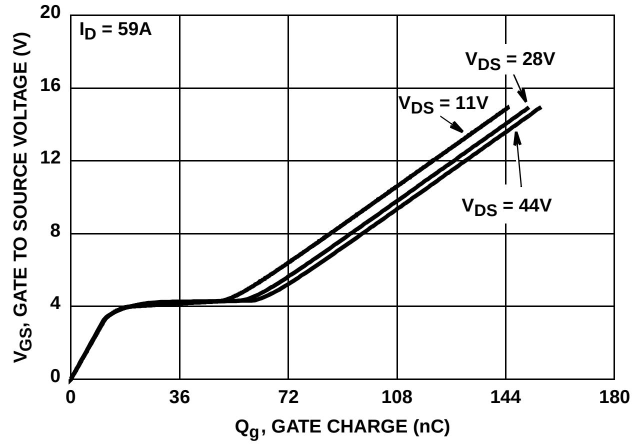


FIGURE 6. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

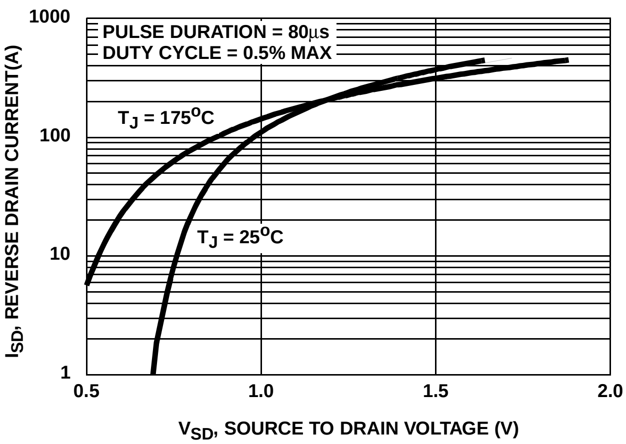


FIGURE 7. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

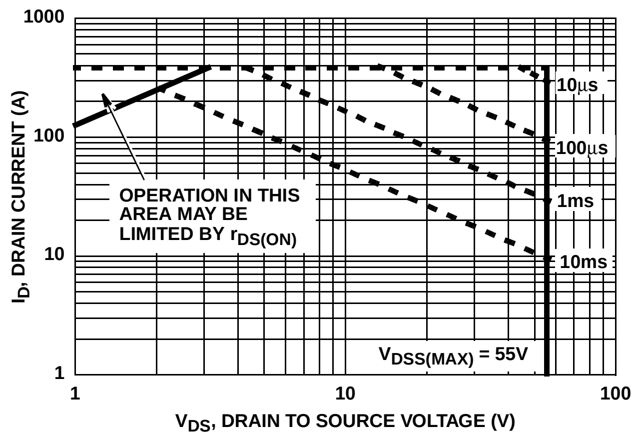


FIGURE 8. FORWARD BIAS SAFE OPERATING AREA

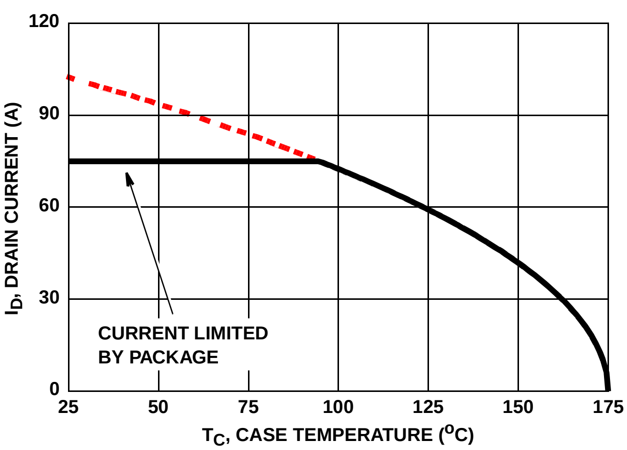


FIGURE 9. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

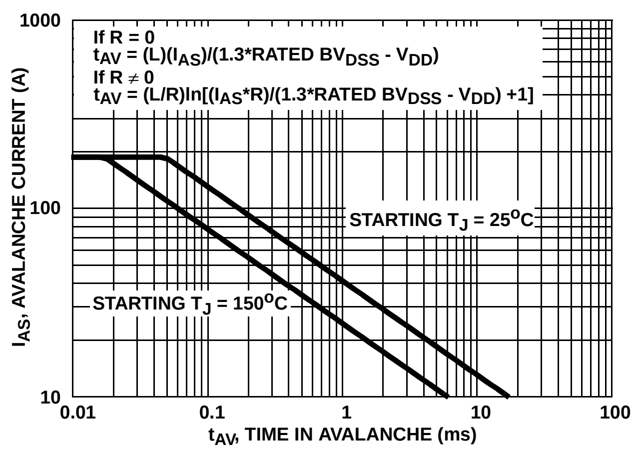


FIGURE 10. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

Typical Performance Curves (Continued)

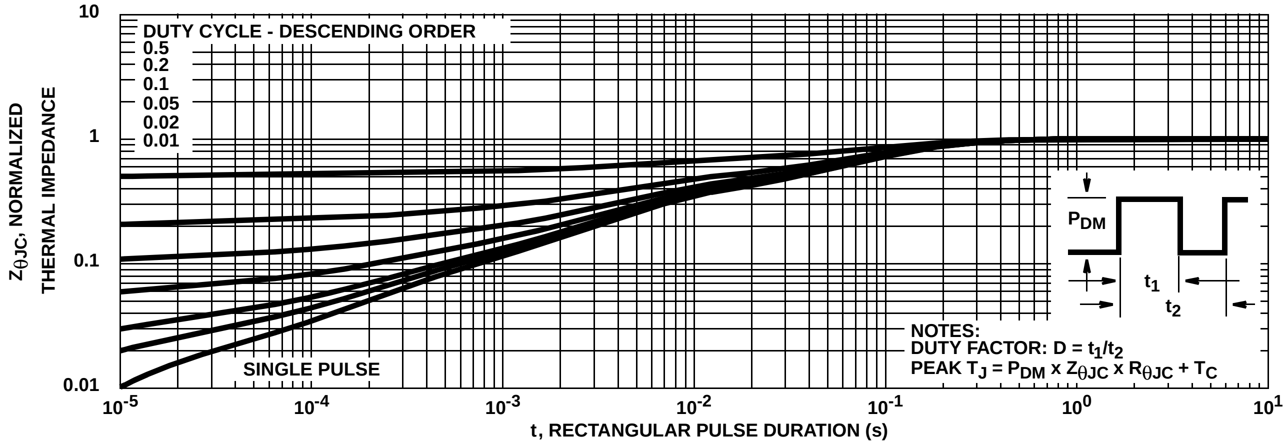


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Test Circuits and Waveforms

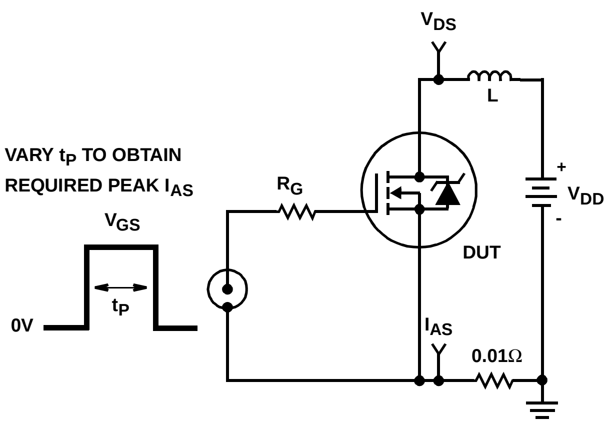


FIGURE 12. UNCLAMPED ENERGY TEST CIRCUIT

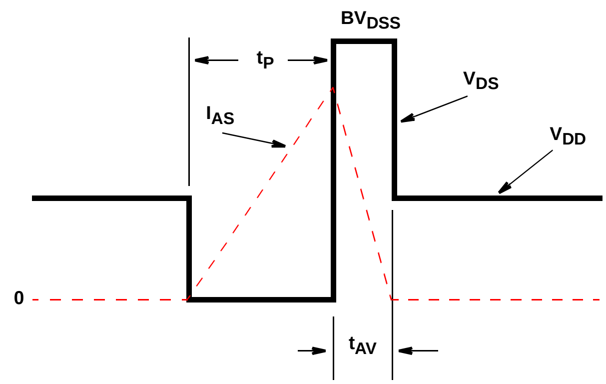


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

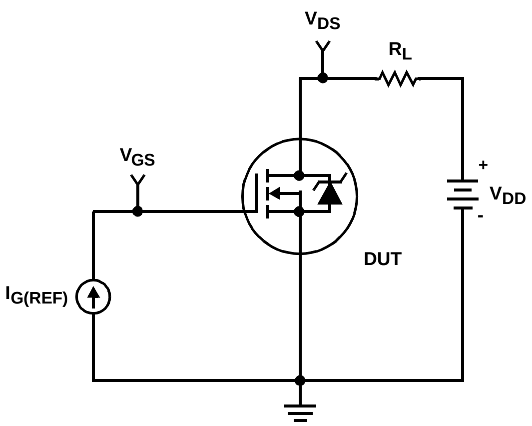


FIGURE 14. GATE CHARGE TEST CIRCUIT

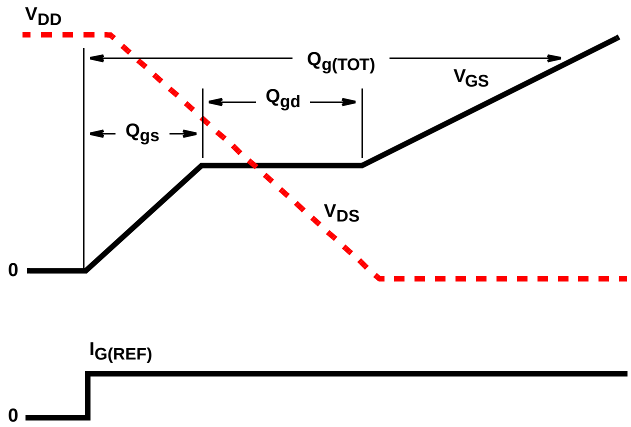


FIGURE 15. GATE CHARGE WAVEFORM

Test Circuits and Waveforms (Continued)

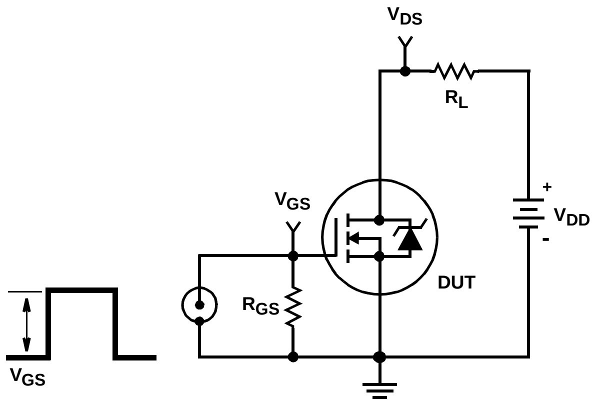


FIGURE 16. SWITCHING TIME TEST CIRCUIT

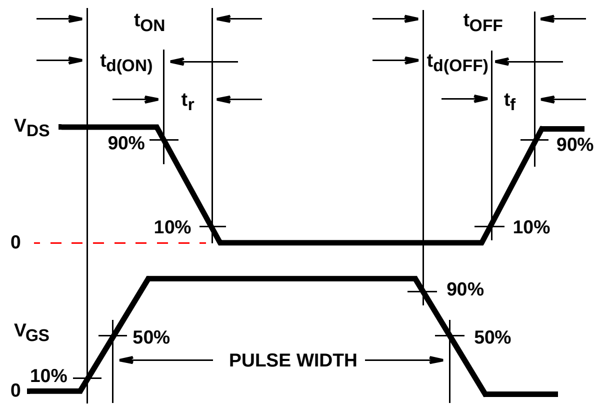
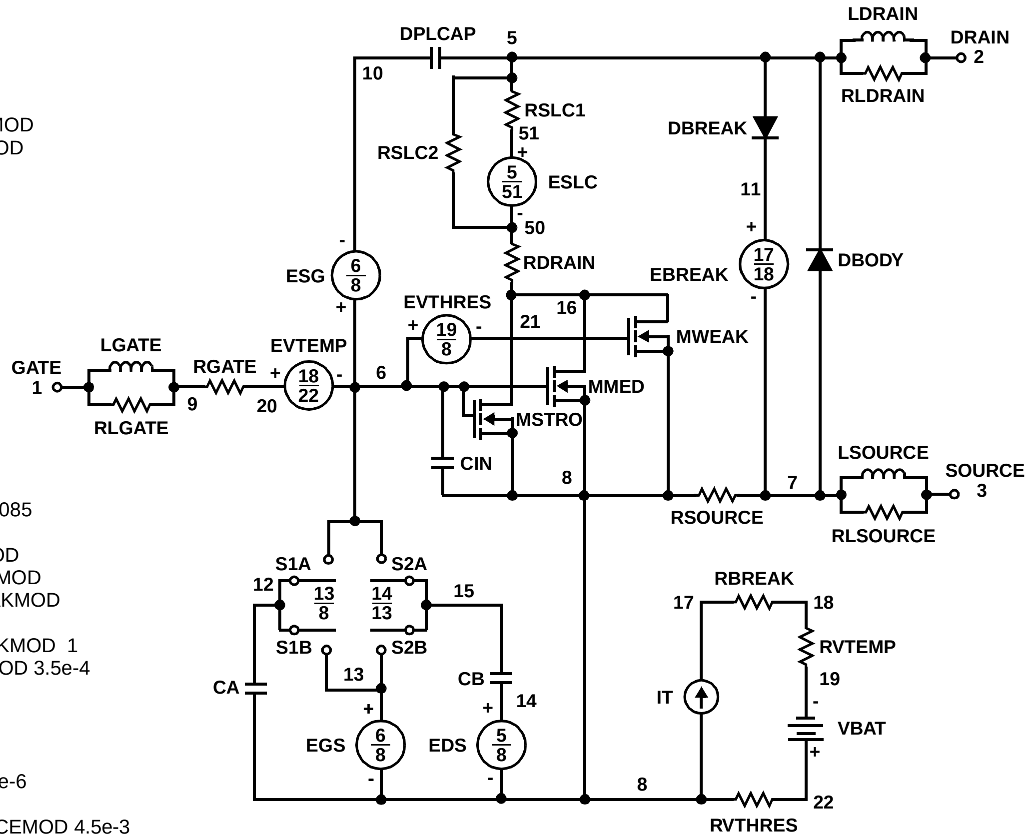


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

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SUBCKT HRF3205P3 2 1 3 ;     rev 7/25/97

CA  12 8 4.9e-9
CB  15  14 4.9e-9
CIN  6  8 3.45e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 57
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1e-9
LGATE 1  9 2.6e-9
LSOURCE  3  7 1.1e-9
K1 LGATE LSOURCE 0.0085

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 3.5e-4
RGATE  9  20 0.36
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 4.5e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*550),3))}

.MODEL DBODYMOD D (IS = 4.25e-12  RS = 1.8e-3  TRS1 = 2.75e-3  TRS2 = 5e-6  CJO = 5.95e-9  TT = 4e-7 M = 0.55)
.MODEL DBREAKMOD D (RS = 0.0  6IKF = 30 TRS1 = -3e-  3TRS2 = 3e-6)
.MODEL DPLCAPMOD D (CJO = 4.45e-  9IS = 1e-3  0N = 1 M = 0.88 VJ = 1.45)
.MODEL MMEDMOD NMOS (VTO = 2.93 KP = 9.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1)
.MODEL MSTROMOD NMOS (VTO = 3.23 KP = 150 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.35 KP = 0.02 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 10)
.MODEL RBREAKMOD RES (TC1 = 8e-  4TC2 = 4e-6)
.MODEL RDRAINMOD RES (TC1 = 8e-2  TC2 = 5e-6)
.MODEL RSLCMOD RES (TC1 = 1e-4 TC2 = 1.05e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-4 TC2 = 1.5e-5)
.MODEL RVTHRESMOD RES (TC1 = -2.3e-3 TC2 = -1.2e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.2e-  3TC2 = -7e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -9  VOFF= -4)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4  VOFF= -9)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0  VOFF= 2.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 2.5  VOFF= 0)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

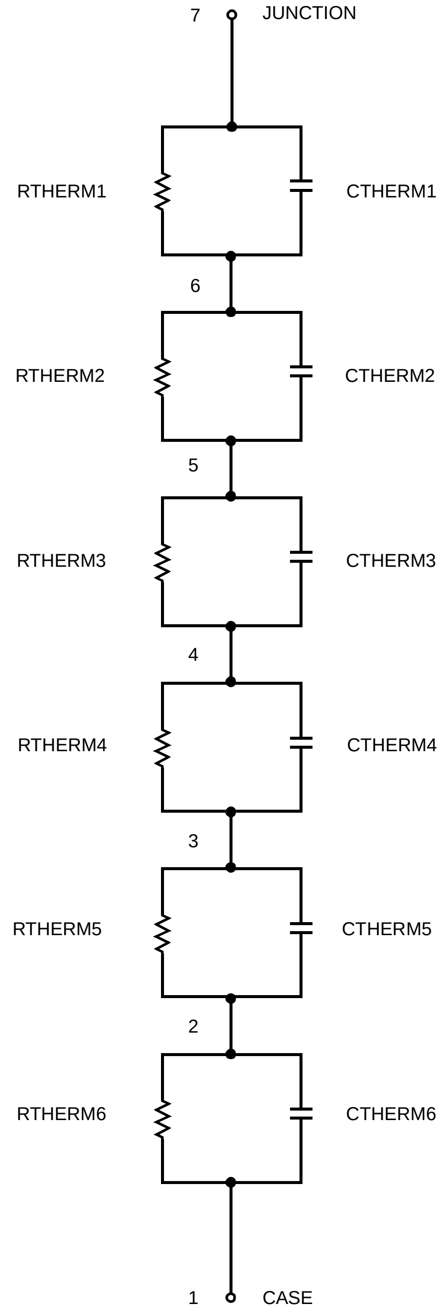
SPICE Thermal Model

REV 25 July 97

HRF3205

CTHERM1 7 6 2.53e-5
CTHERM2 6 5 1.38e-3
CTHERM3 5 4 7.00e-3
CTHERM4 4 3 2.50e-2
CTHERM5 3 2 1.33e-1
CTHERM6 2 1 5.75e-1

RTHERM1 7 6 7.78e-4
RTHERM2 6 5 8.55e-3
RTHERM3 5 4 3.00e-2
RTHERM4 4 3 1.42e-1
RTHERM5 3 2 2.65e-1
RTHERM6 2 1 2.33e-1



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Rev. H4

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