

## Single channel high side driver with analog current sense for automotive applications

Datasheet – production data

### Features

Max supply voltage	$V_{CC}$	41 V
Operating voltage range	$V_{CC}$	4.5 to 36 V
Max on-state resistance (per ch.)	$R_{ON}$	12 m $\Omega$
Current limitation (typ)	$I_{LIMH}$	65 A
Off-state supply current (typ)	$I_S$	2 $\mu$ A <sup>(1)</sup>

1. Typical value with all loads connected

- General features
  - Inrush current active management by power limitation
  - Very low stand-by current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC european directive
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Current sense disable
  - Thermal shutdown indication
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of  $V_{CC}$
  - Thermal shutdown



- Reverse battery protection
- Electrostatic discharge protection

### Application

- All types of resistive, inductive and capacitive loads

### Description

The VN5012AK-E is a monolithic device made using STMicroelectronics VIPower<sup>®</sup> M0-5 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active  $V_{CC}$  pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS\_DIS is driven low or left open. When CS\_DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shutdown intervention. Thermal shutdown with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape and reel
PowerSSO-24	VN5012AK-E	VN5012AKTR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

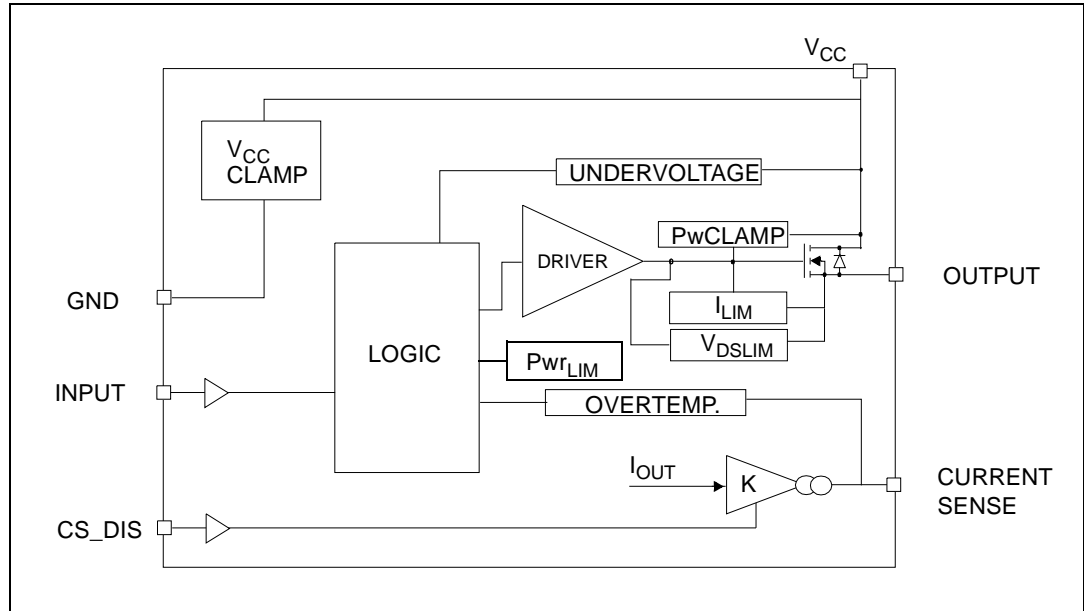


Table 2. Pin function

Name	Function
V <sub>CC</sub>	Battery connection.
OUTPUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE <sub>1,2</sub>	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

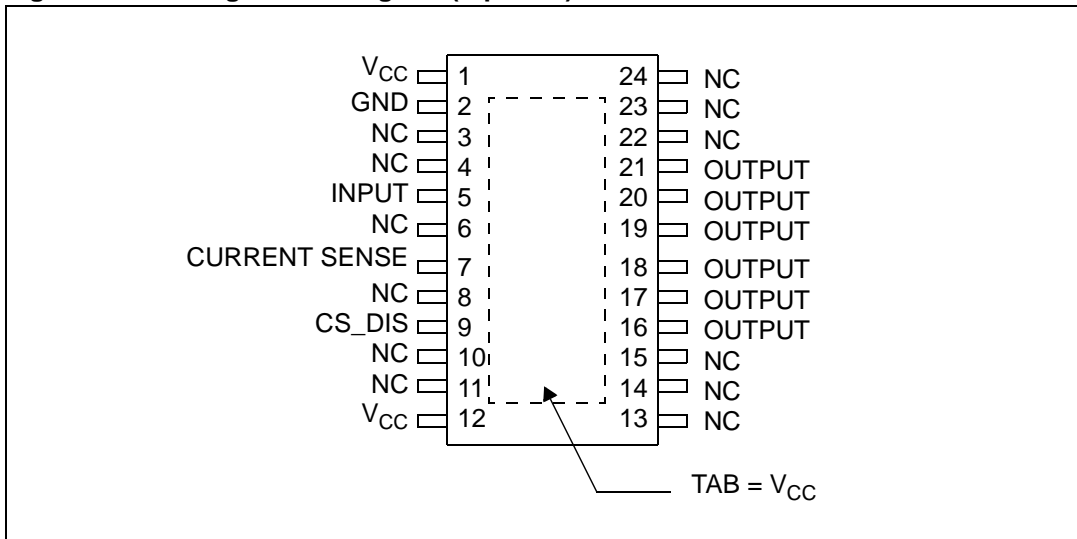


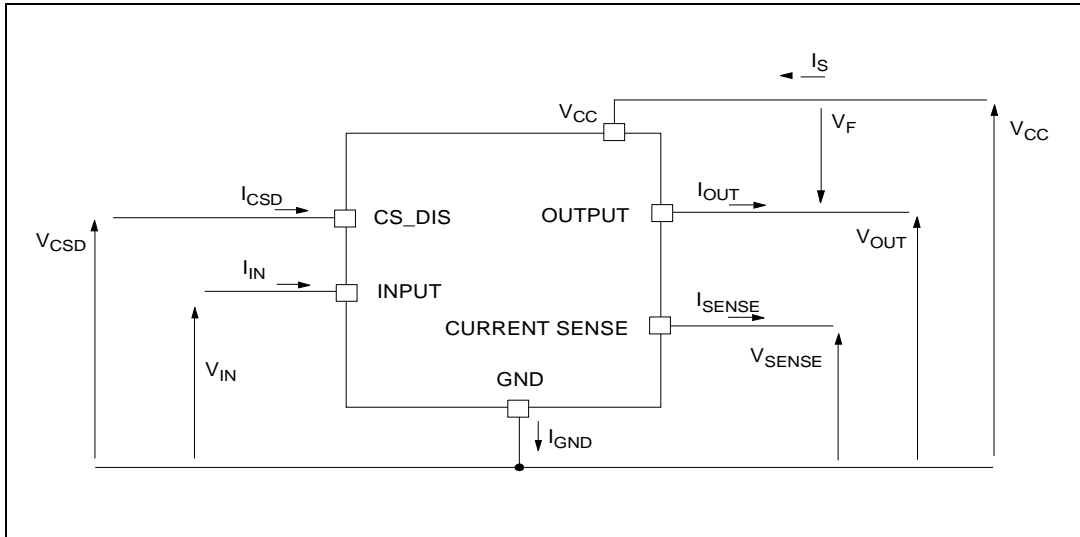
Table 3. Suggested connections for unused and not connected pins

Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. <sup>(1)</sup>	X	X	X	X
To ground	Through 1 KΩ resistor	X	N.R.	Through 10 KΩ resistor	Through 10 KΩ resistor

1. Not recommended.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



Note:  $V_F = V_{OUT} - V_{CC}$  during reverse battery condition.

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC supply voltage	41	V
-V <sub>CC</sub>	Reverse DC supply voltage	0.3	V
-I <sub>GND</sub>	DC reverse ground pin current	200	mA
I <sub>OUT</sub>	DC output current	Internally limited	A
-I <sub>OUT</sub>	Reverse DC output current	-30	A
I <sub>IN</sub>	DC input current	-1 to 10	mA
I <sub>CS_D</sub>	DC current sense disable input current	-1 to 10	mA
-I <sub>CSSENSE</sub>	DC reverse CS pin current	200	mA
V <sub>CSSENSE</sub>	Current sense maximum voltage	V <sub>CC</sub> -41 +V <sub>CC</sub>	V V

**Table 4. Absolute maximum ratings (continued)**

Symbol	Parameter	Value	Unit
$E_{MAX}$	Maximum switching energy ( $L = 1.25$ mH; $R_L = 0$ $\Omega$ ; $V_{bat} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}(typ.)$ )	508	mJ
$V_{ESD}$	Electrostatic discharge (Human Body Model: $R = 1.5$ K $\Omega$ ; $C = 100$ pF)	4000	V
	– INPUT	2000	V
	– CURRENT SENSE	4000	V
	– CS_DIS	2000	V
	– OUTPUT	4000	V
	– $V_{CC}$	5000	V
$V_{ESD}$	Charge device model (CDM-AEC-Q100-011)	750	V
$T_j$	Junction operating temperature	-40 to 150	°C
$T_{stg}$	Storage temperature	-55 to 150	°C

## 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Max value	Unit
$R_{thj-case}$	Thermal resistance junction case (max) (with one channel on)	0.4	°C/W
$R_{thj-amb}$	Thermal resistance junction ambient (max)	See <a href="#">Figure 29</a>	°C/W

## 2.3 Electrical characteristics

$8$  V <  $V_{CC}$  <  $36$  V;  $-40$  °C <  $T_j$  <  $150$  °C, unless otherwise specified.

**Table 6. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC}$	Operating supply voltage		4.5	13	36	V
$V_{USD}$	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
$R_{ON}$	On-state resistance <sup>(2)</sup>	$I_{OUT} = 5$ A; $T_j = 25$ °C			12	m $\Omega$
		$I_{OUT} = 5$ A; $T_j = 150$ °C			24	m $\Omega$
		$I_{OUT} = 5$ A; $V_{CC} = 5$ V; $T_j = 25$ °C			16	m $\Omega$
$V_{clamp}$	Clamp voltage	$I_S = 20$ mA	41	46	52	V



**Table 6. Power section (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S$	Supply current	Off-state; $V_{CC} = 13\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; $V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0\text{ V}$		2 <sup>(1)</sup>	5 <sup>(1)</sup>	$\mu\text{A}$
		On-state; $V_{CC} = 13\text{ V}$ ; $V_{IN} = 5\text{ V}$ ; $I_{OUT} = 0\text{ A}$		1.5	3	$\mu\text{A}$
$I_{L(off)}$	Off-state output current <sup>(2)</sup>	$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$	0	0.01	3	$\mu\text{A}$
		$V_{IN} = V_{OUT} = 0\text{ V}$ ; $V_{CC} = 13\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$	0		5	$\mu\text{A}$
$V_F$	Output - $V_{CC}$ diode voltage <sup>(2)</sup>	$-I_{OUT} = 8\text{ A}$ ; $T_j = 150\text{ }^\circ\text{C}$			0.7	V

1. PowerMOS leakage included.
2. For each channel.

**Table 7. Switching ( $V_{CC} = 13\text{ V}$ ;  $T_j = 25\text{ }^\circ\text{C}$ )**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 2.6\ \Omega$ (see <a href="#">Figure 8</a> )		30		$\mu\text{s}$
$t_{d(off)}$	Turn-off delay time	$R_L = 2.6\ \Omega$ (see <a href="#">Figure 8</a> )		55		$\mu\text{s}$
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 2.6\ \Omega$	See <a href="#">Figure 21</a>			V/ $\mu\text{s}$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 2.6\ \Omega$	See <a href="#">Figure 22</a>			V/ $\mu\text{s}$
$W_{ON}$	Switching energy losses during $t_{won}$	$R_L = 2.6\ \Omega$ (see <a href="#">Figure 8</a> )		1.2		mJ
$W_{OFF}$	Switching energy losses during $t_{woff}$	$R_L = 2.6\ \Omega$ (see <a href="#">Figure 8</a> )		0.7		mJ

**Table 8. Logic input**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	Input low level voltage				0.9	V
$I_{IL}$	Low level input current	$V_{IN} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{IH}$	Input high level voltage		2.1			V
$I_{IH}$	High level input current	$V_{IN} = 2.1\text{ V}$			10	$\mu\text{A}$
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1\text{ mA}$	5.5		7	V
		$I_{IN} = -1\text{ mA}$		-0.7		V
$V_{CSDL}$	CS_DIS low level voltage				0.9	V
$I_{CSDL}$	Low level CS_DIS current	$V_{CSD} = 0.9\text{ V}$	1			$\mu\text{A}$
$V_{CSDH}$	CS_DIS high level voltage		2.1			V
$I_{CSDH}$	High level CS_DIS current	$V_{CSD} = 2.1\text{ V}$			10	$\mu\text{A}$

**Table 8. Logic input (continued)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
$V_{CSCL}$	CS_DIS clamp voltage	$I_{CSD} = 1 \text{ mA}$	5.5		7	V
		$I_{CSD} = -1 \text{ mA}$		-0.7		V

**Table 9. Protections and diagnostics (1)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{limH}$	DC Short circuit current	$V_{CC} = 13 \text{ V}$	45	65	90	A
		$5 \text{ V} < V_{CC} < 36 \text{ V}$			90	A
$I_{limL}$	Short circuit current during thermal cycling	$V_{CC} = 13 \text{ V};$ $T_R < T_j < T_{TSD}$		24		A
$T_{TSD}$	Shutdown temperature		150	175	200	°C
$T_R$	Reset temperature		$T_{RS} + 1$	$T_{RS} + 5$		°C
$T_{RS}$	Thermal reset of STATUS		135			°C
$T_{HYST}$	Thermal hysteresis ( $T_{TSD} - T_R$ )			7		°C
$V_{DEMAG}$	Turn-off output voltage clamp	$I_{OUT} = 2 \text{ A}; V_{IN} = 0 \text{ V};$ $L = 6 \text{ mH}$	$V_{CC} - 41$	$V_{CC} - 46$	$V_{CC} - 52$	V
$V_{ON}$	Output voltage drop limitation	$I_{OUT} = 0.5 \text{ A};$ $T_j = -40 \text{ °C to } 150 \text{ °C}$ (see <a href="#">Figure 9</a> )		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

**Table 10. Current sense (8 V < V<sub>CC</sub> < 16 V)**

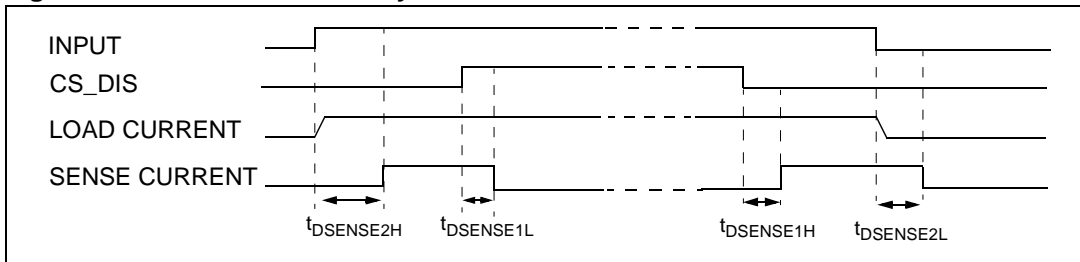
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$K_0$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 0.25 \text{ A}; V_{SENSE} = 0.5 \text{ V};$ $V_{CSD} = 0 \text{ V}; T_j = -40 \text{ °C to } 150 \text{ °C}$	3090	5080	7070	
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 5 \text{ A}; V_{SENSE} = 0.5 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40 \text{ °C to } 150 \text{ °C}$	3590	4480	5370	
		$I_{OUT} = 5 \text{ A}; V_{SENSE} = 0.5 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = 25 \text{ °C to } 150 \text{ °C}$	3790	4480	5170	
$dK_1/K_1^{(1)}$	Current sense ratio drift	$I_{OUT} = 5 \text{ A}; V_{SENSE} = 0.5 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40 \text{ °C to } 150 \text{ °C}$	-8		+8	%
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 10 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40 \text{ °C to } 150 \text{ °C}$	4080	4510	4980	
		$I_{OUT} = 10 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = 25 \text{ °C to } 150 \text{ °C}$	4160	4510	4860	
$dK_2/K_2^{(1)}$	Current sense ratio drift	$I_{OUT} = 10 \text{ A}; V_{SENSE} = 4 \text{ V}; V_{CSD} = 0 \text{ V};$ $T_j = -40 \text{ °C to } 150 \text{ °C}$	-5		+5	%

Table 10. Current sense (8 V < V<sub>CC</sub> < 16 V) (continued)

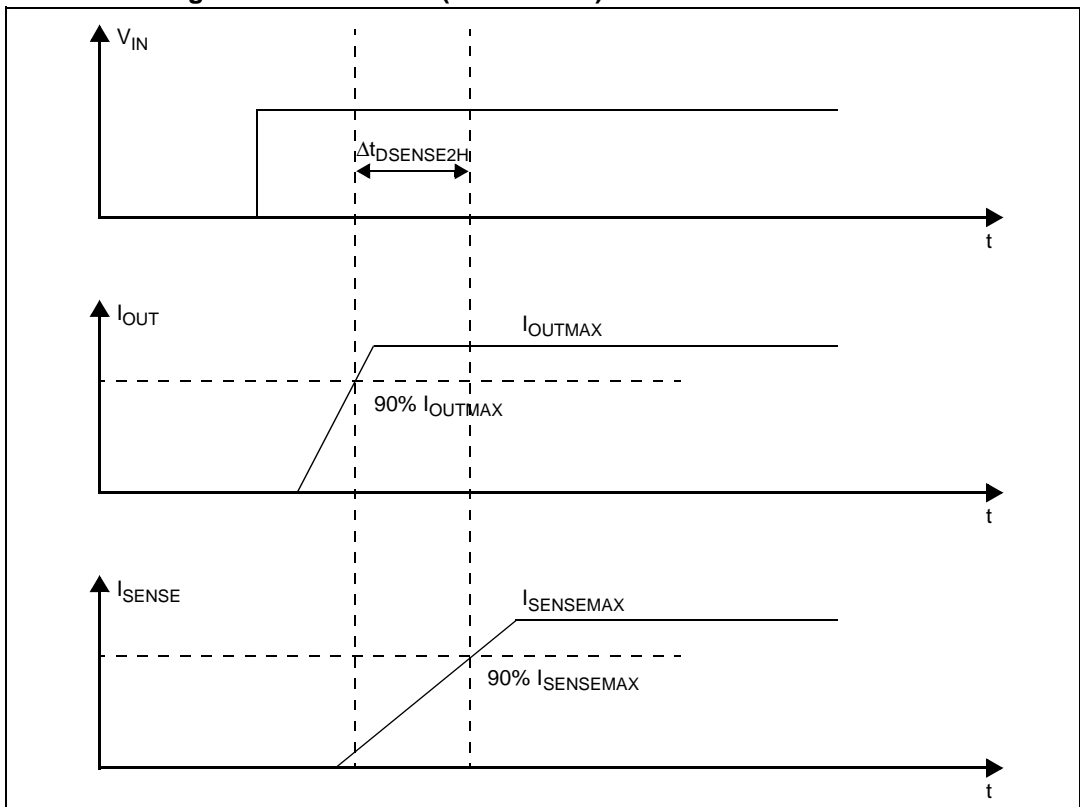
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K <sub>3</sub>	I <sub>OUT</sub> /I <sub>SENSE</sub>	I <sub>OUT</sub> = 25 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> = 0 V; T <sub>j</sub> = -40 °C to 150 °C	4420	4600	4780	
		I <sub>OUT</sub> = 25 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> = 0 V; T <sub>j</sub> = 25 °C to 150 °C	4460	4600	4740	
dK <sub>3</sub> /K <sub>3</sub> <sup>(1)</sup>	Current sense ratio drift	I <sub>OUT</sub> = 25 A; V <sub>SENSE</sub> = 4 V; V <sub>CSD</sub> = 0 V; T <sub>j</sub> = -40 °C to 150 °C	-4		+4	%
I <sub>SENSE0</sub>	Analog sense leakage current	I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 5 V; V <sub>IN</sub> = 0 V; T <sub>j</sub> = -40 °C to 150 °C	0		1	μA
		I <sub>OUT</sub> = 0 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 0 V; V <sub>IN</sub> = 5 V; T <sub>j</sub> = -40 °C to 150 °C	0		2	μA
		I <sub>OUT</sub> = 2 A; V <sub>SENSE</sub> = 0 V; V <sub>CSD</sub> = 5 V; V <sub>IN</sub> = 5 V; T <sub>j</sub> = -40 °C to 150 °C	0		1	μA
I <sub>OL</sub>	Openload on-state current detection threshold	V <sub>IN</sub> = 5 V; I <sub>SENSE</sub> = 5 μA	10		45	mA
V <sub>SENSE</sub>	Max analog sense output voltage	I <sub>OUT</sub> = 15 A; V <sub>CSD</sub> = 0 V	5			V
V <sub>SENSEH</sub>	Analog sense output voltage in over temperature condition	V <sub>CC</sub> = 13 V; R <sub>SENSE</sub> = 2.2 KΩ		9		V
I <sub>SENSEH</sub>	Analog sense output current in over temperature condition	V <sub>CC</sub> = 13 V; V <sub>SENSE</sub> = 5 V		8		mA
t <sub>DSENSE1H</sub>	Delay response time from falling edge of CS_DIS pin	V <sub>SENSE</sub> < 4 V; 1.5 A < I <sub>OUT</sub> < 25 A; I <sub>SENSE</sub> = 90 % of I <sub>SENSE max</sub> (see Figure 4)		50	100	μs
t <sub>DSENSE1L</sub>	Delay response time from rising edge of CS_DIS pin	V <sub>SENSE</sub> < 4 V; 1.5 A < I <sub>OUT</sub> < 25 A; I <sub>SENSE</sub> = 10 % of I <sub>SENSE max</sub> (see Figure 4)		5	20	μs
t <sub>DSENSE2H</sub>	Delay response time from rising edge of INPUT pin	V <sub>SENSE</sub> < 4 V; 1.5 A < I <sub>OUT</sub> < 25 A; I <sub>SENSE</sub> = 90 % of I <sub>SENSE max</sub> (see Figure 4)		270	400	μs
Δt <sub>DSENSE2H</sub>	Delay response time between rising edge of output current and rising edge of current sense	V <sub>SENSE</sub> < 4 V; I <sub>SENSE</sub> = 90 % of I <sub>SENSEMAX</sub> ; I <sub>OUT</sub> = 90 % of I <sub>OUTMAX</sub> ; I <sub>OUTMAX</sub> = 5 A (see Figure 5)			300	μs
t <sub>DSENSE2L</sub>	Delay response time from falling edge of INPUT pin	V <sub>SENSE</sub> < 4 V; 1.5 A < I <sub>OUT</sub> < 25 A; I <sub>SENSE</sub> = 10 % of I <sub>SENSE max</sub> (see Figure 4)		100	250	μs

1. Parameter guaranteed by design, it is not tested.

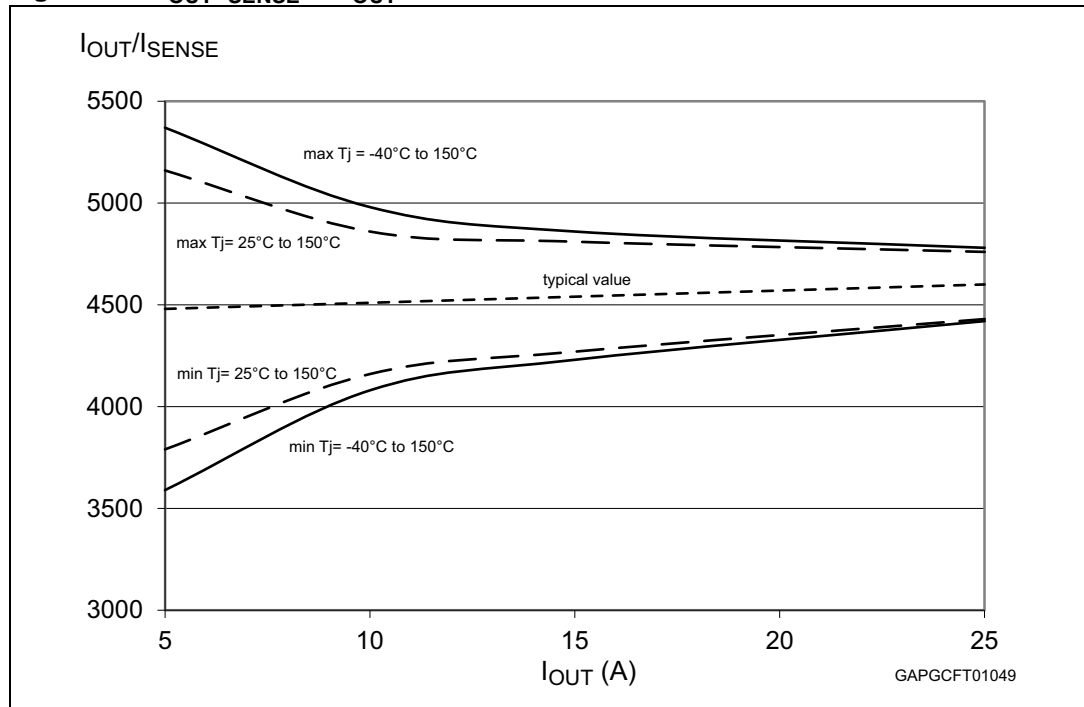
**Figure 4. Current sense delay characteristics**



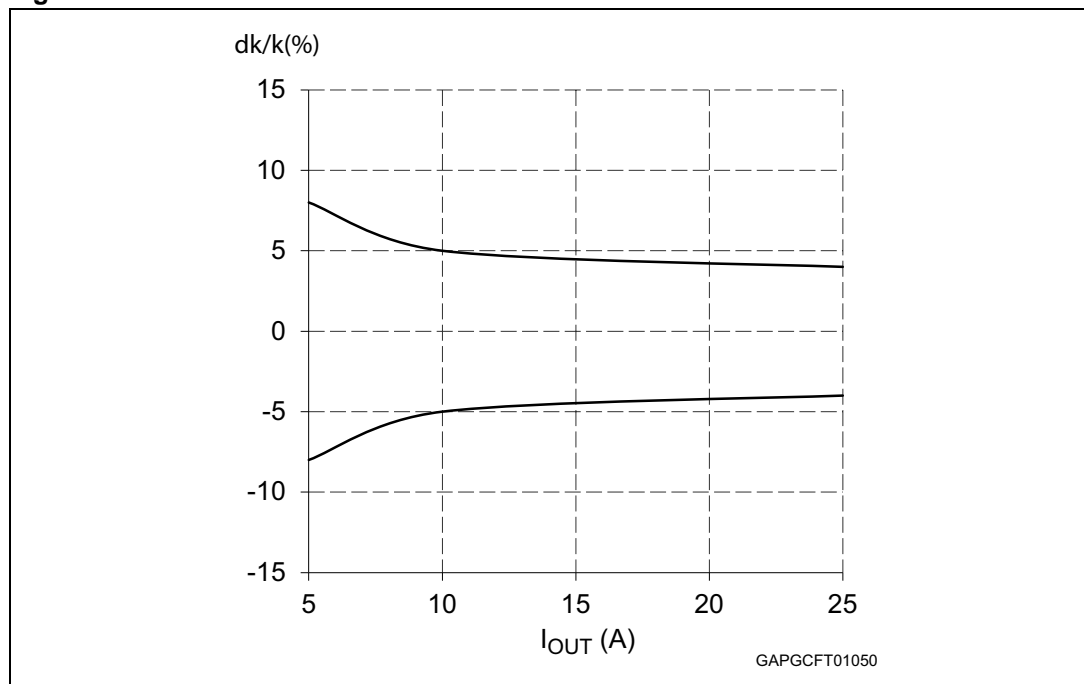
**Figure 5. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)**



**Figure 6.  $I_{OUT}/I_{SENSE}$  vs  $I_{OUT}$**



**Figure 7. Maximum current sense ratio drift vs load current**



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense ( $V_{CSD} = 0\text{ V}$ ) <sup>(1)</sup>
Normal operation	L	L	0
	H	H	Nominal
Over temperature	L	L	0
	H	L	$V_{SENSEH}$
Undervoltage	L	L	0
	H	L	0
Short circuit to GND ( $R_{sc} \leq 10\text{ m}\Omega$ )	L	L	0
	H	L	0 if $T_j < T_{TSD}$ $V_{SENSEH}$ if $T_j > T_{TSD}$
Short circuit to $V_{CC}$	L	H	0
	H	H	< Nominal
Negative output voltage clamp	L	L	0

1. If the  $V_{CSD}$  is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

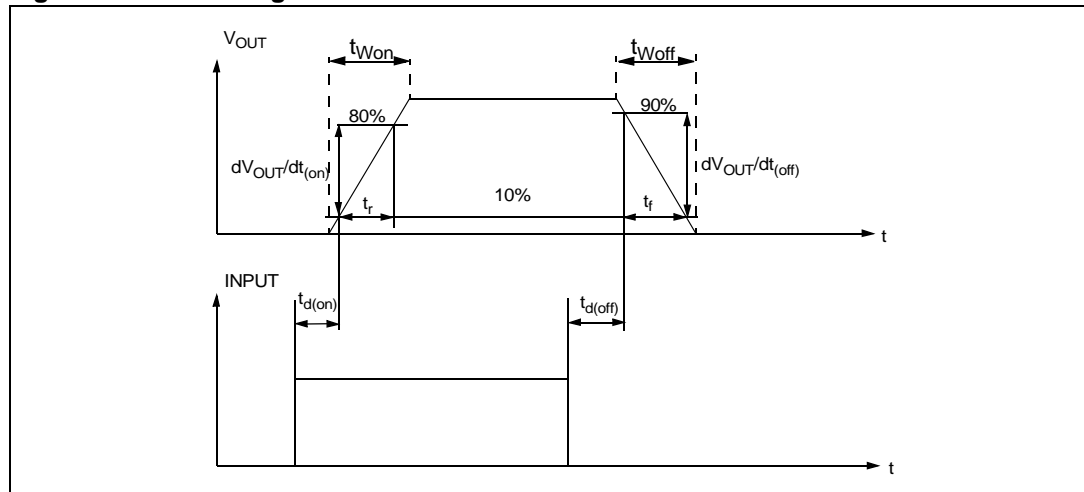
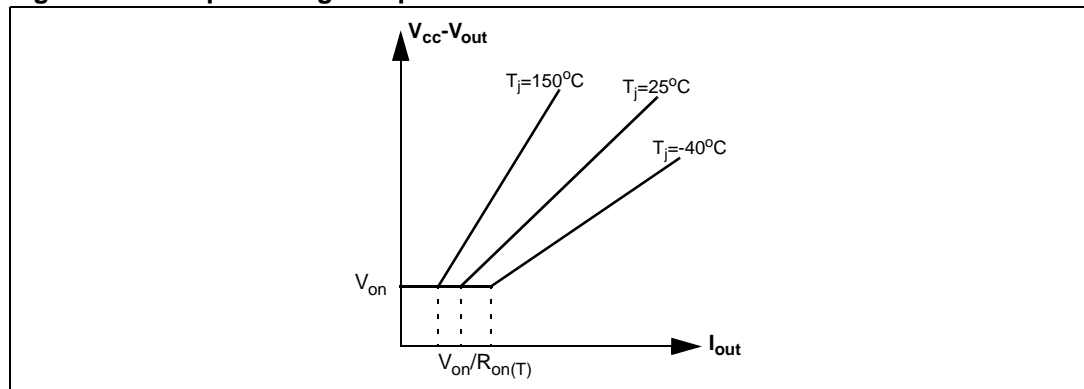


Figure 9. Output voltage drop limitation



**Table 12. Electrical transient requirements (part 1/3)**

ISO 7637-2: 2004(E) test pulse	Test levels <sup>(1)</sup>		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b <sup>(2)</sup>	+65V	+87V	1 pulse			400 ms, 2 Ω

**Table 13. Electrical transient requirements (part 2/3)**

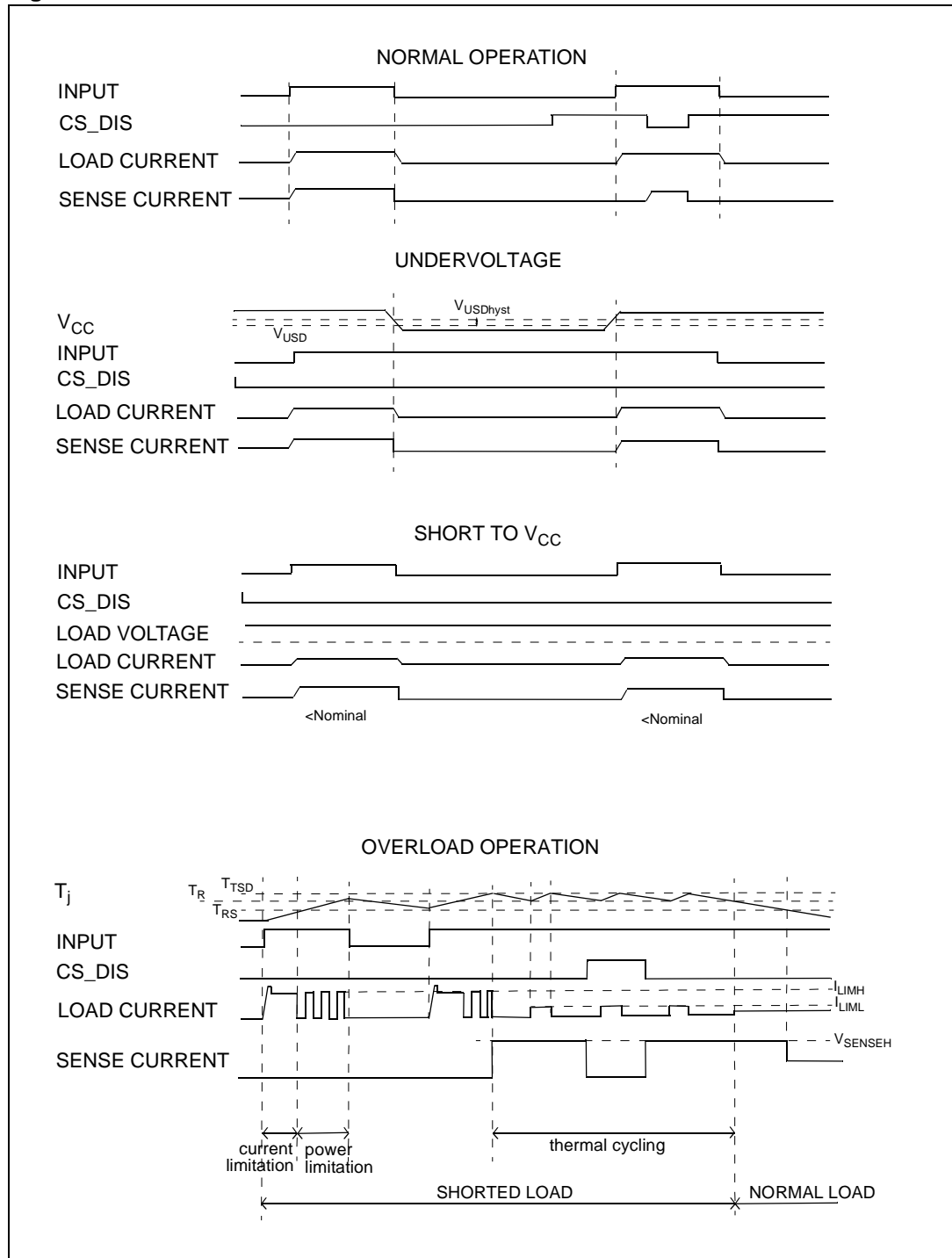
ISO 7637-2: 2004(E) test pulse	Test level results <sup>(1)</sup>	
	III	IV
1	C	C
2	C	C
3a	C	C
3b	C	C
4	C	C
5 <sup>(2)</sup>	C	C

1. The above test levels must be considered referred to  $V_{CC} = 13.5$  V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground.

**Table 14. Electrical transient requirements (part 3/3)**

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the

Figure 10. Waveforms





## 2.4 Electrical characteristics curves

Figure 11. Off-state output current

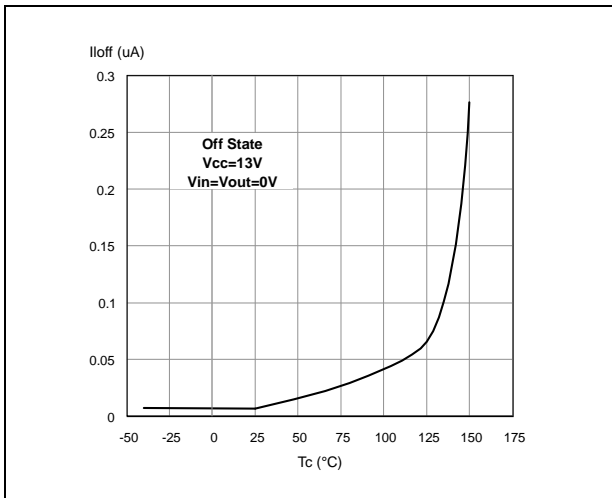


Figure 12. High level input current

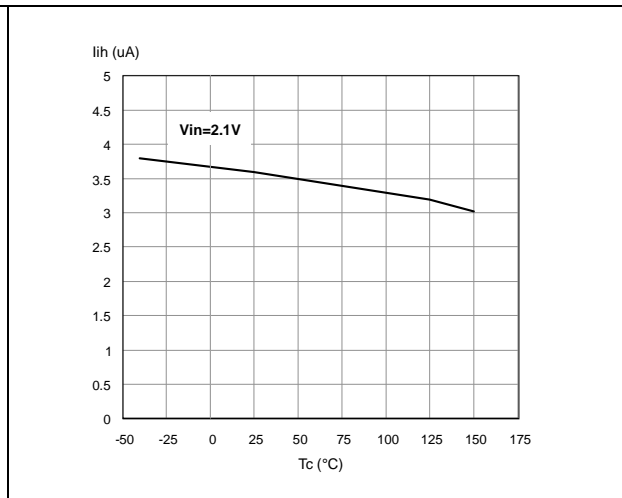


Figure 13. Input clamp voltage

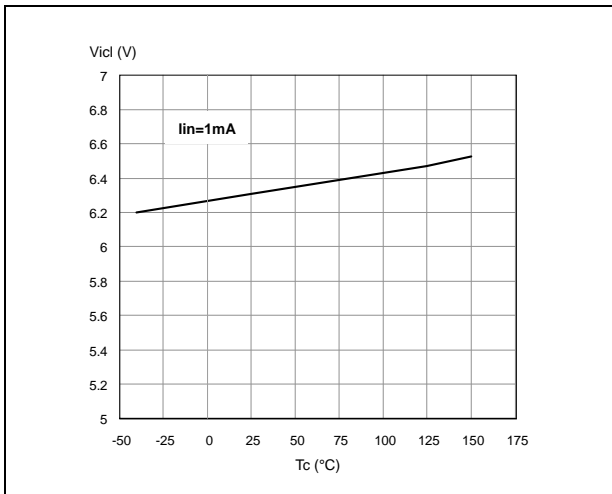


Figure 14. Input high level

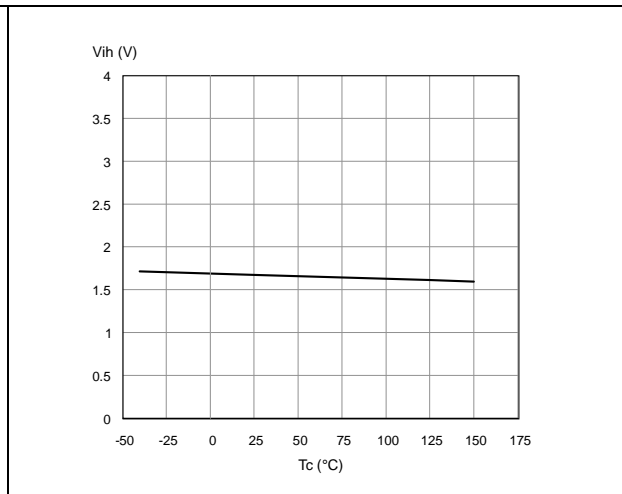


Figure 15. Input low level

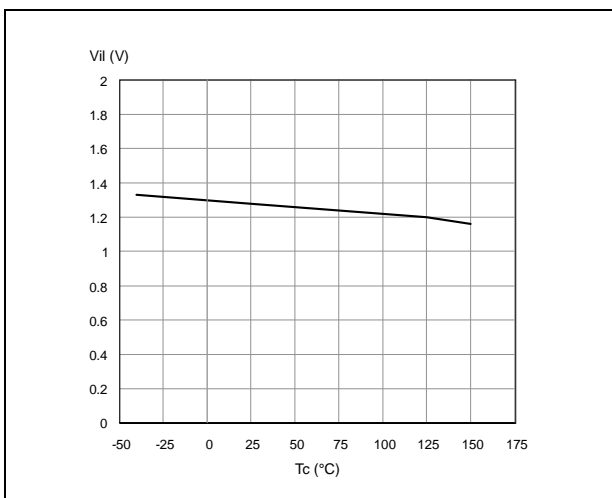


Figure 16. Input hysteresis voltage

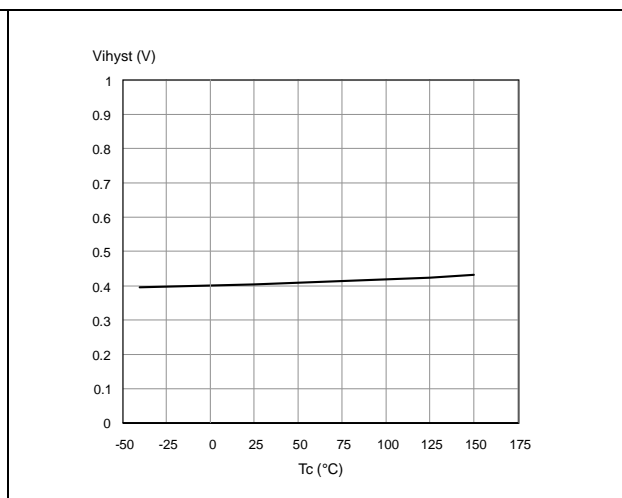


Figure 17. On-state resistance vs  $T_{case}$

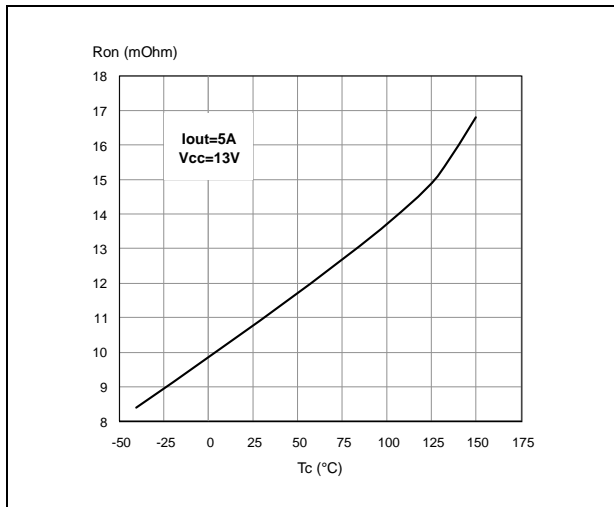


Figure 18. On-state resistance vs  $V_{CC}$

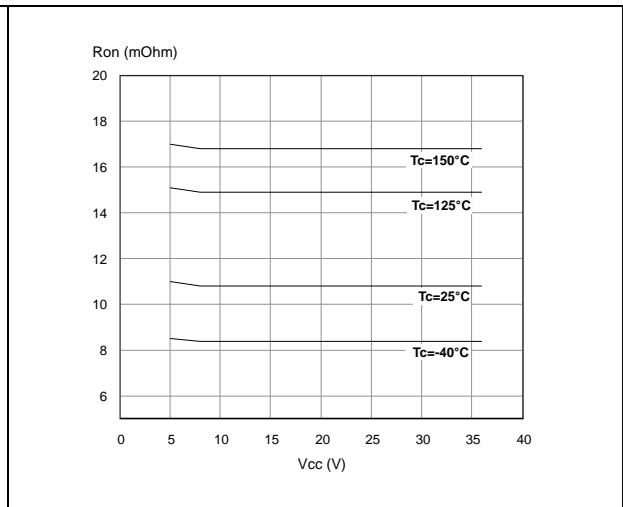


Figure 19. Undervoltage shutdown

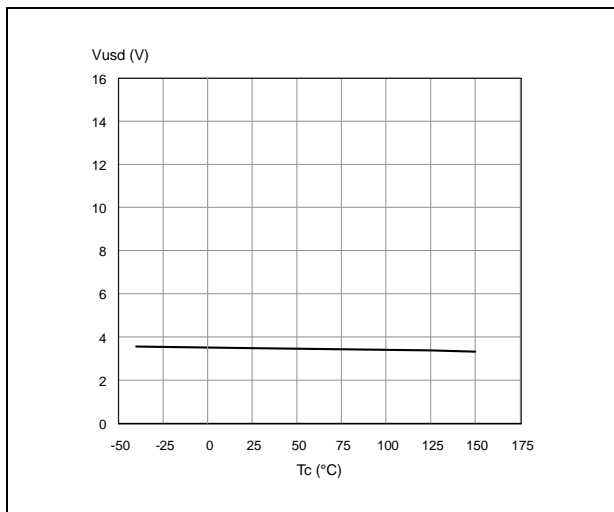


Figure 20.  $I_{LIMH}$  vs  $T_{case}$

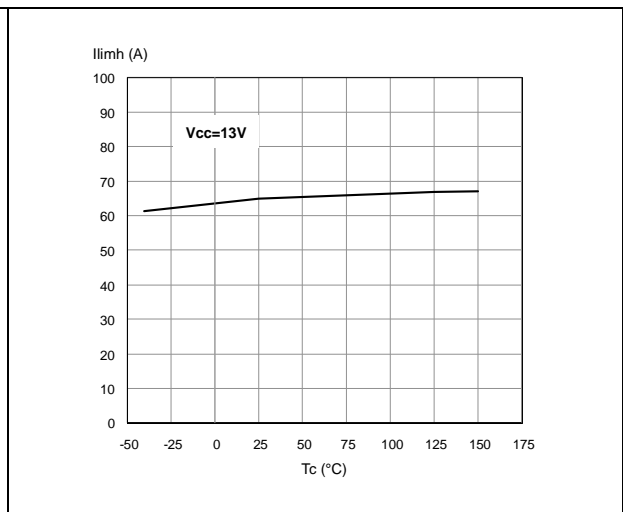


Figure 21. Turn-on voltage slope

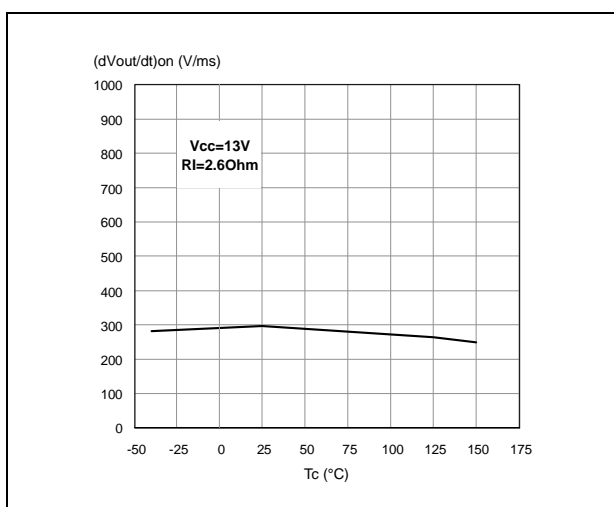


Figure 22. Turn-off voltage slope

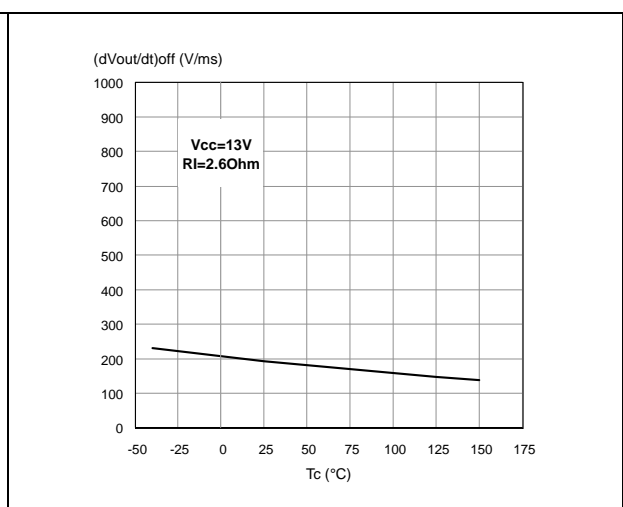


Figure 23. CS\_DIS high level voltage

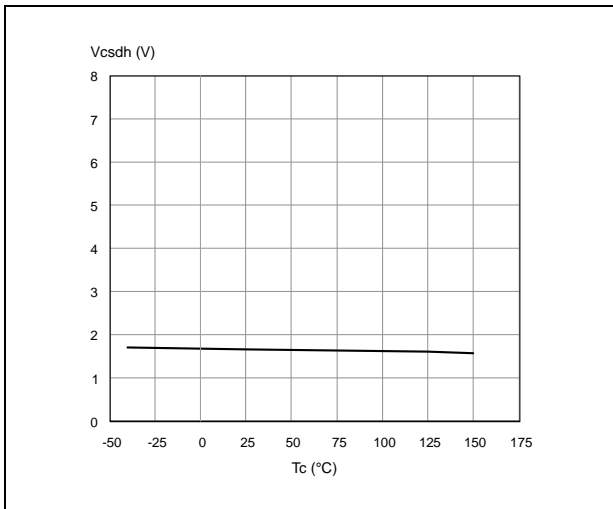


Figure 24. CS\_DIS clamp voltage

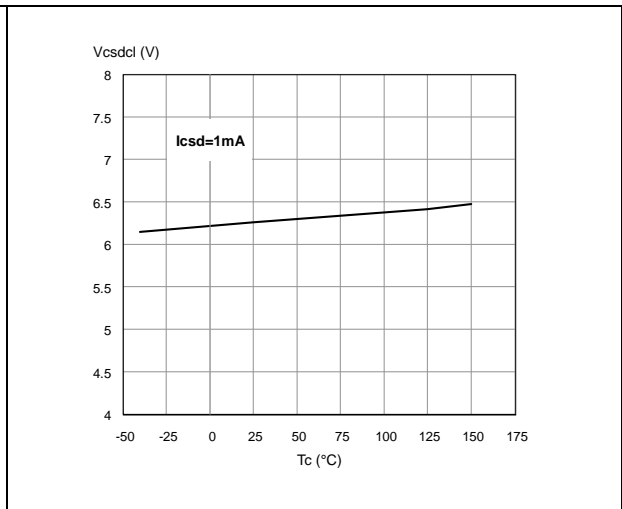
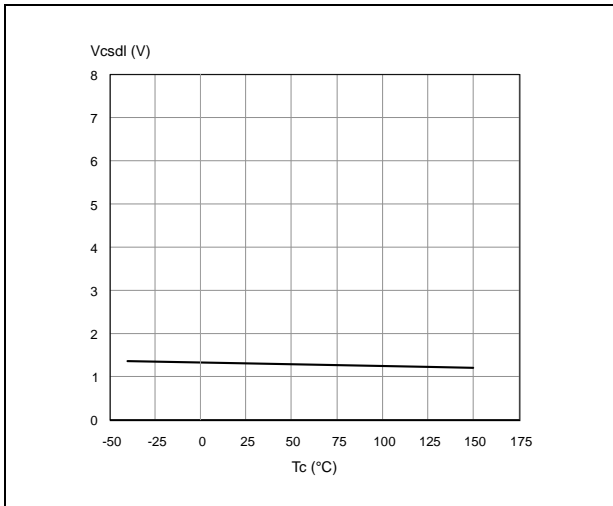
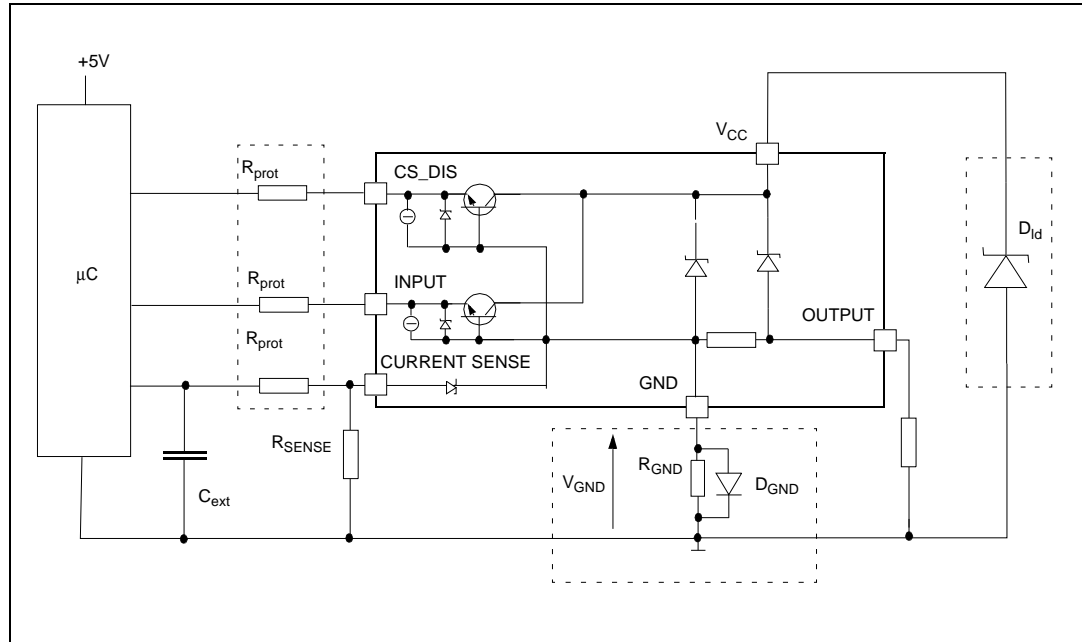


Figure 25. CS\_DIS low level voltage



### 3 Application information

Figure 26. Application schematic



#### 3.1 GND Protection network against reverse battery

##### 3.1.1 Solution 1: resistor in the ground line (R<sub>GND</sub> only)

This can be used with any type of load.

The following is an indication on how to select the R<sub>GND</sub> resistor.

1.  $R_{GND} \leq 600 \text{ mV} / (I_{S(on)max})$ .
2.  $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where  $-I_{GND}$  is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R<sub>GND</sub> (when  $V_{CC} < 0$ : during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where  $I_{S(on)max}$  becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R<sub>GND</sub> produces a shift ( $I_{S(on)max} * R_{GND}$ ) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in case of several high side drivers sharing the same R<sub>GND</sub>.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

### 3.1.2 Solution 2: a diode ( $D_{GND}$ ) in the ground line

A resistor ( $R_{GND}=1\text{ k}\Omega$ ) should be inserted in parallel to  $D_{GND}$  if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ( $\approx 600\text{ mV}$ ) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 3.2 Load dump protection

$D_{ld}$  is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the  $V_{CC}$  max DC rating. The same applies if the device is subject to transients on the  $V_{CC}$  line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

## 3.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the  $V_{CC}$  line, the control pins are pulled negative. ST suggests to insert a resistor ( $R_{prot}$ ) in line to prevent the  $\mu C$  I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of  $\mu C$  and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of  $\mu C$  I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

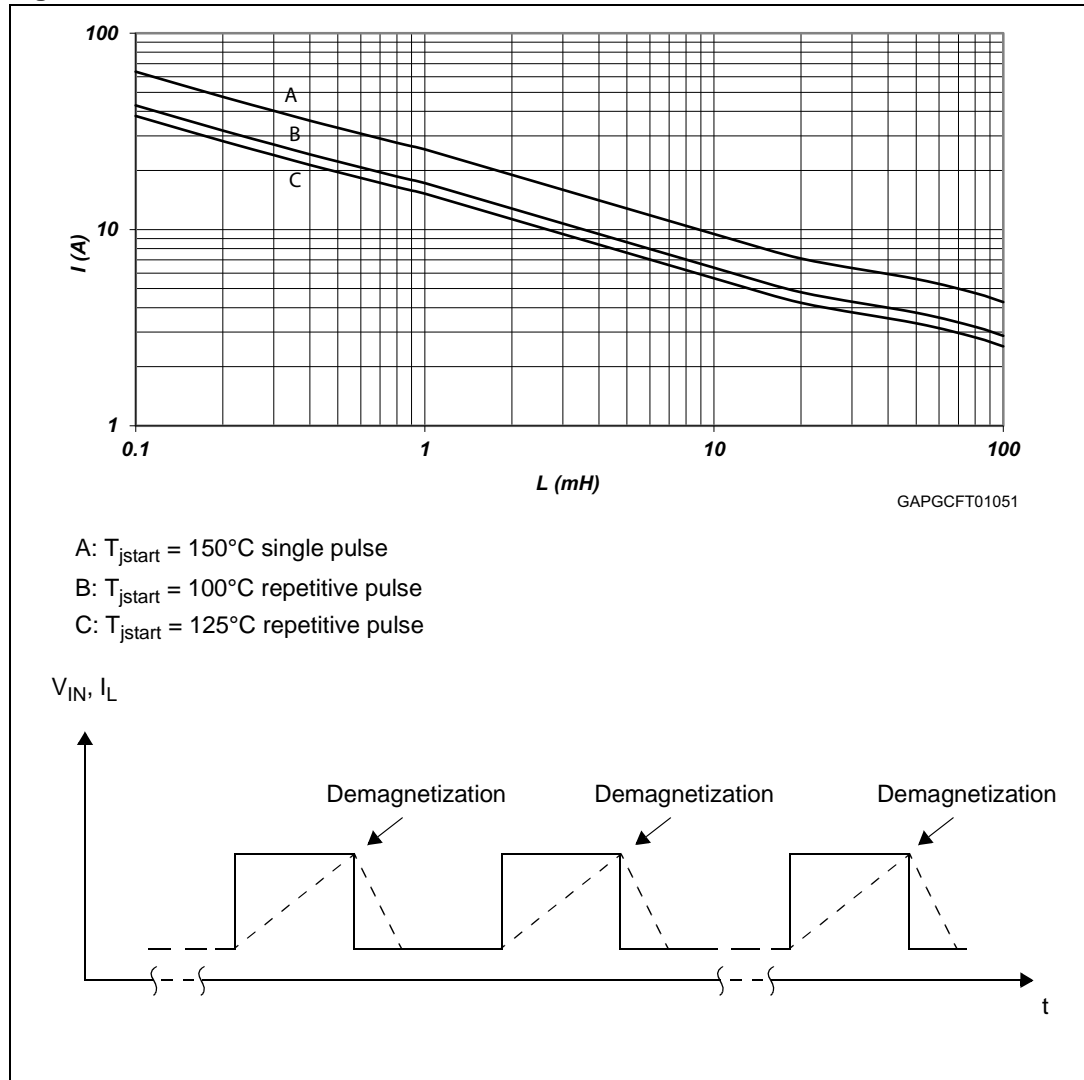
For  $V_{CCpeak} = -100\text{ V}$  and  $I_{latchup} \geq 20\text{ mA}$ ;  $V_{OH\mu C} \geq 4.5\text{ V}$

$$5\text{ k}\Omega \leq R_{prot} \leq 180\text{ k}\Omega.$$

Recommended values:  $R_{prot} = 10\text{ k}\Omega$ ,  $C_{EXT} = 10\text{ nF}$ .

### 3.4 Maximum demagnetization energy ( $V_{CC} = 13.5V$ )

Figure 27. Maximum turn-off current versus inductance

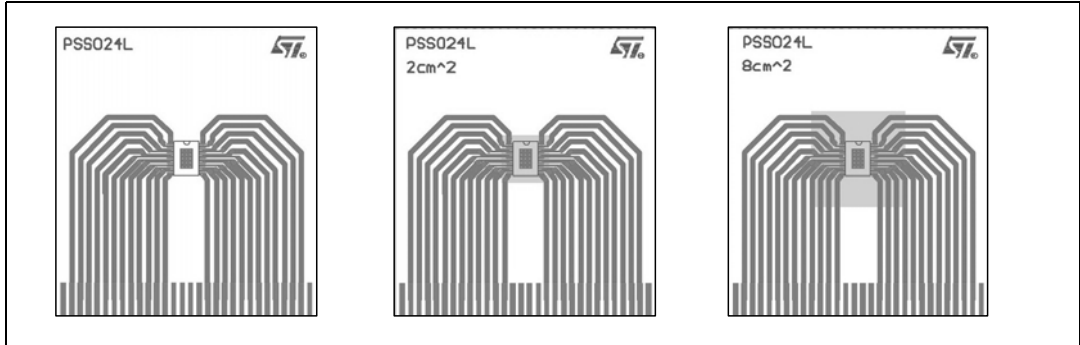


Note: Values are generated with  $R_L = 0 \Omega$ . In case of repetitive pulses,  $T_{jstart}$  (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

## 4 Package and PCB thermal data

### 4.1 PowerSSO-24 thermal data

Figure 28. PowerSSO-24 PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: Double layer, Thermal Vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6mm, Cu thickness = 70  $\mu$ m (front and back side), Copper areas: from minimum pad layout to 8 cm<sup>2</sup>).

Figure 29.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

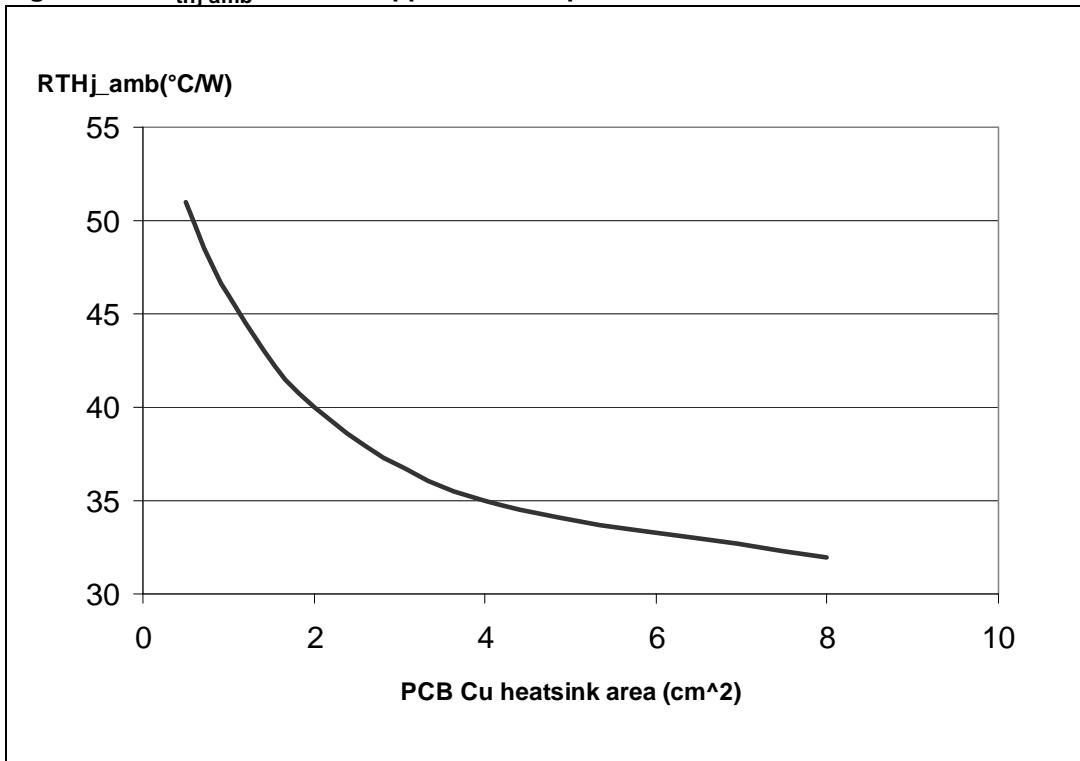
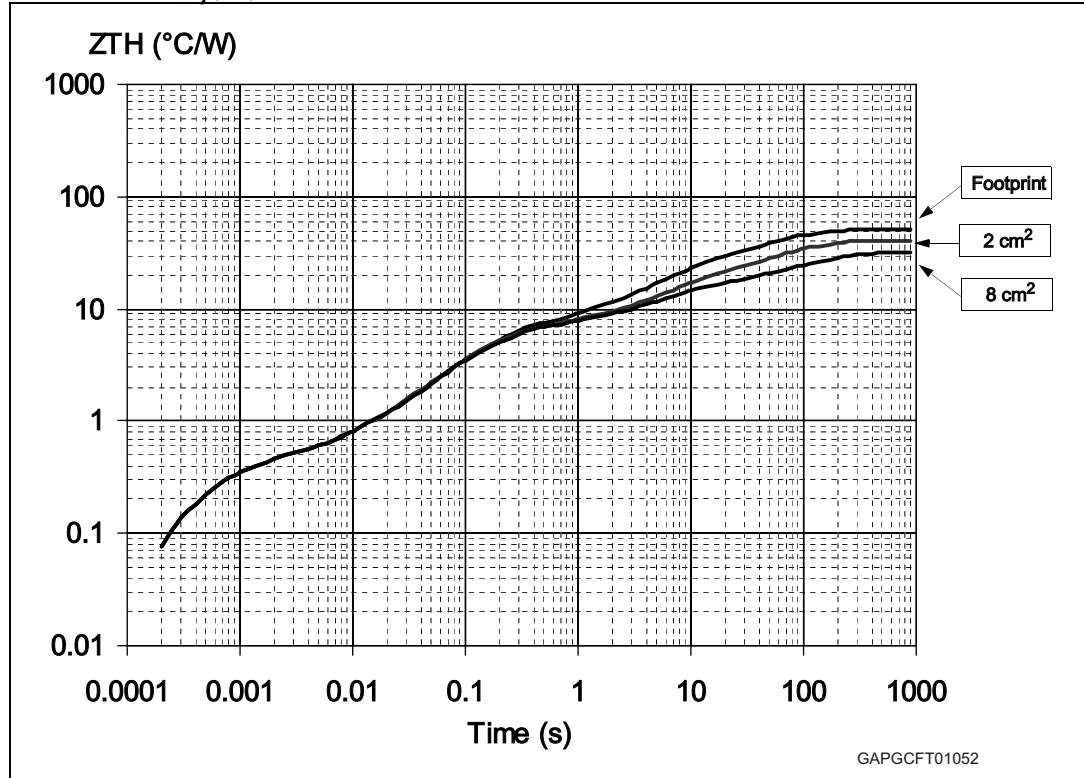


Figure 30.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

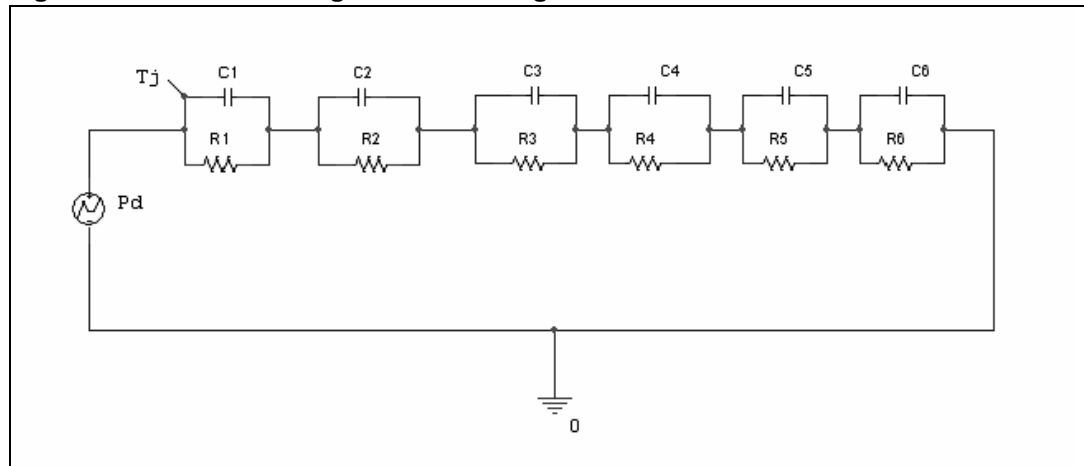


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 31. Thermal fitting model of a single channel HSD in PowerSSO-24



- The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.



Table 15. Thermal parameter

Area/island (cm <sup>2</sup> )	Footprint	2	8
R1 (°C/W)	0.1		
R2 (°C/W)	0.3		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 (W.s/°C)	0.0025		
C2 (W.s/°C)	0.0024		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com).

ECOPACK® is an ST trademark.

### 5.2 PowerSSO-24 package mechanical data

Figure 32. PowerSSO-24 package dimensions

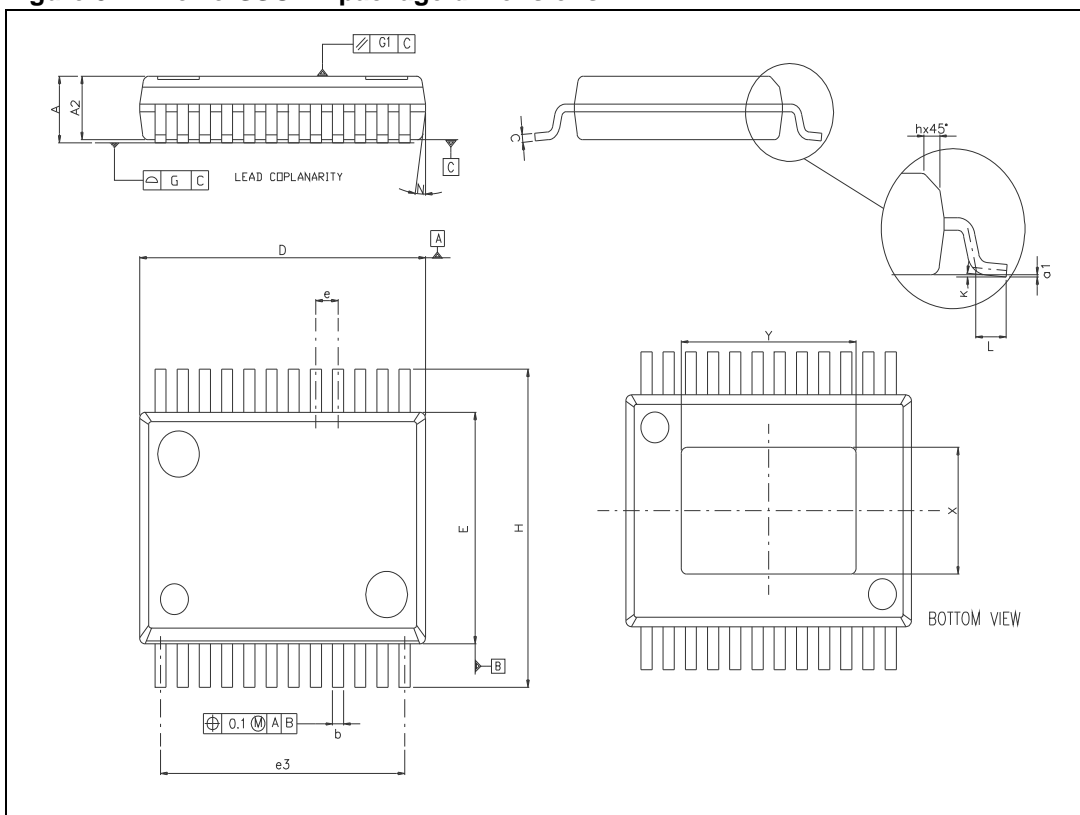


Table 16. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	-	-	2.45
A2	2.15	-	2.35
a1	0	-	0.1
b	0.33	-	0.51
c	0.23	-	0.32
D	10.10	-	10.50
E	7.4	-	7.6
e	-	0.8	-
e3	-	8.8	-
G	-	-	0.1
G1	-	-	0.06
H	10.1	-	10.5
h	-	-	0.4
L	0.55	-	0.85
N	-	-	10deg
X	4.1	-	4.7
Y	6.5	-	7.1

### 5.3 PowerSSO-24 packing information

Figure 33. PowerSSO-24 tube shipment (no suffix)

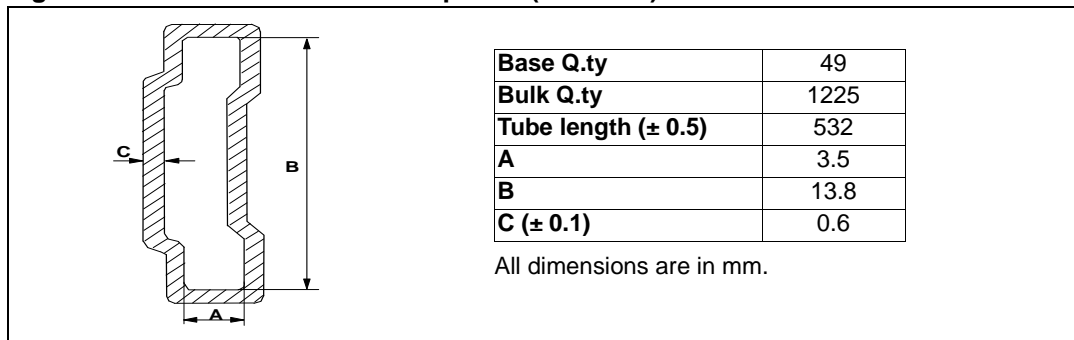
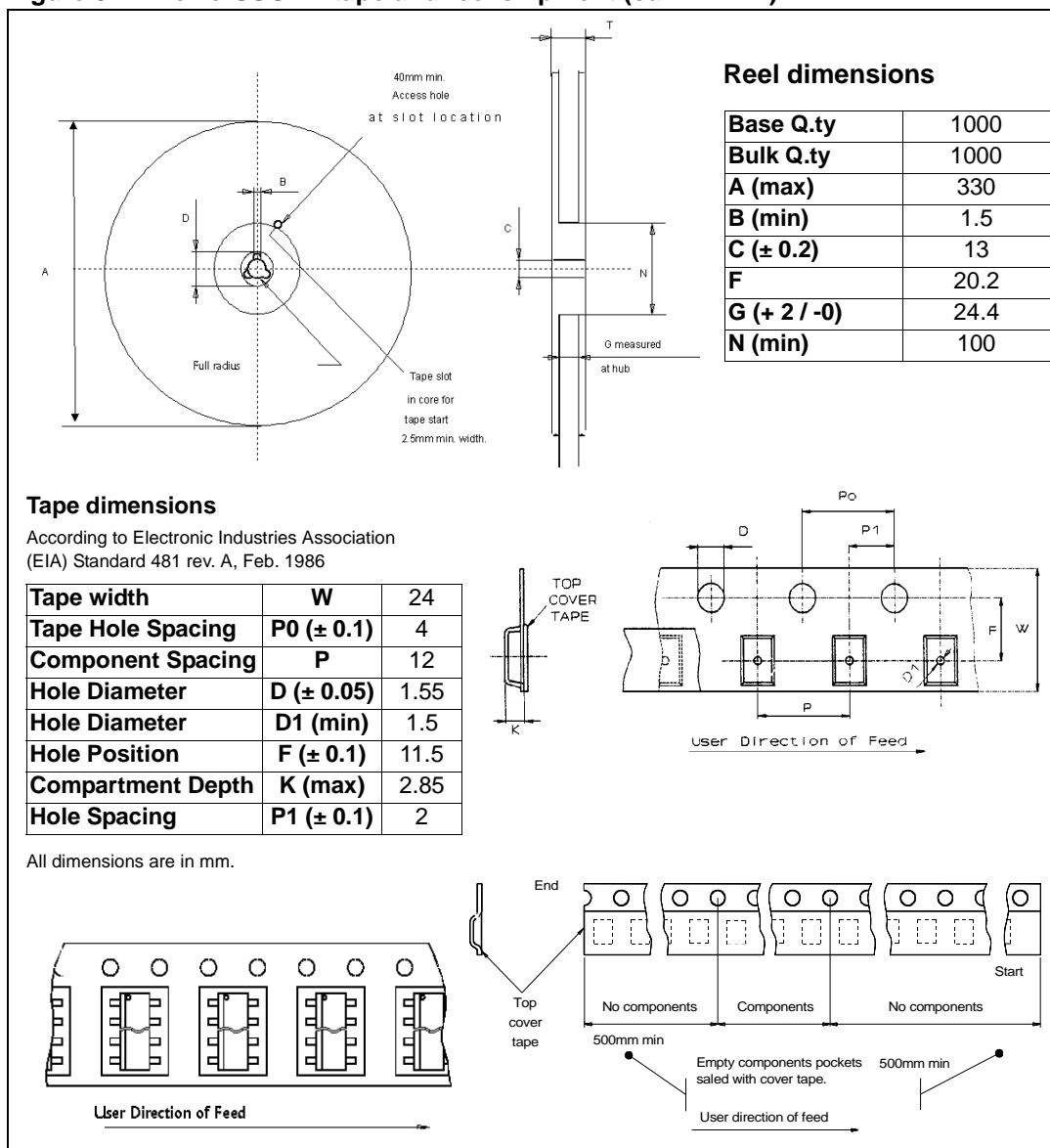


Figure 34. PowerSSO-24 tape and reel shipment (suffix “TR”)



## 6 Revision history

**Table 17. Document revision history**

Date	Revision	Changes
24-Jan-2006	1	Initial release.
13-Feb-2007	2	Document reformatted and restructured. Added <a href="#">Section 3.4: Maximum demagnetization energy (<math>V_{CC} = 13.5V</math>)</a> .
03-Oct-2007	3	Document reformatted and restructured. Added lists of tables and figures. Added <a href="#">ECOPACK® packages</a> information. <a href="#">Table 4: Absolute maximum ratings</a> : changed $E_{MAX}$ value from 283 to 508 mJ. <a href="#">Table 10: Current sense (<math>8 V &lt; V_{CC} &lt; 16 V</math>)</a> : added dk1/k1, dk2/k2, dk3/k3, $\Delta t_{DSENSE2H}$ parameters. Added <a href="#">Figure 5: Delay response time between rising edge of output current and rising edge of current sense (CS enabled)</a> . Updated <a href="#">Figure 6: <math>I_{OUT}/I_{SENSE}</math> vs <math>I_{OUT}</math></a> . Added <a href="#">Figure 7: Maximum current sense ratio drift vs load current</a> . <a href="#">Table :</a> - Updated test level values III and IV for test pulse 5b and notes.
13-Dec-2007	4	Updated <a href="#">Table 10: Current sense (<math>8 V &lt; V_{CC} &lt; 16 V</math>)</a> : – changed dk1/k1 values from $\pm 7$ to $\pm 8$ % – changed dk2/k2 values from $\pm 3$ to $\pm 5$ % – changed dk3/k3 values from $\pm 2$ to $\pm 4$ % – changed $t_{DSENSE2H}$ max value from 600 $\mu s$ to 400 $\mu s$ – changed $\Delta t_{DSENSE2H}$ max value from 250 $\mu s$ to 300 $\mu s$ – added $I_{OL}$ parameter. Updated <a href="#">Figure 7: Maximum current sense ratio drift vs load current</a> with new dk/k values.
12-Feb-2008	5	Corrected typing error in <a href="#">Table 10: Current sense (<math>8 V &lt; V_{CC} &lt; 16 V</math>)</a> : changed $I_{OL}$ test condition from $V_{IN} = 0V$ to $V_{IN} = 5V$ .
01-Aug-2008	6	Updated <a href="#">Table 16: PowerSSO-24 mechanical data</a> : changed a1 max. value from 0.075 mm to 0.1 mm.
01-Jun-2009	7	Updated <a href="#">Table 16: PowerSSO-24 mechanical data</a> : – Changed A (min) value from 2.15 mm to - and A (max) from 2.47 mm to 2.45 mm – Changed A2 (max) from 2.40 mm to 2.35 mm
18-Oct-2012	8	Updated <a href="#">Description</a>
23-Sep-2013	9	Updated Disclaimer.

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