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July 2014

FDMA1025P
Dual P-Channel PowerTrench® MOSFET
–20V, –3.1A, 155mΩ

Features

- Max $r_{DS(on)}$ = 155mΩ at V_{GS} = –4.5V, I_D = –3.1A
- Max $r_{DS(on)}$ = 220mΩ at V_{GS} = –2.5V, I_D = –2.3A
- Low profile - 0.8mm maximum - in the new package MicroFET 2X2 mm
- RoHS Compliant
- Free from halogenated compounds and antimony oxides

General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra - portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

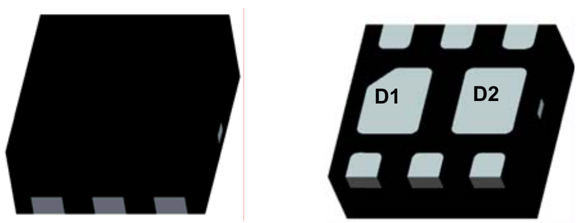
The MicroFET 2X2 package offers exceptional thermal performance for its physical size and well suited to linear mode applications.

Application

- DC - DC Conversion

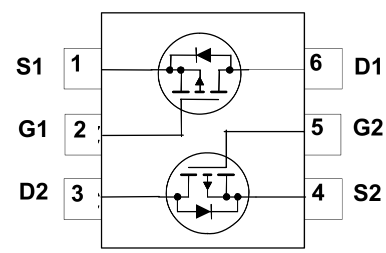
PIN 1

S1 G1 D2



D1 G2 S2

MicroFET 2X2



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		–20	V
V_{GS}	Gate to Source Voltage		±12	V
I_D	Drain Current -Continuous	(Note 1a)	–3.1	A
	-Pulsed		–6	
P_D	Power Dissipation for Single Operation	(Note 1a)	1.4	W
	Power Dissipation	(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance Single Operation, Junction to Ambient	(Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance Single Operation, Junction to Ambient	(Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance Dual Operation, Junction to Ambient	(Note 1c)	69	
$R_{\theta JA}$	Thermal Resistance Dual Operation, Junction to Ambient	(Note 1d)	151	

Package Marking and Ordering Information

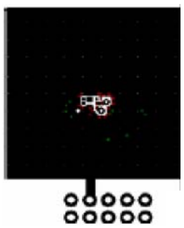
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
025	FDMA1025P	MicroFET 2X2	7''	8mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

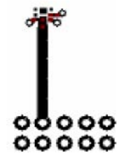
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = –250μA, V_{GS} = 0V	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16V, V_{GS} = 0V			–1	μA
		V_{DS} = –16V, V_{GS} = 0V, T_J = 125°C			–100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = –250μA	–0.4	–0.9	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = –250μA, referenced to 25°C		–3.8		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –4.5V, I_D = –3.1A		88	155	mΩ
		V_{GS} = –2.5V, I_D = –2.3A		144	220	mΩ
		V_{GS} = –4.5V, I_D = –3.1A, T_J = 125°C		121	220	mΩ
g_{FS}	Forward Transconductance	V_{DS} = –5V, I_D = –3.1A		6.2		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –10V, V_{GS} = 0V, f = 1MHz		340	450	pF
C_{oss}	Output Capacitance			80	105	pF
C_{rss}	Reverse Transfer Capacitance			45	70	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = –10V, I_D = –3.1A, V_{GS} = –4.5V, R_{GEN} = 6Ω		5	10	ns
t_r	Rise Time			14	26	ns
$t_{d(off)}$	Turn-Off Delay Time			13	24	ns
t_f	Fall Time			8	16	ns
$Q_{g(TOT)}$	Total Gate Charge at 4.5V	V_{GS} = 0V to –4.5V, V_{DD} = –10V, I_D = –3.1A		3.4	4.8	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = –10V, I_D = –3.1A		0.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			1.0		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Source-Drain Diode Forward				–1.1	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = –1.1A (Note 2)		–0.8	–1.2	V
t_{rr}	Reverse Recovery Time	I_F = –3.1A, di/dt = 100A/μs		17	26	ns
Q_{rr}	Reverse Recovery Charge			10	15	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   (a) $R_{\theta JA}$ = 86 °C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
   (b) $R_{\theta JA}$ = 173 °C/W when mounted on a minimum pad of 2 oz copper. For single operation.
   (c) $R_{\theta JA}$ = 69 ^{o}C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5 ” x 1.5 ” x 0.062 ” thick PCB. For dual operation.
   (d) $R_{\theta JA}$ = 151 ^{o}C/W when mounted on a minimum pad of 2 oz copper. For dual operation.

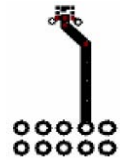


a)86 ^{o}C/W when mounted on a 1 in^2 pad of 2 oz copper.



b)173 ^{o}C/W when mounted on a minimum pad of 2 oz copper.

c)69 ^{o}C/W when mounted on a 1 in^2 pad of 2 oz copper.



d)151 ^{o}C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0

Typical Characteristics T_J = 25°C unless otherwise noted

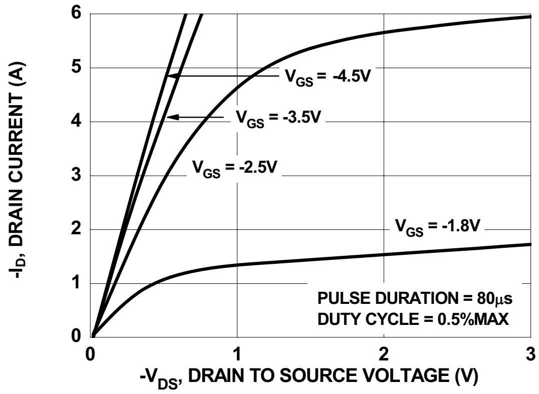


Figure 1. On Region Characteristics

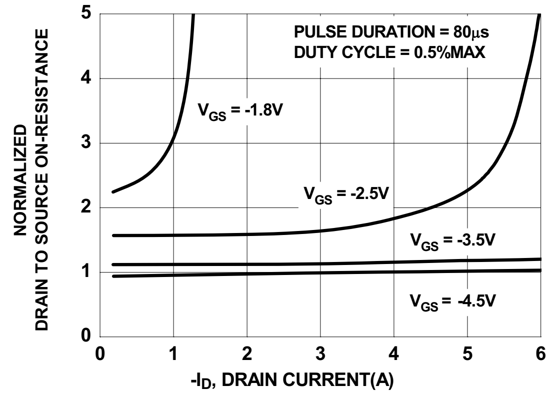


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

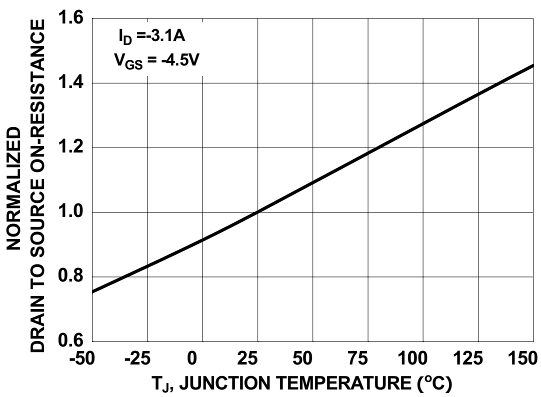


Figure 3. Normalized On Resistance vs Junction Temperature

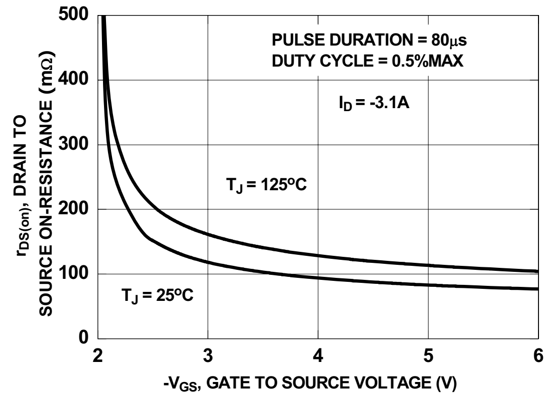


Figure 4. On-Resistance vs Gate to Source Voltage

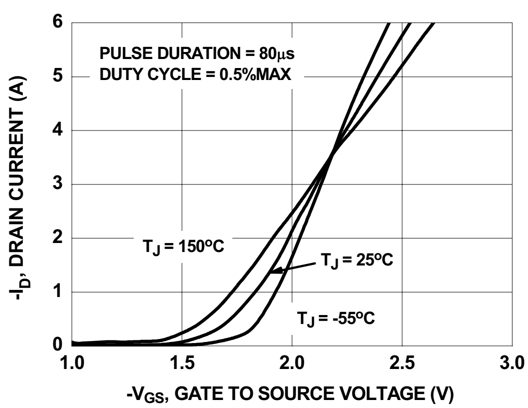


Figure 5. Transfer Characteristics

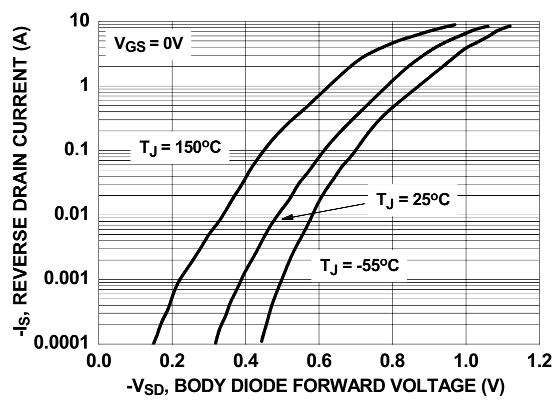


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

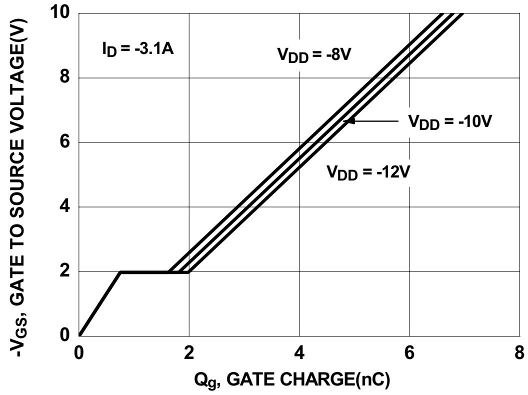


Figure 7. Gate Charge Characteristics

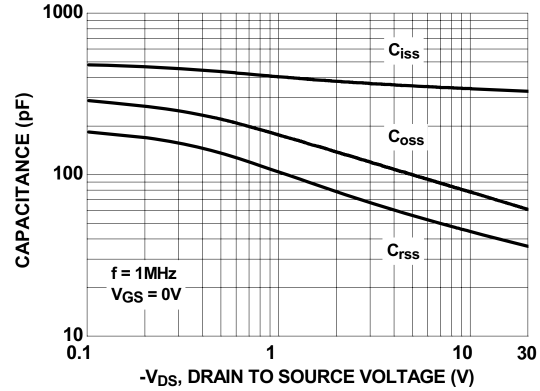


Figure 8. Capacitance vs Drain to Source Voltage

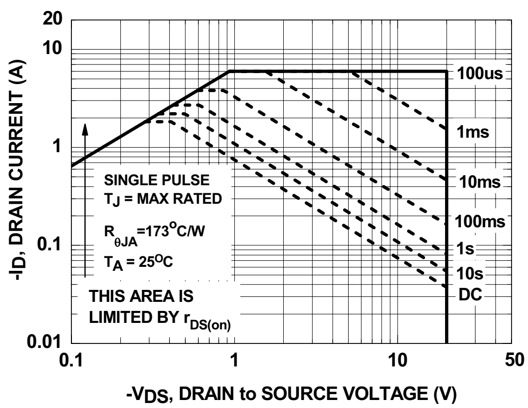


Figure 9. Forward Bias Safe Operating Area

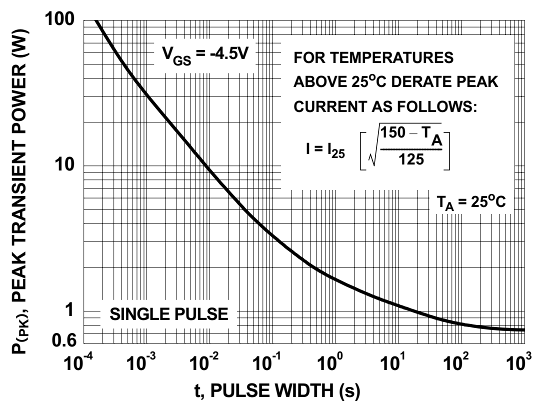


Figure 10. Single Pulse Maximum Power Dissipation

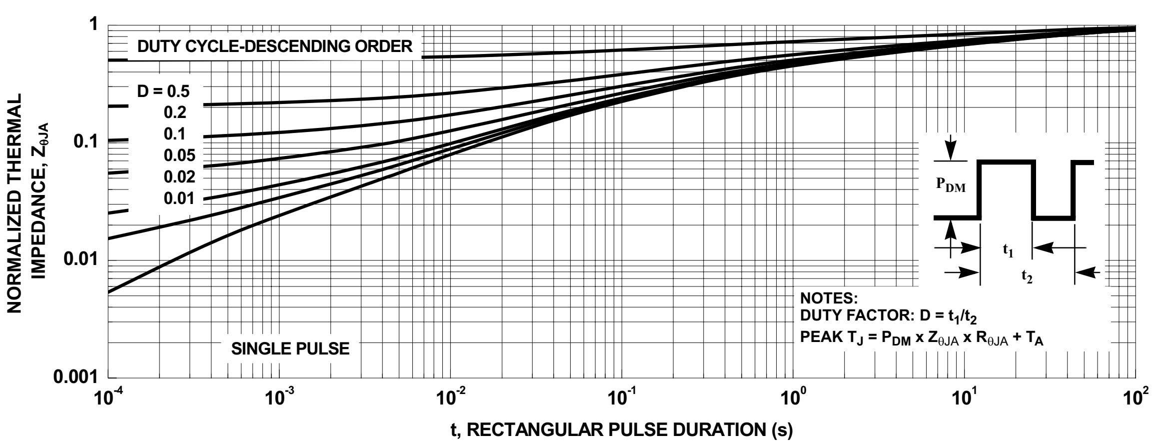
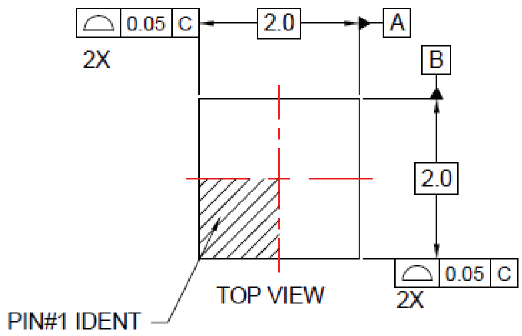
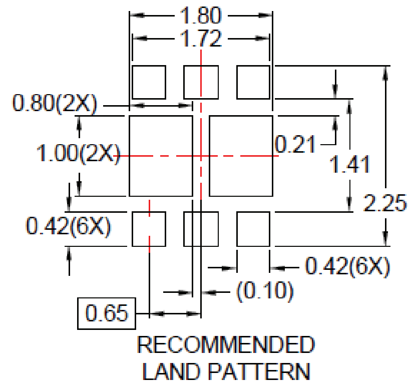
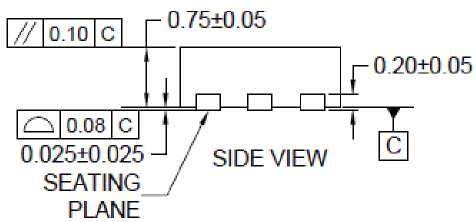


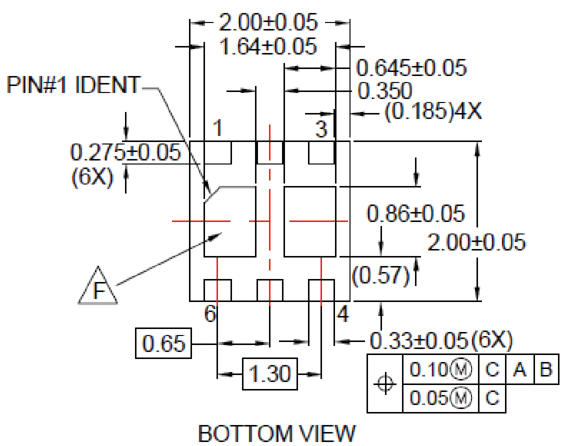
Figure 11. Transient Thermal Response Curve

Dimensional Outline and Pad Layout









NOTES:

A. CONFORM TO JADEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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Rev. I68

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