REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make changes to 1.5 and glassivation as specified under APPENDIX A. - ro	99-04-13	Raymond Monnin
B	Add device type 02. Make changes to 1.2.2, 1.4, table I, figures 1, 2, 3 and APPENDIX A. - ro	99-06-02	Raymond Monnin
C	Update drawing to current requirements. Editorial changes throughout. – drw	06-08-24	Raymond Monnin
D	Add device types 03 and 04. Delete figure 4 Radiation exposure circuit, paragraph 4.4.4.3 Single event phenomena (SEP), Latch up information, and references to device class M requirements. - ro	15-06-25	Charles F. Saffle
E	Add device type 05, case outlines Y and Z, single event phenomena (SEP) and figure A-2. - ro	17-03-23	Charles F. Saffle

REV																				
SHEET																				
REV	E	E	E	E	E	E	E	E	E	E	E									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS	REV	E	E	E	E	E	E	E	E	E	E	E	E	E
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Rick Officer

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
99-04-01

REVISION LEVEL
E

MICROCIRCUIT, DIGITAL-LINEAR, RADIATION HARDENED DUAL INVERTING MOSFET DRIVER, MONOLITHIC SILICON

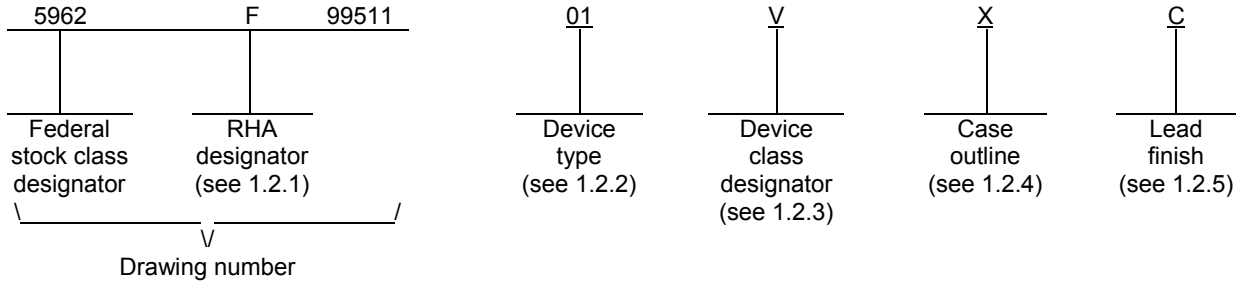
SIZE	CAGE CODE	
A	**67268**	**5962-99511**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of high reliability (device class Q), space application (device class V) and for appropriate satellite and similar applications (device class T). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class T, the user is encouraged to review the manufacturer's Quality Management (QM) plan as part of their evaluation of these parts and their acceptability in the intended application.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q, T and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-4423RH	Radiation hardened dual inverting MOSFET drivers with < 10 V lockout voltage
02	HS-4423BRH	Radiation hardened dual inverting MOSFET drivers with < 7.5 V lockout voltage
03	HS-4423EH	Radiation hardened dual inverting MOSFET drivers with < 10 V lockout voltage
04	HS-4423BEH	Radiation hardened dual inverting MOSFET drivers with < 7.5 V lockout voltage
05	RH-PM4423	Radiation hardened 4.5 A dual inverting low side MOSFET driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q, V	Certification and qualification to MIL-PRF-38535
T	Certification and qualification to MIL-PRF-38535 with performance as specified in the device manufacturers approved quality management plan.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDFP4-F16	16	Flat pack
Y	CDFP4-F16	16	Flat pack 1/
Z	See figure 1	10	Flat pack 2/ 3/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q, T and V.

1.3 Absolute maximum ratings. 4/

Device types 01, 02, 03, 04:

Supply voltage range (V_S)	10 V to 20 V
Input voltage range (V_{IN})	-0.3 V to +V 5/
Output short circuit duration (single supply)	Continuous 6/
Maximum junction temperature (T_J)	175°C
Maximum storage temperature	-65°C to +150°C
Maximum lead temperature (soldering 10 seconds)	265°C
Thermal resistance, junction-to-case (θ_{JC})	18°C/W
Thermal resistance, junction-to-ambient (θ_{JA})	90°C/W 7/

Device type 05:

Supply voltage range (V_S)	PGND -0.3 V to PGND + 20 V
Signal ground (SGND)	PGND – 5 V to PGND + 5 V
Input voltage (PWM1 and PWM2)	SGND – 0.3 V to VS + 0.3 V
Driver output voltage (OUT1 and OUT2)	PGND – 0.3 V to VS + 0.3 V
DC output current (for each driver)	750 mA
Storage temperature range	-65°C to +150°C
Maximum junction temperature (T_J)	150°C
Lead temperature (soldering 10 seconds)	260°C 8/
Maximum power dissipation (P_D) at T_A = 70°C:	
Case Y	1.10 W
Case Z	0.7 W
Maximum power dissipation (P_D) at T_A = 125°C:	
Case Y	0.36 W
Case Z	0.21 W

1/ AIN ceramic header with metalized bottom side pull back of 0.001 inch x 0.02 inch.
2/ AI2O3 ceramic header.
3/ The lid is connected to the seal ring (the pin 4 of the package).
4/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
5/ Inputs must not go more negative than -0.3 V.
6/ Short circuit from the output to V_S can cause excessive heating and eventual destruction.
7/ θ_{JA} is measured with the component mounted on an evaluation printed circuit (PC) board in free air.
8/ Distance not less than 1.5 mm from the device body and the same lead shall not be re-soldered until 3 minutes have elapsed.

1.3 Absolute maximum ratings - continued. 4/

Thermal resistance, junction-to-case (θ_{JC}):
- Case Y ..... 8°C/W
- Case Z ..... 25°C/W

Thermal resistance, junction-to-ambient (θ_{JA}):
- Case Y ..... 70°C/W 9/
- Case Z ..... 117°C/W 9/

1.4 Recommended operating conditions.

Supply voltage range (V_S):
- Device types 01, 02, 03, 04 ..... 12 V to 18 V
- Device type 05 ..... 4.65 V to 18 V

Low voltage lockout voltage:
- Device types 01 and 03 ..... < 10.0 V
- Device types 02 and 04 ..... < 7.5 V

Operating temperature range ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (high dose rate = 50 – 300 rad(Si)/s):
- Device types 01 and 02:
  - Device classes Q and V ..... 300 krad(Si) 10/
  - Device class T ..... 100 krad(Si) 10/
- Device types 03 and 04 ..... 300 krad(Si) 11/
- Device type 05 ..... 100 krad(Si) 12/

Maximum total dose available (low dose rate ≤ 0.01 rad(Si)/s):
- Device types 03 and 04 ..... 50 krad(Si) 11/
- Device type 05 ..... 100 krad(Si) 12/

Single event phenomena (SEP) :
- Device type 05:
  - No SEL occurs at normal LET (see 4.4.4.3) ..... ≤ 60 MeV/(mg/cm^2) 13/
  - SET observed at LET (see 4.4.4.3) (saturated cross section = 1.1 X10^{-6}cm^2) ..... ≥ 18 MeV/(mg/cm^2) 13/

9/ Measured on 2s2p board as per standard JEDEC (JEDS51-7) in natural convection.

10/ Device types 01 and 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. Device types 01 and 02 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for class Q or V and 100 krads(Si) for class T.

11/ Device types 03 and 04 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

12/ The manufacturer supplying device type 05 has performed characterization testing in accordance with MIL-STD-883 method 1019 condition A (high dose rate = 50 – 300 rads(Si)/s) and condition D (low dose rate = 10 mrads(Si)/s) to a dose level of 100 krad(Si). Manufacturer also performed accelerated annealing 1.5X over test and observed no time dependent effects. The post-irradiation of HDR and LDR test parametric values falls within the specification limits as specified in Table IA. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and D.

13/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP characteristics, but are not production tested unless specified by the customer through the purchase order or contract. For more information on SEP test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

JEDEC Solid State Technology Association

JEDEC 51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
JEDEC PUB 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3 for device types 01, 02, 03, and 04.

3.2.4 Block diagram. The logic diagram shall be as specified on figure 4 for device type 05.

3.2.5 Truth table. The truth table shall be as specified in figure 5.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current, low	I_{CCSB} low	V_S = 18 V, inputs = 0 V	1	01, 02, 03, 04		3.5	mA
			2, 3			4.0	
		M,D,P,L,R,F 2/	1			4.0	
Power supply current, high	I_{CCSB} high	V_S = 18 V, inputs = 18 V	1	01, 02, 03, 04		3.5	mA
			2, 3			4.0	
		M,D,P,L,R,F 2/	1			4.0	
Input current, low	I_{IL}	V_S = 18 V	1	01, 02		±2	µA
			2, 3			±4	
		M,D,P,L,R,F 2/	1			±4	
		V_S = 18 V	1	03, 04		±5	
			2, 3			±10	
		M,D,P,L,R,F 2/	1			±10	
Input current, high	I_{IH}	V_S = 18 V	1	01, 02		±2	µA
			2, 3			±4	
		M,D,P,L,R,F 2/	1			±4	
		V_S = 18 V	1	03, 04		±5	
			2, 3			±10	
		M,D,P,L,R,F 2/	1			±10	
Voltage output	V_{OL}, V_{OH}	V_S = 12 V	1	01, 02, 03, 04	V_S – 0.75	0.8	V
			2, 3		V_S – 0.75	0.8	
		M,D,P,L,R,F 2/	1		V_S – 0.75	0.8	
Input voltage	V_{IL}, V_{IH}	V_S = 12 V, limits applied during functional test	1	01, 02, 03, 04	3.0	0.4	V
			2, 3		3.5	0.4	
		M,D,P,L,R,F 2/	1		3.5	0.4	
Functional test	FT	V_S = 12 V, V_S = 18 V	7, 8A, 8B	01, 02, 03, 04			
		M,D,P,L,R,F 2/	7				

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation delay, low	t_{PHL}	V_S = 12 V,	9	01, 02,		250	ns
		C_L = 4300 pF	10, 11	03, 04		350	
		M,D,P,L,R,F 2/	9			350	
Propagation delay, high	t_{PLH}	V_S = 12 V	9	01, 02,		250	ns
		C_L = 4300 pF	10, 11	03, 04		350	
		M,D,P,L,R,F 2/	9			350	
Response time, rise	TR	V_S = 12 V,	9	01, 02,		75	ns
		C_L = 4300 pF	10, 11	03, 04		95	
		M,D,P,L,R,F 2/	9			95	
Response time, fall	TF	V_S = 12 V,	9	01, 02,		75	ns
		C_L = 4300 pF	10, 11	03, 04		95	
		M,D,P,L,R,F 2/	9			95	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply current, low	ICCSB low = ICCL	V_S = 4.65 V, inputs = 0 V	1	05		1.5	mA
			2			1.7	
			3			1.4	
		V_S = 18 V, inputs = 0 V	1			2.1	
			2			2.4	
			3			2	
Power supply current, high	ICCSB high = ICCH	V_S = 4.65 V, inputs = 3.3 V	1	05		1.5	mA
			2			1.7	
			3			1.4	
		V_S = 18 V, inputs = 3.3 V	1			2.1	
			2			2.4	
			3			2	
Input current, low and high 3/	IPWM = I_{IL} and I_{IH}	V_S = 4.65 V and 18 V, PWMx = 0 V	1,2,3	05	-1	+1	µA
		V_S = 4.65 V and 18 V, PWMx = 3.3 V				+2	
High level output voltage	V_{OH}	V_S = 4.65 V and 18 V, inputs = 3.3 V, outputs = 1 mA	1,2,3	05	V_S – 0.01		V
Low level output voltage	V_{OL}	V_S = 4.65 V and 18 V, inputs = 0 V, outputs = 1 mA	1,2,3	05		10	mV
Input voltage high, PWMx	V_{IH}	V_S = 4.65 V and 18 V, inputs = rise ramp	1,2,3	05	2		V
Input voltage low, PWMx	V_{IL}	V_S = 4.65 V and 18 V, inputs = fall ramp	1,2,3	05		0.8	mV
Under voltage lock out threshold turn on 3/	$UVLO_{(ON)}$	V_S = rising (rise ramp), PWMx = 3.3 V	1,2,3	05		4.65	V
Under voltage lock out threshold turn off 3/	$UVLO_{(OFF)}$	V_S = falling (fall ramp), PWMx = 3.3 V	1,2,3	05	3.6		V
Under voltage lock out hysteresis 3/	$UVLO_{(HYST)}$	UVLOhyst = turn on – turn off	1,2,3	05		0.4	V

See footnotes at end of table.

TABLE IA Electrical performance characteristics - Continued.

Test	Symbol	Conditions 2/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Source resistance	RHI	V_S = 10 V, inputs = 3.3 V, I_{OUT} = 100 mA	1	05		1.1	Ω
			2			1.4	
			3			1.0	
Sink resistance	RLO	V_S = 10 V, inputs = 0 V, I_{OUT} = 100 mA	1	05		1.4	Ω
			2			1.9	
			3			1.2	
Propagation delay, low	t_{PHL}	V_S = 10 V, C_{OUT} to GND = 10 nF	9, 10	05		175	ns
			11			300	
Propagation delay, high	t_{PLH}	V_S = 10 V, C_{OUT} to GND = 10 nF	9, 10	05		175	ns
			11			300	
Response time, rise 3/	TR	V_S = 10 V, C_{OUT} = 10 nF	9,10,11	05		60	ns
Response time, fall 3/	TF	V_S = 10 V, C_{OUT} = 10 nF	9,10,11	05		60	ns

1/ V_S = 12 V to 18 V for device types 01, 02, 03, and 04. V_S = 4.65 V to 18 V for device type 05.

2/ RHA device types 01 and 02 supplied to this drawing will meet all levels M, D, P, L, R and F of irradiation for device classes Q or V and levels M, D, P, L, and R of irradiation for device class T. However, device types 01 and 02 are only tested at the “F” level for device classes Q or V and the “R” level for device class T in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein).

RHA device types 03 and 04 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and irradiation of M, D, P, and L levels for condition D. However, device types 03 and 04 are only tested at the “F” level in accordance with MIL-STD-883, method 1019, condition A, and tested at the “L” level in condition D (see 1.5 herein).

RHA device type 05 has been characterized through all levels M, D, P, L, and R of irradiation. However, device type 05 is only tested at the “R” level.

Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

3/ Go no go test only.

TABLE IB. SEP test limits. 1/ 2/

Device type	V_S = 4.65 V and 18 V		Bias V_S = 18 V, For latch-up test No latch-up (SEL) occurs at incident angle effective LET 4/
	SET observed threshold LET 3/	Maximum device cross section	
05	LET = 18 MeV/(mg/cm^2)	1.1 X10^{-6}cm^2	LET ≤ 60 MeV/(mg/cm^2)

1/ For single event phenomena (SEP) test conditions, see 4.4.4.3 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by the technical review board and qualifying activity.
3/ SET was observed at LET= 18 MeV/(mg/cm^2) with cross section 1.1 X10^{-6}cm^2 .
4/ No single-event latch up (SEL) was observed when irradiated with Xe ions at normal incidence angle corresponding to a surface LET of 60 MeV/(mg/cm^2).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

Case outline Z

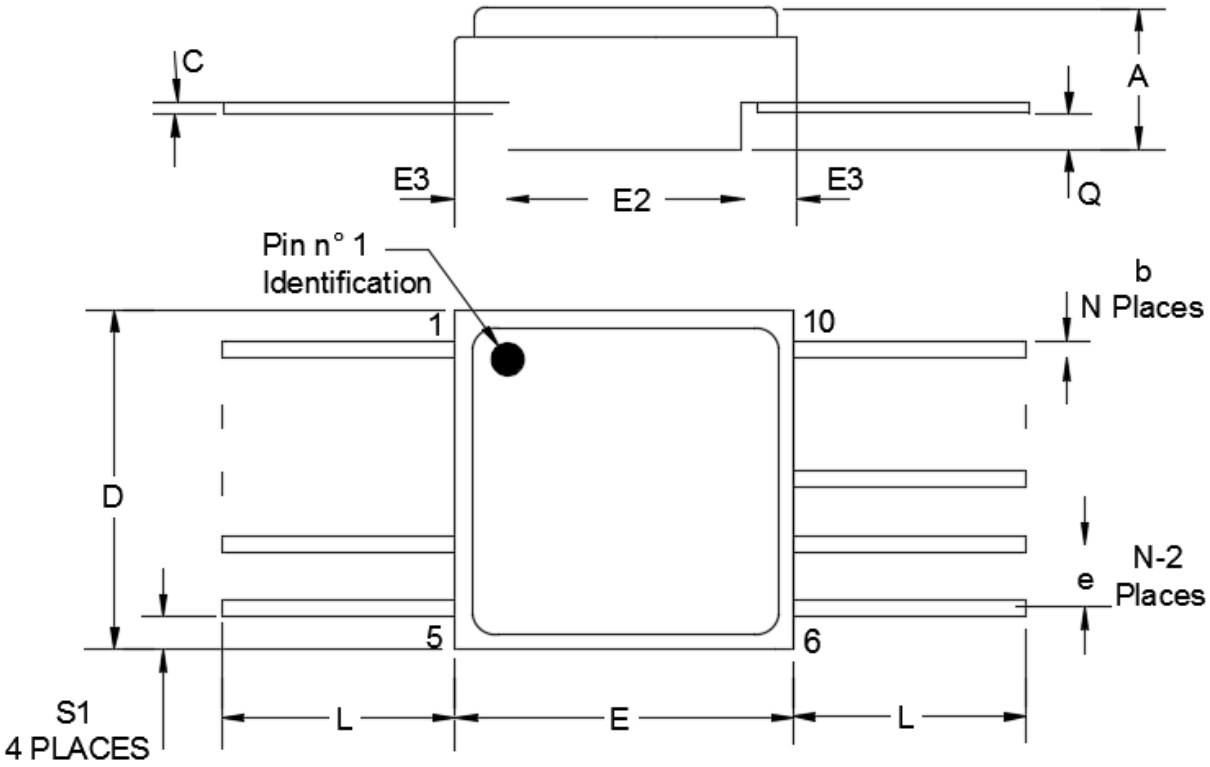


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99511
		REVISION LEVEL E	SHEET 12

DSCC FORM 2234
APR 97

Symbol	Dimensions					
	Inches			Millimeters		
	Minimum	Medium	Maximum	Minimum	Medium	Maximum
A	.089	.096	.103	2.26	2.44	2.62
b	.015	.017	.019	0.38	0.43	0.48
c	.004	.005	.006	0.102	0.127	0.152
D	.250	.255	.260	6.35	6.48	6.60
E	.250	.255	.260	6.35	6.48	6.60
E2	.170	.175	.180	4.32	4.45	4.58
E3	.035	.040	.045	0.88	1.01	1.14
e	.050 BSC			1.27 BSC		
L	.250	---	.370	6.35	---	9.40
Q	.026	.031	.036	0.66	0.79	0.92
S1	.006	.019	.032	0.16	0.485	0.81
N	10			10		

NOTES:
1. The US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch pounds units, the inch pound units shall take precedence
2. N is the maximum number of terminals positions.

FIGURE 1. Case outline - continued.

Device types	01, 02, 03, and 04	05	05
Case outline	X	Y	Z
Terminal number	Terminal symbol		
1	NC	NC	PWM_1
2	INPUT A	PWM_1	SGND
3	NC	NC	PGND
4	GND	SGND	CONNECTED TO THE SEAL RING
5	GND	PGND	PWM_2
6	NC	NC	OUTL_2
7	INPUT B	PWM_2	OUTH_2
8	NC	NC	V_S
9	NC	NC	OUTH_1
10	$\overline{\text{OUTPUT B}}$	OUTL_2	OUTL_1
11	$\overline{\text{OUTPUT B}}$	OUTH_2	---
12	V_S	V_S	---
13	V_S	V_S	---
14	$\overline{\text{OUTPUT A}}$	OUTH_1	---
15	$\overline{\text{OUTPUT A}}$	OUTL_1	---
16	NC	NC	---

FIGURE 2. Terminal connections.

Device types 01, 02, 03, 04

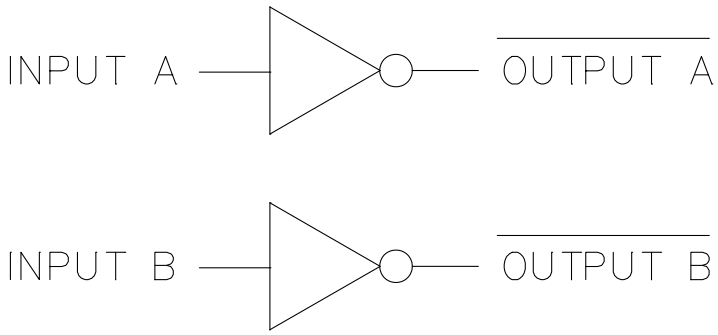


FIGURE 3. Logic diagram.

Device type 05

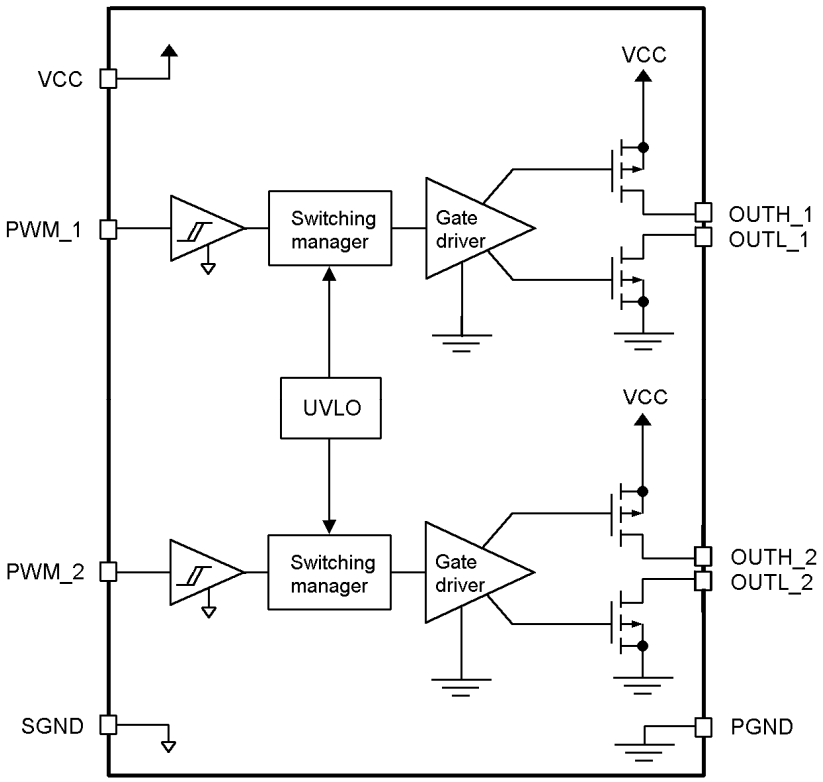


FIGURE 4. Block diagram.

Device types 01, 02, 03, 04		Device type 05 SEE NOTE	
INPUT A	$\overline{\text{OUTPUT A}}$	PWM_1	OUTH_1 = OUTL_1
1	0	0	1
0	1	1	0
INPUT B	$\overline{\text{OUTPUT B}}$	PWM_2	OUTH_2 = OUTL_2
1	0	0	1
0	1	1	0

NOTE: For device type 05 only, OUTH_X shorted to OUTL_X.

FIGURE 5. Truth table.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,7	1,7	As specified in QM plan
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8A, 8B, 9, 10, 11 1/	1, 2, 3, 2/ 3/ 7, 8A, 8B, 9, 10, 11, Δ	As specified in QM plan
Group A test requirements (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	As specified in QM plan

1/ PDA applies to subgroup 1 and 7.
2/ PDA applies to subgroups 1, 7, and Δ's.
3/ Delta limits (see table IIB) shall be required and the delta values shall be computed with reference to the zero hour electrical parameters (see table IA).

TABLE IIB. Burn-in delta parameters T_A = +25°C

Parameters	Symbol	Device type	Min	Max	Units
Power supply current	I_{CCSB} low	01, 02, 03, 04		175	μA
	I_{CCSB} high	01, 02, 03, 04		175	μA
	ICC H and ICCL	05	-75	+75	μA
Input current	I_{IL}	01, 02, 03, 04		1	μA
	I_{IH}	01, 02, 03, 04		1	μA
Source resistance	RHI	05	-100	+100	mΩ
Sink resistance	RLO	05	-100	+100	mΩ

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, 03, 04 and 05. In addition, for device types 03, 04, and 05 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.2.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5 krad(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 or JESD51-7 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for the latchup measurements.

g. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA test condition of SEP.

b. Occurrence of latch-up (SEL).

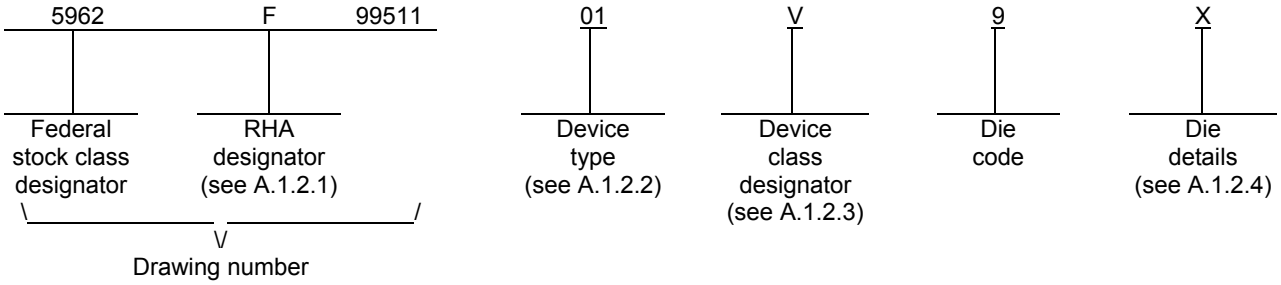
c. Number of transients (SET).

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99511

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS-4423RH	Radiation hardened MOSFET driver with < 10 V lockout voltage
02	HS-4423BRH	Radiation hardened MOSFET driver with < 7.5 V lockout voltage
03	HS-4423EH	Radiation hardened MOSFET driver with < 10 V lockout voltage
04	HS-4423BEH	Radiation hardened MOSFET driver with < 7.5 V lockout voltage
05	RH-PM4423	Radiation hardened 4.5 A dual inverting low side MOSFET driver

A.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-1
03	A-1
04	A-1
05	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-1
03	A-1
04	A-1
05	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-1
03	A-1
04	A-1
05	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-1
03	A-1
04	A-1
05	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99511

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1 and A-2.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1 and A-2.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1 and A-2.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and figures A-1 and A-2.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.5 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, 4.4.4.2.1, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

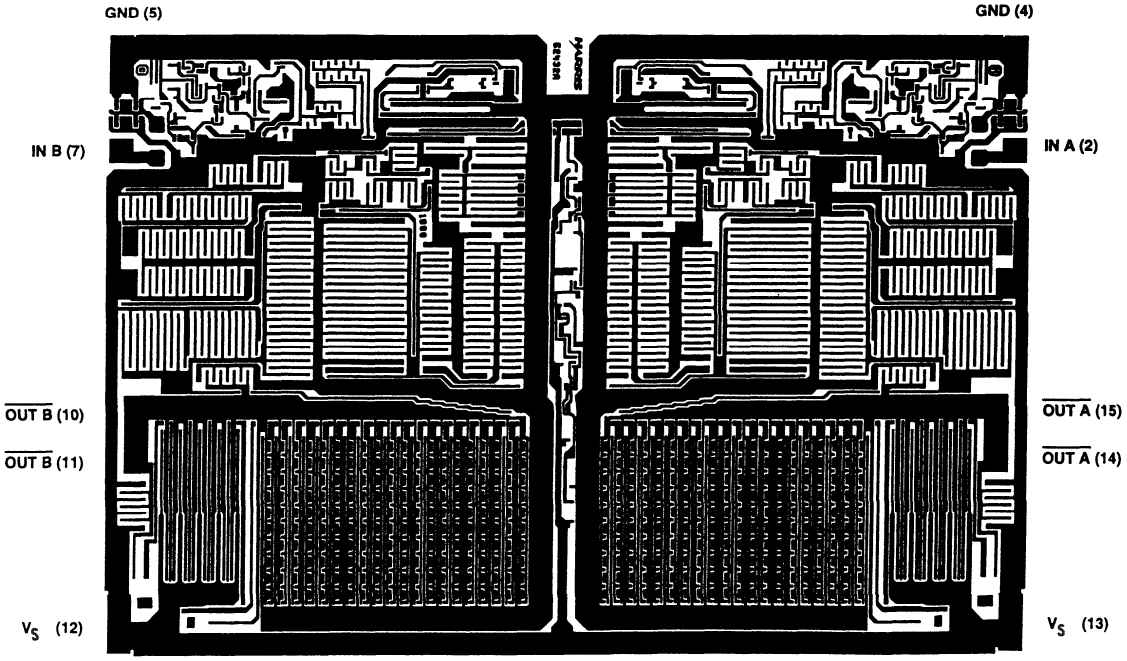
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99511

Device types 01, 02, 03, and 04



Die bonding pad locations and electrical functions

NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

Die physical dimensions.
Die size: 3370 microns x 4890 microns
Die thickness: 19 mils ± 1 mils

Interface materials.
Top metallization: Al Si Cu 16.0 kÅ ±2 kÅ
Backside metallization: None.

Glassivation.
Type: PSG
Thickness: 8.0 kÅ ±1.0 kÅ

Substrate: RSG: Single-poly dielectrically isolated BiCMOS

Assembly related information.
Substrate potential: Unbiased.
Special assembly instructions: None.

FIGURE A-1. Die bonding pad locations and electrical functions.

Device type 05

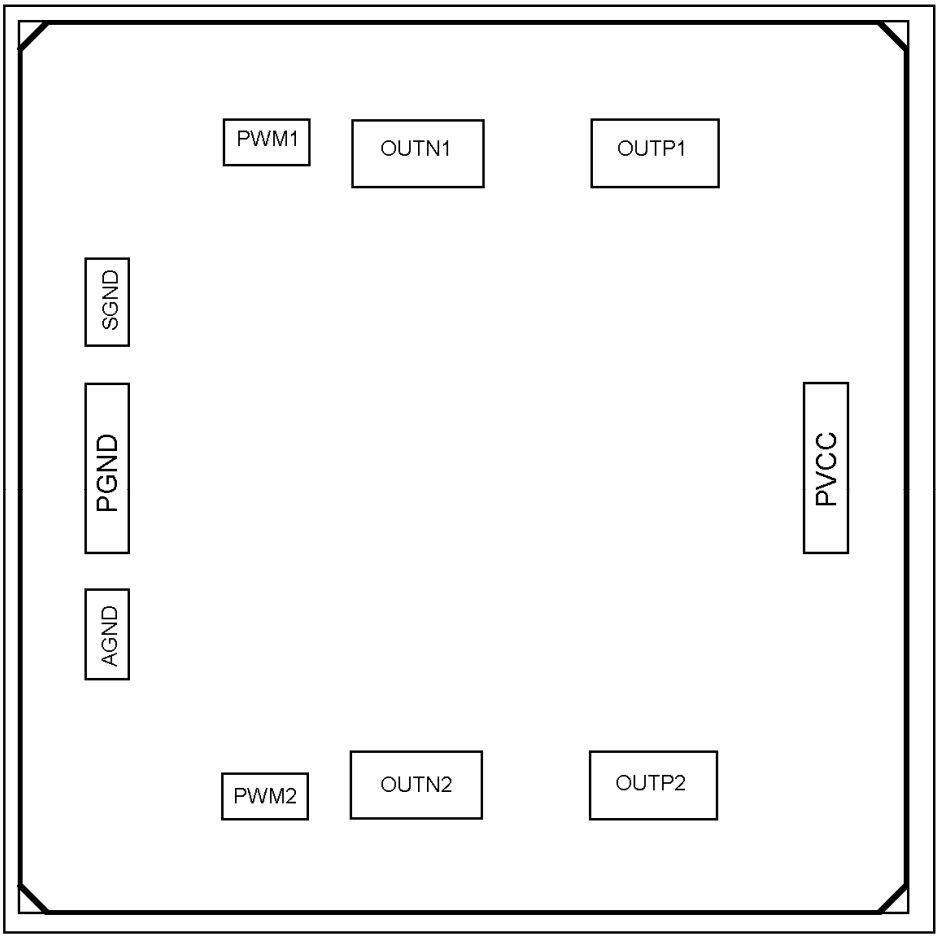


FIGURE A-2. Die bonding pad locations and electrical functions.

Pad size	
PGND = PVCC	360 μm x 90 μm
OUT_A = OUT_B	270 μm x 138 μm
PWM 1 = PWM2 = AGND = SGND	180 μm x 90 μm

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 78 mils x 78 mils
Die thickness: 375 μm (± 25 μm) or 15 mil (±1 mil)

Interface materials.
Top metallization: Metal 1: Ti//AlCu/TiN = 0.425 μm (±0.0425 μm)
Metal 2: Ti//AlCu/TiN = 0.575 μm (±0.0575 μm)
Metal 3: Ti//AlCu/TiN = 0.905 μm (±0.0905 μm)
Metal 4: Ti//AlCu/TiN = 3.175 μm (±0.4725 μm)

Top passivation: TEOS = 500 nm (±50 nm)
SiN = 550 nm (±55 nm)
Polymide = 5000 nm (±1000 nm)

Backside metallization: bare silicon

Glassivation.
Type: See top passivation
Thickness: See top passivation

Substrate: Silicon

Special assembly instructions: AGND bonded with PGND

Pad layout coordinates					
Pad symbol	X center	Y center	Pad symbol	X center	Y center
PGND	-815.7	+0.3	PVCC	+825.45	+0.3
SGND	-815.7	+380	OUTP2	+435.525	-725.05
PWM1	-455.95	+751.725	OUTN2	-110.6	-725.05
OUTN1	-110.6	+725.65	PWM2	-455.95	-751.725
OUTP1	+431.525	+725.65	AGND	-815.7	-379.4

NOTES:
1. Units are in μm.
2. AGND bonded with PGND.

FIGURE A-2. Die bonding pad locations and electrical functions - continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-03-23

Approved sources of supply for SMD 5962-99511 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962F9951101QXC	34371	HS9-4423RH-8
5962F9951101VXC	34371	HS9-4423RH-Q
5962F9951101V9A	34371	HS0-4423RH-Q
5962F9951102QXC	34371	HS9-4423BRH-8
5962F9951102VXC	34371	HS9-4423BRH-Q
5962F9951102V9A	34371	HS0-4423BRH-Q
5962R9951101TXC	3/	HS9-4423RH-T
5962R0051102TXC	3/	HS9-4423BRH-T
5962F9951103VXC	34371	HS9-4423EH-Q
5962F9951103V9A	34371	HS0-4423EH-Q
5962F9951104VXC	34371	HS9-4423BEH-Q
5962F9951104V9A	34371	HS0-4423BEH-Q
5962R9951105VYC	F8859	RHRPM4423K01V
5962R9951105VYA	F8859	RHRPM4423K02V
5962R9951105VZC	F8859	RHRPM4423LK01V
5962R9951105VZA	F8859	RHRPM4423LK02V
5962R9951105V9A	F8859	RHRPM4423D2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34371	Intersil Corporation 1650 Robert J. Conlan Blvd. NE Palm Bay, FL 32905-3406
F8859	ST Microelectronics 3 rue de Suisse CS 60816 35208 RENNES cedex2-FRANCE