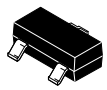
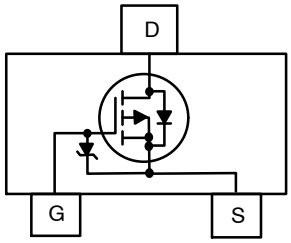
# Digital FET, P-Channel

## -25 V, -0.12 A, 10 Ω

# FDV302P



SOT−23−3
CASE 318−08



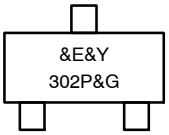

### General Description

This P−Channel logic level enhancement mode field effect transistor is produced using our proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on−state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, this one P−channel FET can replace several digital transistors with different bias resistors such as the DTCx and DCDx series.

### Features

- −25 V, −0.12 A Continuous, −0.5 A Peak
  - $R_{DS(on)}$ = 13 Ω @ $V_{GS}$ = −2.7 V
  - $R_{DS(on)}$ = 10 Ω @ $V_{GS}$ = −4.5 V
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits. $V_{GS(th)}$ < 1.5 V
- Gate−Source Zener for ESD Ruggedness. > 6 kV Human Body Model
- Compact Industry Standard SOT−23 Surface Mount Package
- Replace Many PNP Digital Transistors (DTCx and DCDx) with One DMOS FET
- This Device is Pb−Free and Halide Free

### MARKING DIAGRAM




| | |
|---|---|
| &E | = Designates Space |
| &Y | = Binary Calendar Year Coding Scheme |
| 302P | = Specific Device Code |
| &G | = Date Code |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDV302P | SOT−23−3 (Pb−Free, Halide−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

### ABSOLUTE MAXIMUM RATINGS $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | −25 | V |
| $V_{GSS}$ | Gate−Source Voltage | −8 | V |
| $I_D$ | Drain Current − Continuous | −0.12 | A |
| | Drain Current − Pulsed | −0.5 | |
| $P_D$ | Maximum Power Dissipation | 0.35 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | −55 to 150 | °C |
| ESD | Electrostatic Discharge Rating MIL−STD−883D Human Body Model (100 pF/1500 Ω) | 6.0 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient | 357 | °C/W |

**ELECTRICAL CHARACTERISTICS** $T_A$ = 25°C unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 μA | –25 | – | – | V |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | $I_D$ = –250 μA, Referenced to 25°C | – | –20 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –20 V, $V_{GS}$ = 0 V | – | – | –1 | μA |
| | | $V_{DS}$ = –20 V, $V_{GS}$ = 0 V, $T_J$ = 55°C | – | – | –10 | |
| $I_{GSS}$ | Gate – Body Leakage Current | $V_{GS}$ = –8 V, $V_{DS}$ = 0 V | – | – | –100 | nA |
| **ON CHARACTERISTICS** (Note 1) | | | | | | |
| $\Delta V_{GS(th)}/\Delta T_J$ | Gate Threshold Voltage Temp. Coefficient | $I_D$ = –250 μA, Referenced to 25°C | – | 1.9 | – | mV/°C |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | –0.65 | –1 | –1.5 | V |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –2.7 V, $I_D$ = –0.05 A | – | 10.6 | 13 | Ω |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –0.2 A | – | 7.9 | 10 | |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –0.2 A, $T_J$ = 125°C | – | 12 | 18 | |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –2.7 V, $V_{DS}$ = –5 V | –0.05 | – | – | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –0.2 A | – | 0.135 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 11 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 7 | – | |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 1.4 | – | |
| **SWITCHING CHARACTERISTICS** (Note 1) | | | | | | |
| $t_{D(on)}$ | Turn–On Delay Time | $V_{DD}$ = –6 V, $I_D$ = –0.2 A, $V_{GS}$ = –4.5 V, $R_{GEN}$ = 50 Ω | – | 5 | 12 | ns |
| $t_r$ | Turn–On Rise Time | | – | 8 | 16 | |
| $t_{D(off)}$ | Turn–Off Delay Time | | – | 9 | 18 | |
| $t_f$ | Turn–Off Fall Time | | – | 5 | 10 | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –5 V, $I_D$ = –0.2 A, $V_{GS}$ = –4.5 V | – | 0.22 | 0.31 | nC |
| $Q_{gs}$ | Gate–Source Charge | | – | 0.11 | – | |
| $Q_{gd}$ | Gate–Drain Charge | | – | 0.04 | – | |
| **DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | – | – | –0.2 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –0.2 A (Note 1) | – | –1 | –1.5 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL CHARACTERISTICS

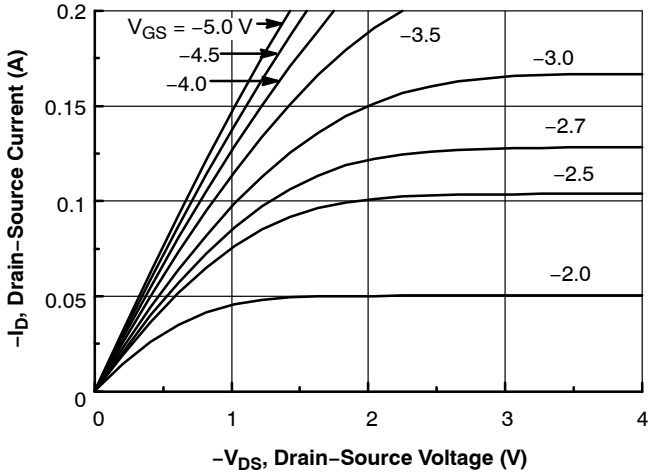



**Figure 1. On−Region Characteristics**

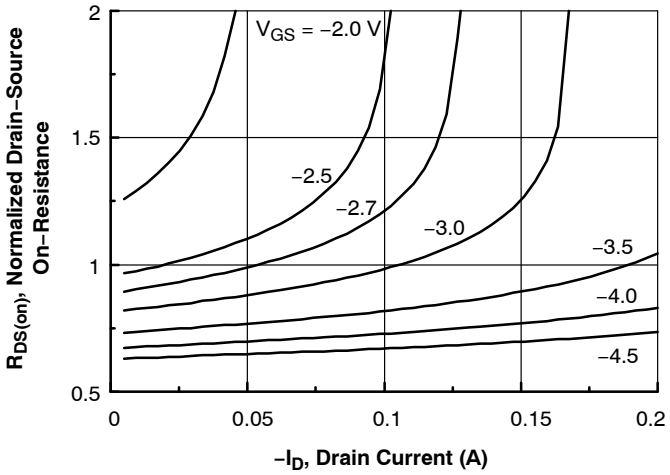



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

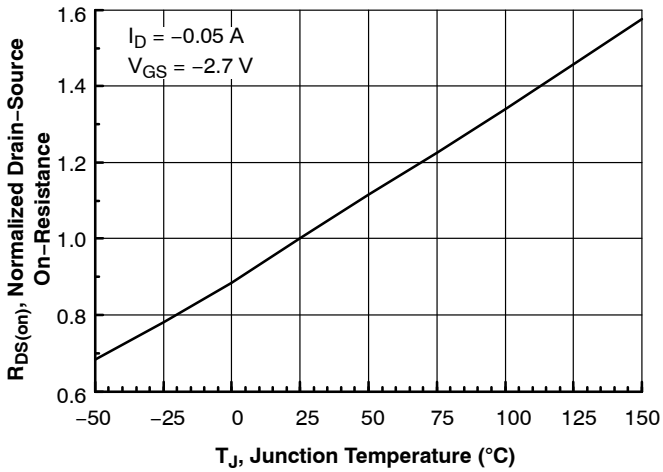



**Figure 3. On−Resistance Variation with Temperature**

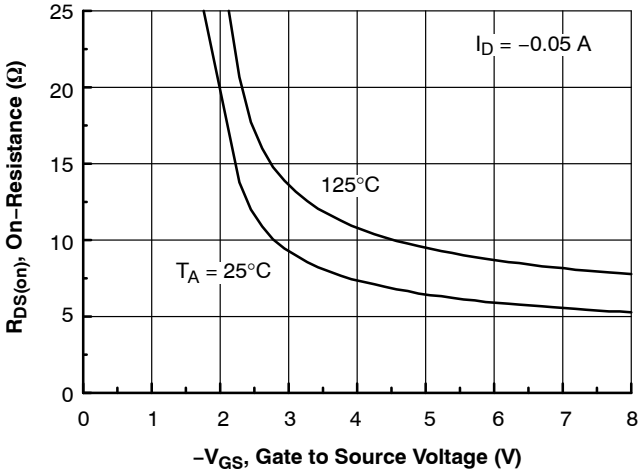



**Figure 4. On Resistance Variation with Gate−To−Source Voltage**

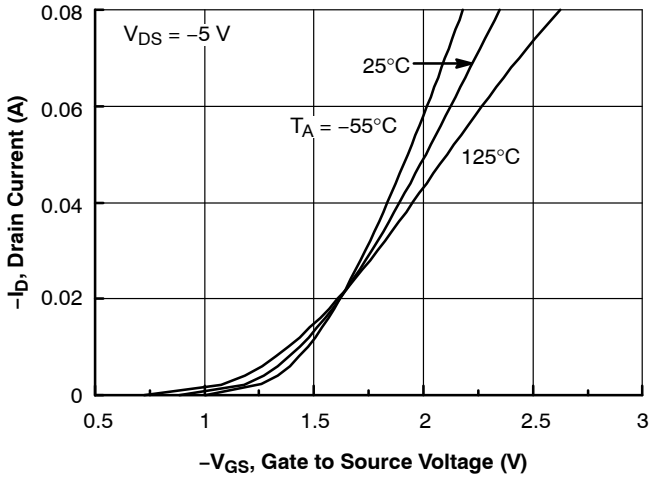



**Figure 5. Transfer Characteristics**

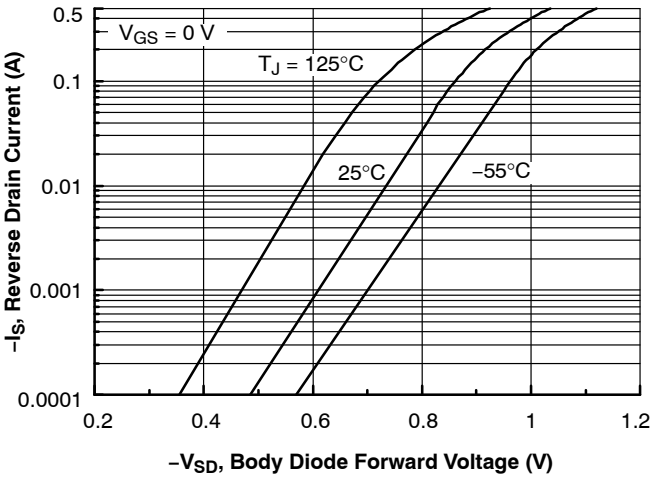



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## TYPICAL CHARACTERISTICS (continued)

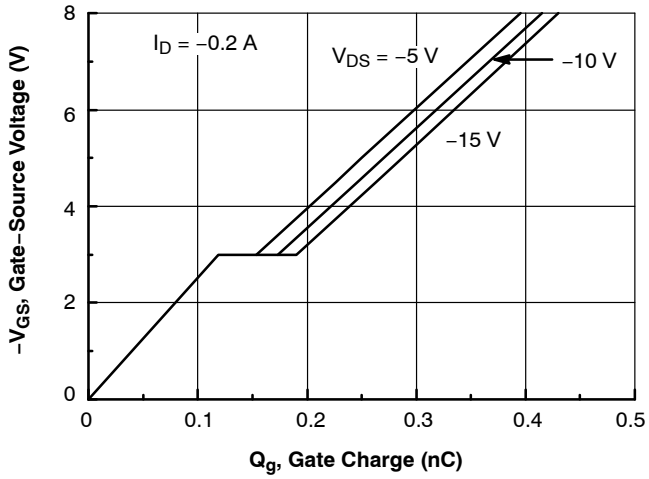



Figure 7. Gate Charge Characteristics

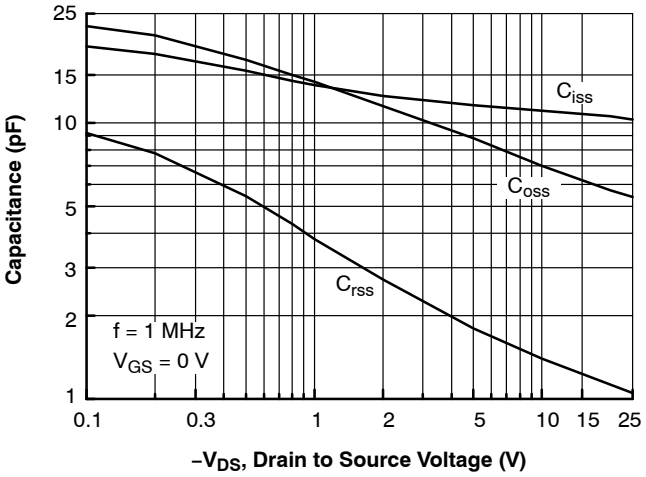



Figure 8. Capacitance Characteristics

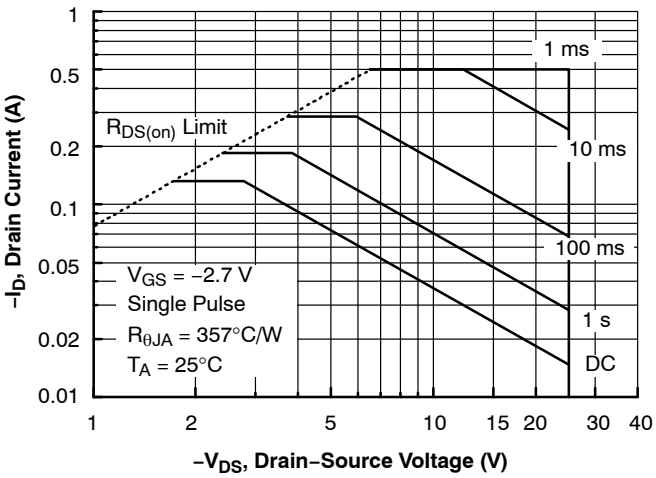



Figure 9. Maximum Safe Operating Area

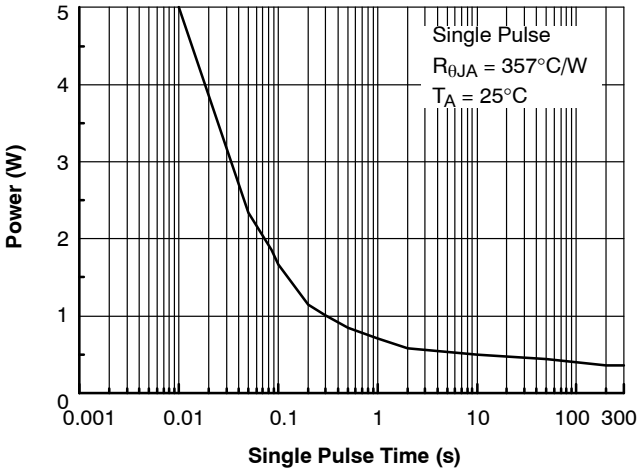



Figure 10. Single Pulse Maximum Power Dissipation

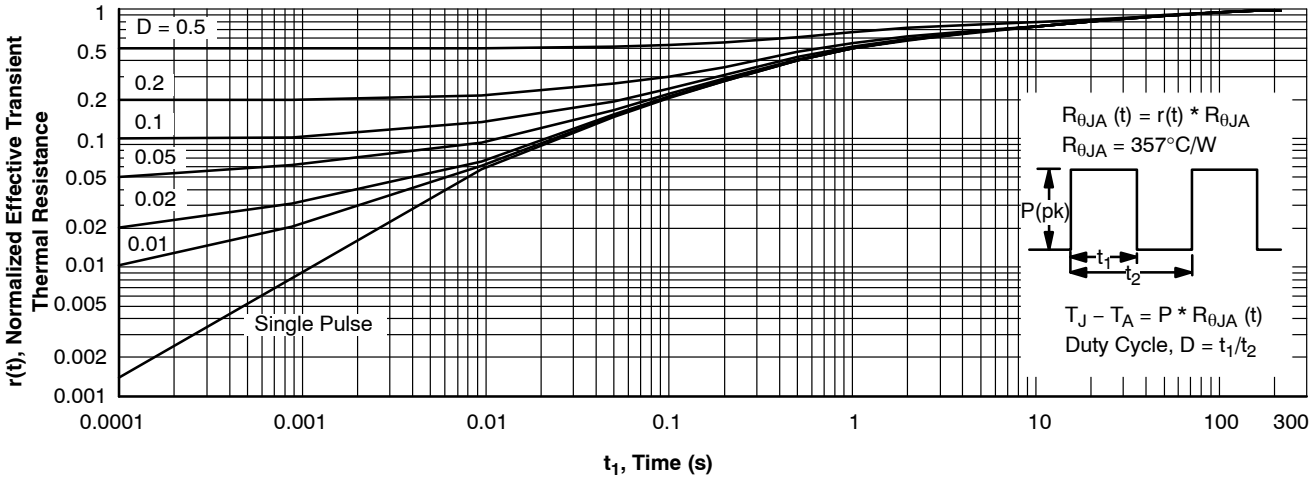


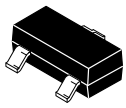

Figure 11. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

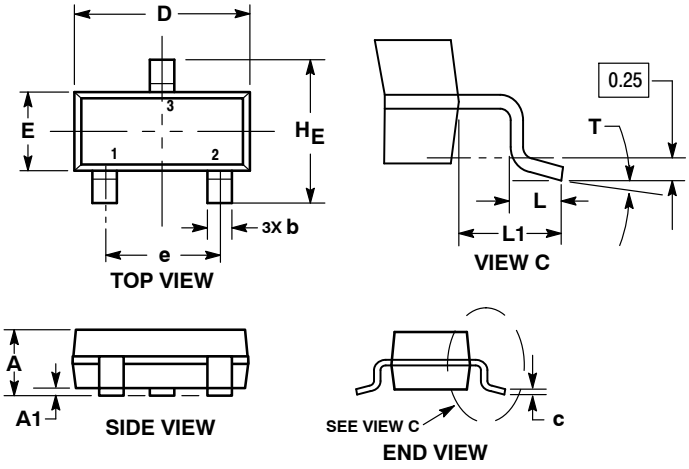
ON Semiconductor®

**SOT−23 (TO−236)**
CASE 318−08
ISSUE AS

DATE 30 JAN 2018



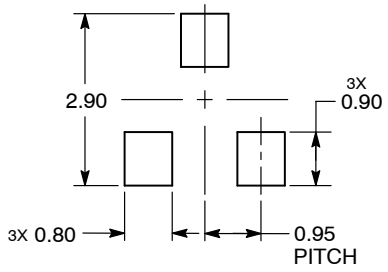
SCALE 4:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

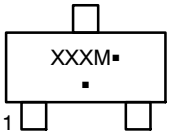
| | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| DIM | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.89 | 1.00 | 1.11 | 0.035 | 0.039 | 0.044 |
| A1 | 0.01 | 0.06 | 0.10 | 0.000 | 0.002 | 0.004 |
| b | 0.37 | 0.44 | 0.50 | 0.015 | 0.017 | 0.020 |
| c | 0.08 | 0.14 | 0.20 | 0.003 | 0.006 | 0.008 |
| D | 2.80 | 2.90 | 3.04 | 0.110 | 0.114 | 0.120 |
| E | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| e | 1.78 | 1.90 | 2.04 | 0.070 | 0.075 | 0.080 |
| L | 0.30 | 0.43 | 0.55 | 0.012 | 0.017 | 0.022 |
| L1 | 0.35 | 0.54 | 0.69 | 0.014 | 0.021 | 0.027 |
| $H_E$ | 2.10 | 2.40 | 2.64 | 0.083 | 0.094 | 0.104 |
| T | 0° | −−− | 10° | 0° | −−− | 10° |

### RECOMMENDED SOLDERING FOOTPRINT




DIMENSIONS: MILLIMETERS

### GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOT−23 (TO−236)** | **PAGE 1 OF 1** |

## PUBLICATION ORDERING INFORMATION

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**Email Requests to:** orderlit@onsemi.com

**onsemi Website:** www.onsemi.com

**TECHNICAL SUPPORT**
**North American Technical Support:**
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

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