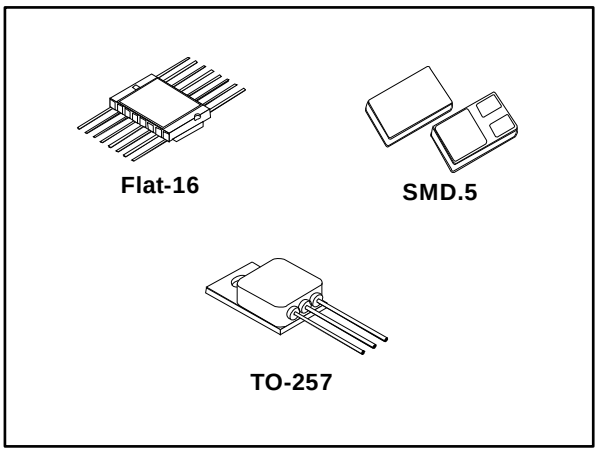
RHFL4913

1.5 V rad-hard positive fixed voltage regulator

Datasheet - preliminary data



Features

- Fixed 1.5 V output voltage
- Output current up to 3 A in SMD.5 and TO-257 packages, 2 A in Flat-16 package
- Embedded overtemperature, overcurrent protections
- Adjustable current limitation
- Output overload monitoring/signaling
- Inhibit (ON/OFF) TTL-compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Rad-hard: tested up to 300 krad MIL-STD-883E method 1019.6 and 100 krad low dose rate conditions
- SEL free up to 120 MeV·cm^2/mg
- SET < 5% of V_{OUT} at 86 MeV·cm^2/mg

Description

The device is a high performance radiation hardened LDO regulator, suitable for output current up to 3 A (TO-257 and SMD.5 versions). The operating input voltage range is from 3 V to 12 V. The device has been specifically designed for harsh radiation environments, such as aerospace applications.

Integrated overtemperature protection, adjustable overcurrent protection and monitoring offer a high level of robustness.

It is available in Flat-16, SMD.5 and TO-257 hermetic packages.

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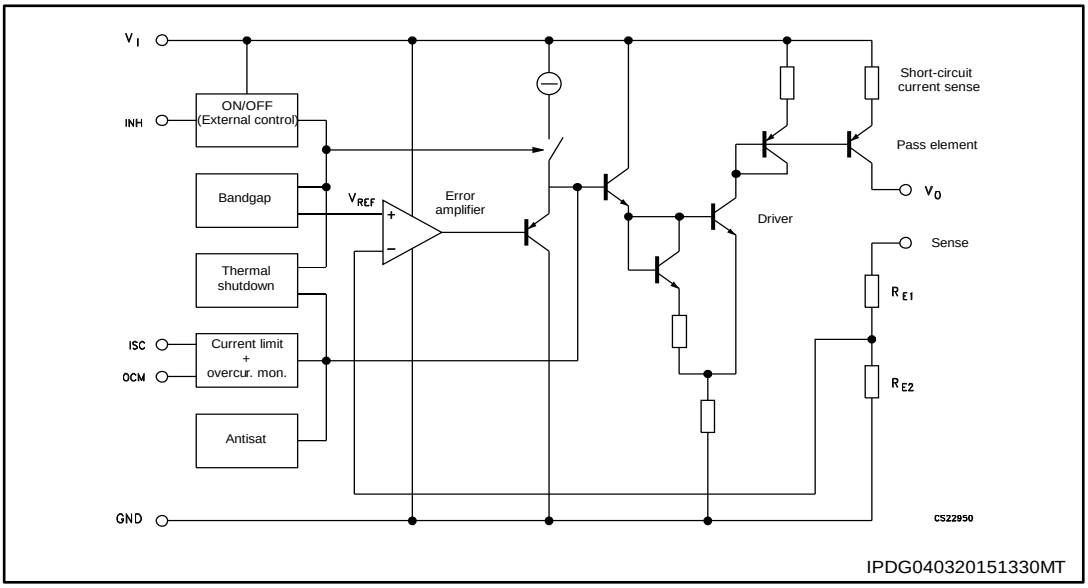
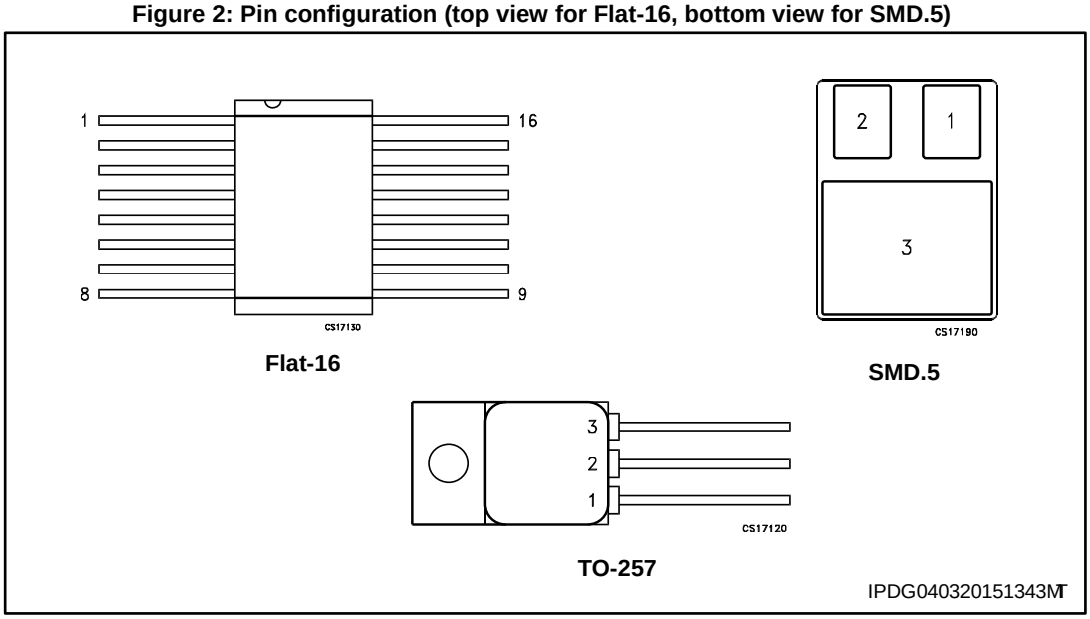
1 Diagram

Figure 1: Block diagram for Flat-16 package



2 Pin configuration

Figure 2: Pin configuration (top view for Flat-16, bottom view for SMD.5)



The upper metallic package lid, the bottom metallization on Flat-16 and the metal lid on SMD.5 are disconnected both from the regulator die and package terminals, hence electrically floating.

Table 1: Pin description

Pin name	Flat-16 (1)	SMD.5 (2)	TO-257	Description
V_O	1, 2, 6, 7 (3)	1	3	LDO output
V_I	3, 4, 5 (4)	2	1	LDO input
GND	13	3	2	Ground
I_{SC}	8	N.C.	N.C.	Short-circuit current adjustment pin: a resistor can be connected between this pin and V_I to set the current limit value
OCM	10	N.C.	N.C.	Overcurrent monitor flag (open drain)
INHIBIT	14	N.C.	N.C.	INHIBIT pin, TTL-compatible. The device is ON when INHIBIT pin is set to a low logic level. This pin is internally pulled down
SENSE	16	N.C.	N.C.	Output sense pin. This pin must be connected to V_O or to the load in case of remote sensing
NC	9, 11, 12, 15	N.C.	N.C.	Not internally connected (can be connected to GND)

Notes:

(1)The upper metallic package lid and the bottom metallization are disconnected both from the regulator die and package terminals, hence electrically floating.

(2)The upper metallic package lid is disconnected both from the regulator die and package terminals, hence electrically floating.

(3)All available output pins must be connected together to ensure stability and regulation.

(4)All available input pins must be connected together to ensure stability and regulation.

3 Maximum ratings

Table 2: Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_I	DC input voltage, V_I - V_{GND}		-0.3 to 14	V
V_O, V_{SENSE}	DC output voltage, output sense pin voltage vs. GND		-0.3 to (V_I + 0.3)	V
V_{INH}	INHIBIT pin voltage vs. GND		-0.3 to 14	V
V_{OCM}	Overcurrent monitor pin voltage vs. GND		-0.3 to 14	V
V_{ISC}	Current limit pin voltage vs. GND		-0.3 to 14	V
I_O	Output current	SMD.5 and TO-257 versions	3	A
		Flat-16 version	2	
P_D	T_C = 25 °C power dissipation	Flat-16 and SMD.5 versions	15	W
		TO-257 version	10	
T_{STG}	Storage temperature range		-65 to +150	°C
T_{OP}	Operating junction temperature range		-55 to +150	°C
T_J	Junction temperature (1)		+150	°C
ESD	Electrostatic discharge capability, HBM model		2	kV
	Electrostatic discharge capability, CDM model		500	V

Notes:

(1)Internally limited to maximum +175 °C by thermal shutdown circuit.

Exceeding maximum ratings may damage the device.

Table 3: Thermal data

Symbol	Parameter	Flat-16	TO-257	SMD.5	Unit
R_{thJC}	Thermal resistance junction-case max.	8.3	12.5	8.3	°C/W
T_{SOLD}	Maximum soldering temperature, 10 s	300			°C

4 Electrical characteristics

T_J = 25 °C, V_I = 3 V, V_o = 1.5 V, C_I = C_O = 1 µF tantalum, unless otherwise specified. Typical values are measured at 25 °C.

Table 4: Electrical characteristics

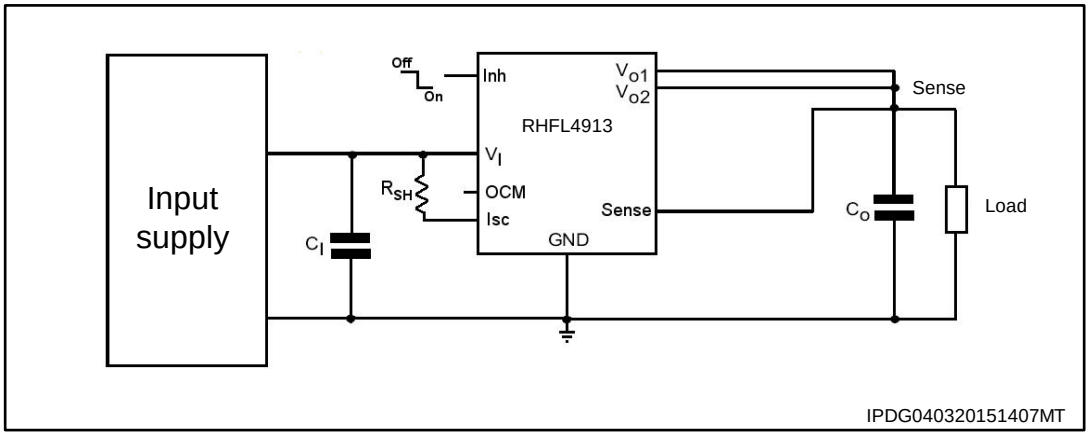
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_I	Operating input voltage	I_O = 5 mA -55 °C < T_J < + 125 °C	3		12	V
V_O	Output voltage accuracy	I_O = 5 mA	1.46		1.54	V
I_{SHORT}	Output current limit (1)	Adjustable by external resistor		4.5		A
$\Delta V_O/\Delta V_I$	Line regulation	V_I = 3 to 12 V, I_O = 5 mA, T_J =+25 °C		0.03	0.3	%
		V_I = 3 to 12 V, I_O = 5 mA, T_J = -55°C			0.4	
		V_I = 3 to 12 V, I_O = 5 mA, T_J = +125 °C			0.4	
$\Delta V_O/\Delta I_O$	Load regulation	I_O = 5 mA to 400 mA T_J = + 25 °C		0.1	0.4	%
		I_O = 5 mA to 400 mA -55 °C < T_J < +125 °C			0.4	
		I_O = 5 mA to 1 A T_J = + 25 °C		0.2	0.6	
		I_O = 5 mA to 1 A -55 °C < T_J < + 125 °C			0.6	
Z_{OUT}	Output impedance	I_O = 100 mA DC and 20 mA rms		100		mΩ
I_q	Quiescent current	I_O = 5 mA, on mode -55 °C < T_J < + 125 °C		1.8	6	mA
		I_O = 30 mA, on mode -55 °C < T_J < +125 °C		2.5	8	
		I_O = 30 mA, on mode T_J = +25 °C			5	
		I_O = 300 mA, on mode -55 °C < T_J < + 125 °C		8	30	
		I_O = 300 mA, on mode T_J = +25 °C			25	
		I_O = 1 A, on mode, T_J = -55 °C			100	
		I_O = 1 A, on mode, T_J = +25 °C		23	60	
		I_O = 1 A, on mode, T_J = +125 °C			40	
		V_I = V_O + 2 V, V_{INH} = 2.4 V off mode		0.2	0.6	
$V_{INH(ON)}$	Inhibit voltage	I_O = 5 mA -55 °C < T_J < + 125 °C			0.8	V

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$V_{INH(OFF)}$	Inhibit voltage	I_O = 5 mA -55 °C < T_J < + 125 °C		2.4			V
SVR	Supply voltage rejection (1)	$V_I = V_O$ + 2.5 V ± 1 V I_O = 5 mA	f = 120 Hz		70		dB
			f = 33 kHz		45		
I_{SH}	Shutdown input current	V_{INH} = 5 V			15		µA
V_{OCM}	OCM pin voltage	Sinked I_{OCM} = 24 mA active low			0.38		V
t_{PLH} t_{PHL}	Inhibit propagation delay (1)	$V_I = V_O$ + 2.5 V V_{INH} = 2.4 V I_O = 400 mA	on-off		15		µs
			off-on		2		µs
eN	Output noise voltage (1)	B = 10 Hz to 100 kHz I_O = 5 mA to 2 A			15		µVrms

Notes:

(1)This value is guaranteed by design. For each application it's strongly recommended to comply with the maximum current limit of the package used.

Figure 3: Typical application diagram



5 Radiation performance

5.1 Total ionizing dose (MIL-STD-883E test method 1019.6)

The products, which are guaranteed in radiation within RHA QML-V system, fully comply with the MIL-STD-883E test method 1019.6 specification. The RHFL4913 is being RHA QML-V qualified, tested and characterized in full compliance with the MIL-STD-883E specification, both below 10 mrad/s and between 50 and 300 rad/s.

- Testing is performed in accordance with MIL-PRF-38535 and MIL-STD-883E test method 1019.6 for total ionizing dose (TID)
- ELDRS characterization is performed in qualification on both biased and unbiased parts only, on a sample of ten units from two different wafer lots
- Each wafer lot is tested at high dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification

Table 5: TID test results

Type	Conditions	Value	Unit
TID	18 krad(Si)/h high dose rate up to	300	krad
	10 mrad(Si)/s low dose rate up to	100	
	ELDRS free up to	100	
Output voltage radiation drift	From 0 krad to 300 krad, MIL-STD-883E method 1019.6 - at 18 krad(Si)/h	8.9	ppm/krad
Quiescent current (on- state)	From 0 krad to 300 krad at 50 rad/s , MIL-STD-883E method 1019.6, V_I = 2.5 V to 12 V, I_O = 5 to 30 mA, T_J = -55 to + 125 °C	<12	mA

5.2 SEE (single event effect) results

Table 6: "Heavy ion test results" summarizes the results of heavy ion tests. The HI trials have been performed on the adjustable version, the RHFL4913A, to obtain the output voltage of 1.5 V. SEL and SET performance described here below is related to the circuit configuration and bias conditions shown in *Figure 4: "Heavy ion test configuration (RHFL4913A)"* and *Table 7: "Bias configuration"* and *Table 8: "Test configuration"*.

Table 6: Heavy ion test results

Type	Conditions	Value	Unit
Heavy ions (1)	SEL immunity up to	120	MeV·cm^2/mg
	SET < 5% of V_{OUT}, (2) V_{IN} < 3.3 V	86	

Notes:

(1)The behavior of the product submitted to heavy ions is not tested in production. Heavy ion trials are performed on qualification lots only. HI trials have been performed on the adjustable version, the RHFL4913A, to obtain 1.5 V output voltage.

(2)When V_{IN} > 3.3 V, guidelines on the external component reported in the application note AN2984 “Minimizing the SET-related effects on the output of a voltage linear regulator", can be helpful.

Implementation of the below configuration is recommended when the RHFL4913A supplies high input voltage sensitivity components, such as low voltage FPGA and ASICs. SET robustness can be furtherly improved by using the additional R-C network described in the AN2984 “Minimizing the SET-related effects on the output of a voltage linear regulator".

Figure 4: Heavy ion test configuration (RHFL4913A)

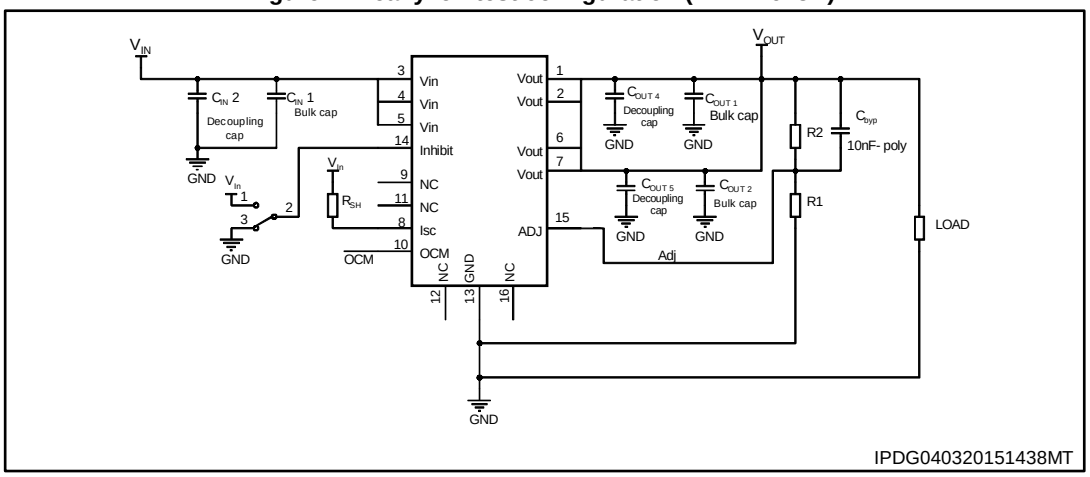


Table 7: Bias configuration

Test mode	Bias	Bias conditions
SEL	-	V_{IN} = 12 V, V_{OUT} = 9 V, (R1 = 1 kΩ, R2 = 6.2 kΩ), $V_{INHIBIT}$ = 0 V, I_{OUT} = 5 mA
SET	Bias 1	V_{IN} = 3 V, V_{OUT} =1.5 V (R1 = 1 kΩ, R2 = 200 Ω), $V_{INHIBIT}$ = 0 V, I_{OUT} = 1 A
	Bias 2	V_{IN} = 3 V, V_{OUT} = 0 V (R1 = 1 kΩ, R2 = 200 Ω), $V_{INHIBIT}$ = 5 V, I_{OUT} = 0 A
	Bias 3	V_{IN} = 3.3 V, V_{OUT} = 2.5 V, (R1 = 1 kΩ, R2 = 1 kΩ), $V_{INHIBIT}$ = 0 V, I_{OUT} = 0 to 1 A

Table 8: Test configuration

Test mode	Test configuration	
SET	Configuration 1	(47 µF+100 nF set of capacitors in each output port): - C_{IN1} = 100 µF tantalum, ESR < 30 mΩ - C_{OUT1} = C_{OUT2} = 47 µF tantalum, < 30 mΩ - C_{IN2} = C_{OUT4} = C_{OUT5} = 100 nF polyester (1) - C_{byp} = 10 nF polyester (1) - R_{isc} = 40 kΩ (to achieve 2 A current limit)
	Configuration 2	- C_{IN1} = C_{OUT1} = 220 µF tantalum, E_{SR} < 30 mΩ - C_{OUT2} = not connected - C_{IN2}= C_{OUT4} = 100 nF polyester (1) - C_{OUT5} = not connected - C_{byp} = 10 nF polyester (1) - R_{isc} = 40 kΩ (to achieve 2 A current limit)
SEL	SEL configuration	- C_{IN1} = 100 µF tantalum, E_{SR} < 30 mΩ - C_{OUT1} = C_{OUT2} = 47 µF tantalum, E_{SR} < 30 mΩ - C_{IN2} = C_{OUT4} = C_{OUT5} = 100 nF polyester (1) - C_{byp} = 10 nF polyester (1) - R_{isc} = 40 kΩ (2 A current limit)

Notes:

(1)Order code: CDR04BX104AKWS, manufactured by AVX.

5.3 Guidelines for SET mitigation

This section provides a detailed description of possible solutions, which protect the load against the SET. In this respect, there are two main areas of intervention: ground connection and external component selection.

5.3.1 Ground connections

To achieve the best performance of output voltage accuracy, noise immunity and robustness against single event effects, a proper PCB layout has to be developed, by following below indications.

According to qualitative simulations of single event, some very short SET (i.e. those having duration within 100 ns range) are strongly dependent on the stray inductances versus GND. The best solution to reduce the parasitic inductance is the adoption of a GND plane (with separate power and sense paths where possible). By minimizing the stray GND impedance, a better control of the SET amplitude (near to the load) can be achieved.

If this solution is not applicable, a star-bus topology could be used, where the PCB reference GND connection is close to the GND pin of the regulator.

To achieve a good GND sense, the following rules have to be met:

- The regulator GND pin and load GND node have to be connected to the sense and power GND traces on the PCB , using vias to minimize the path
- An array of multiple via structures works better if compared to a single via
- GND connectors/plugs: separate plugs have to be used for power supply and testing probes
- Input/output capacitor GND terminals have to be connected to GND sense on PCB

5.3.2 Capacitor selection

Tantalum capacitors both for input and output, are a preferable choice.

With reference to *Figure 4: "Heavy ion test configuration (RHFL4913A)"*, on the input and output ports, a combination of capacitors has to be present. On the input terminals, 100 µF bulk capacitor (C_{IN1}) could be in parallel with a polyester 100 nF one ($C_{IN2,}$) used for decoupling purpose.

For each of the two output connections (pins 1, 2 and 6, 7) a combination of 47 µF bulk capacitor ($C_{OUT1,}$ $C_{OUT2,}$) in parallel with a polyester 100 nF ($C_{OUT4,}$ C_{OUT5}) has to be used for decoupling purpose.

Low-ESL capacitors have to be adopted for 100 nF elements.

Concerning the selection of three bulk capacitors:

- Use tantalum SMD
- Select size and ESL as small as possible
- Place capacitors as close as possible to the input/output terminals
- Use an array of capacitors in parallel, where possible. This works better than a single capacitor against short events

6 Typical performance characteristics

T_J = 25 °C, V_I = 3 V, I_O = 5 mA, C_I = C_O = 1 µF, unless otherwise specified.

Figure 5: Output voltage vs. temperature (V_{IN} = 3 V, I_{OUT} = 5 mA)

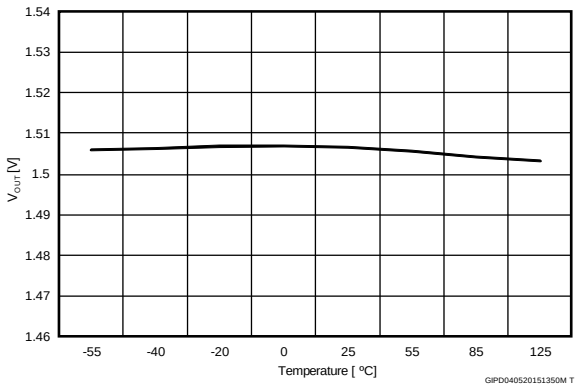


Figure 6: Output voltage vs. temperature (V_{IN} 12 V, I_{OUT} = 5 mA)

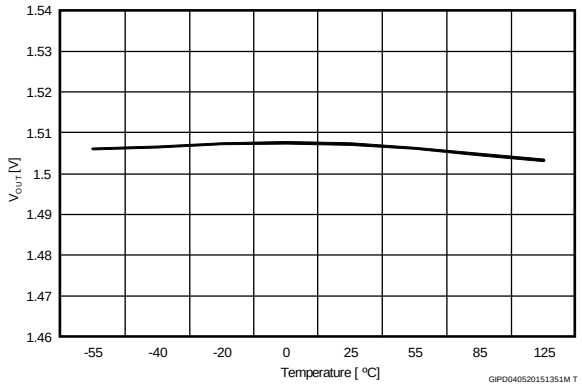


Figure 7: Output voltage vs. temperature (V_{IN} = 3 V, I_{OUT} = 400 mA)

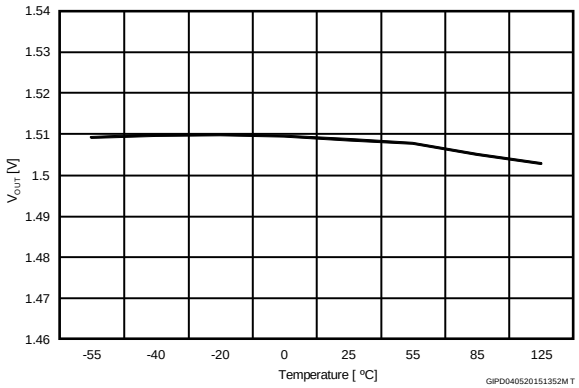


Figure 8: Output voltage vs. temperature (V_{IN} = 3 V, I_{OUT} = 1 A)

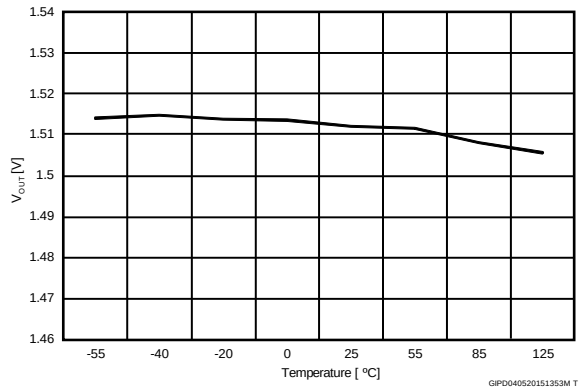


Figure 9: Output voltage vs. temperature (V_{IN} = 3 V, I_{OUT} = 2 A)

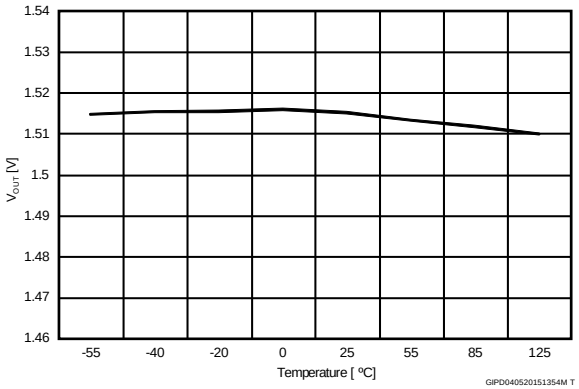


Figure 10: Output voltage vs. temperature (V_{IN} = 4 V, I_{OUT} = 3 A)

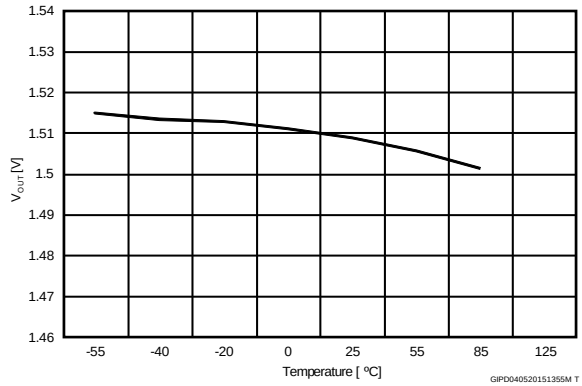


Figure 11: Minimum input voltage vs. temperature (I_{OUT} = 5 mA)

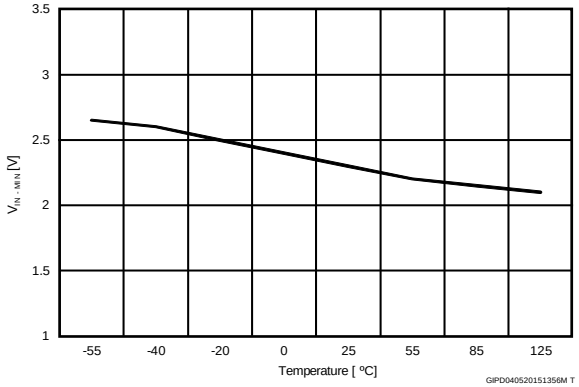


Figure 12: Line regulation vs. temperature (V_{IN} = 3 V to 12 V, I_{OUT} = 5 mA)

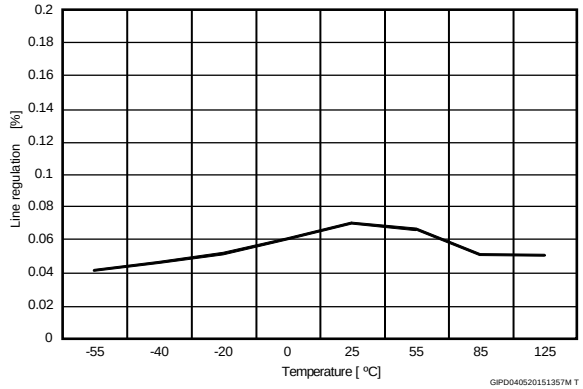


Figure 13: Load regulation vs. temperature (V_{IN} = 3 V, I_{OUT} = 5 mA to 400 mA)

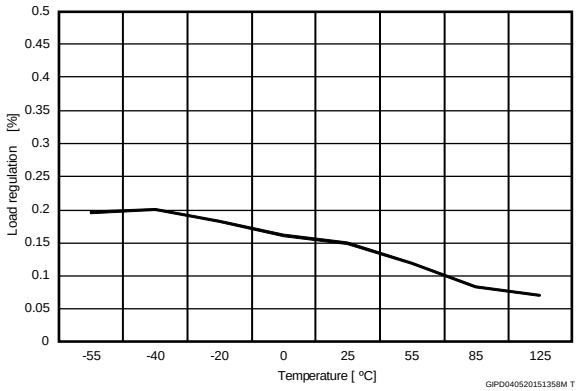


Figure 14: Load regulation vs. temperature (V_{IN} = 3 V, I_{OUT} = 5 mA to 1 A)

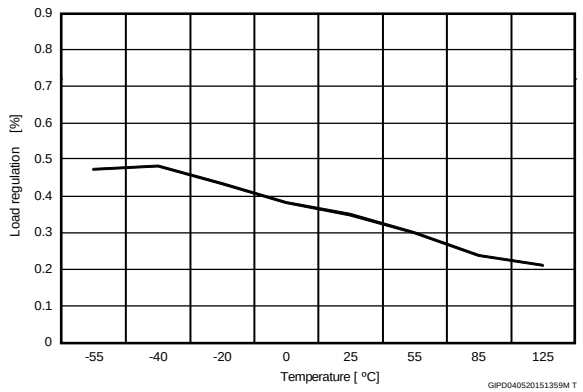


Figure 15: Load regulation vs. temperature (V_{IN} = 3 V, I_{OUT} = 5 mA to 2 A)

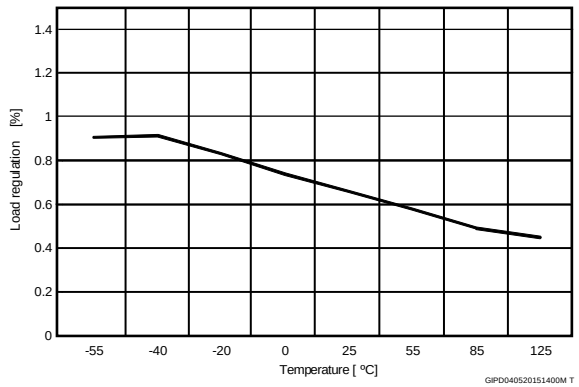


Figure 16: Quiescent current vs. temperature (V_{IN} = 3 V, I_{OUT} = 5 mA)

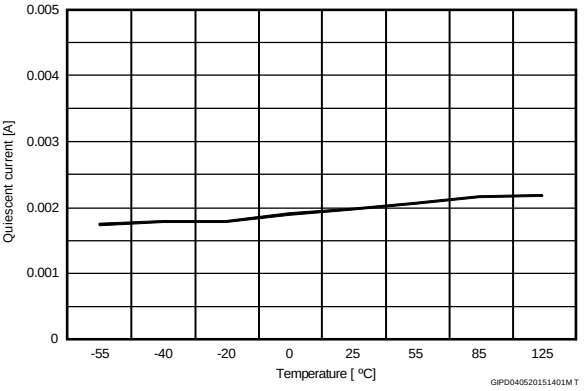


Figure 17: Quiescent current vs. temperature (V_{IN} = 3 V, I_{OUT} = 30 mA)

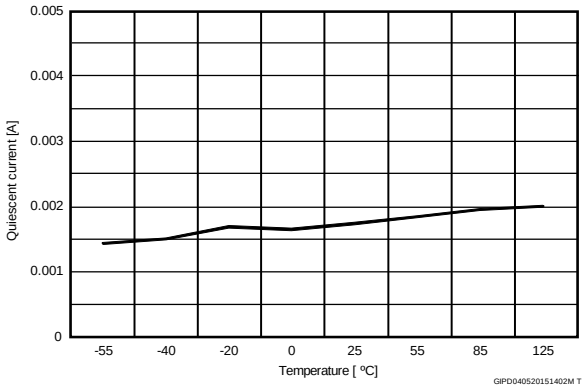


Figure 18: Quiescent current vs. temperature (V_{IN} = 3 V, I_{OUT} = 300 mA)

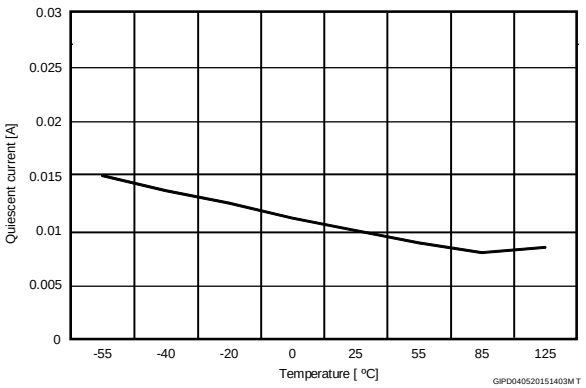


Figure 19: Quiescent current vs. temperature (V_{IN} = 3 V, I_{OUT} = 1 A)

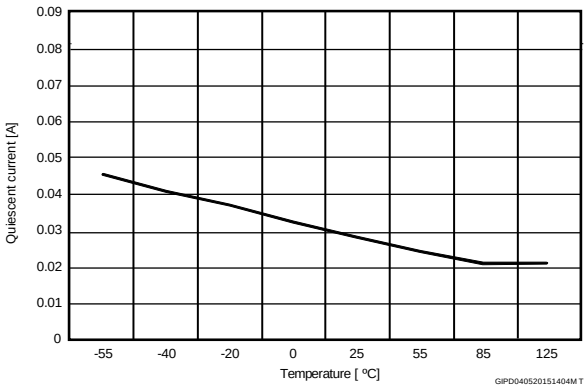


Figure 20: Quiescent current vs. temperature (V_{IN} = 3 V, I_{OUT} = 2 A)

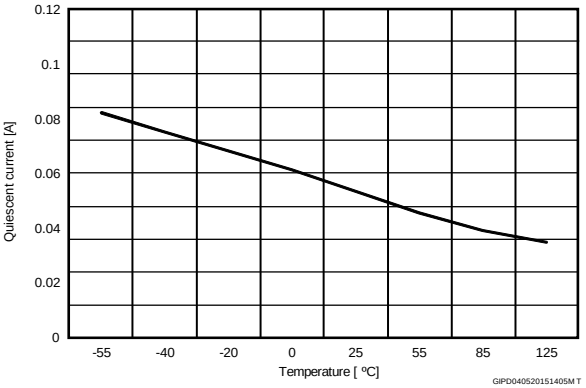


Figure 21: Quiescent current vs. temperature (V_{IN} = 3 V, I_{OUT} = 3 A)

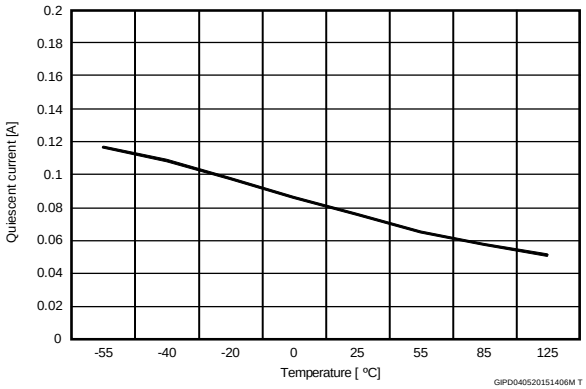


Figure 22: Off mode quiescent current vs. temperature (V_{IN} = 3.5 V, V_{INH} = 2.4 V)

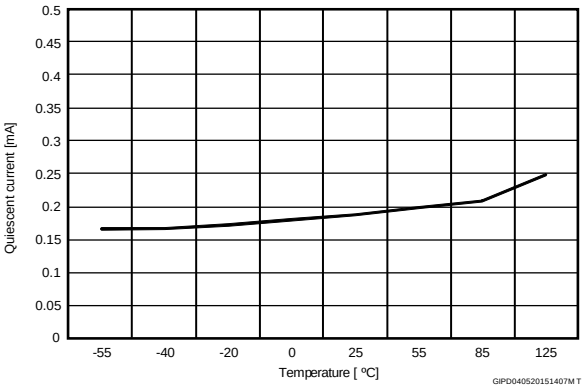


Figure 23: Inhibit on threshold vs. temperature

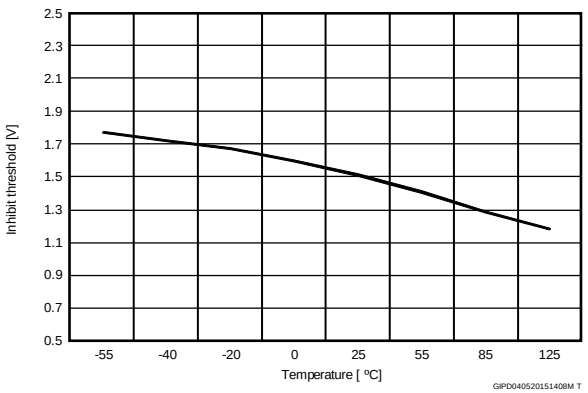


Figure 24: Inhibit off threshold vs. temperature

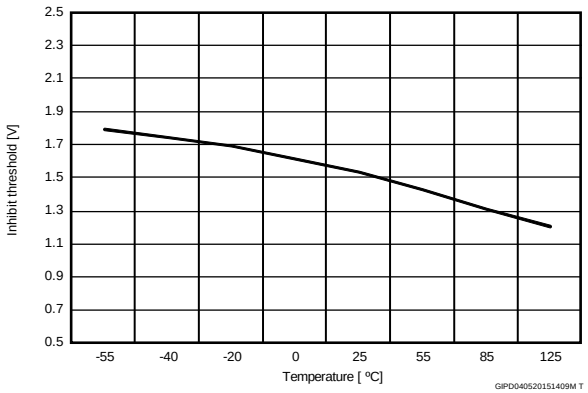


Figure 25: Startup with enable

V_{IN}=4V, V_{INH} from 2 to 0V, I_{OUT}=5mA, C_{IN}=C_{OUT}=1µF, T_{fall}=5µs

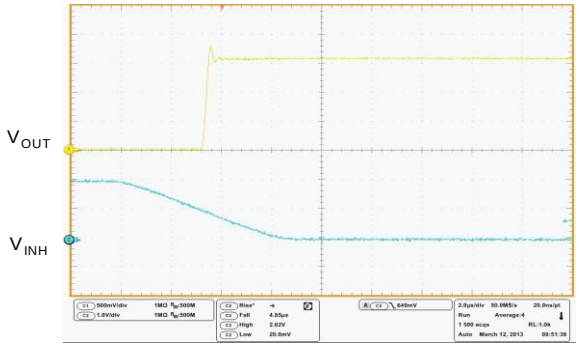


Figure 26: Turn-off with enable

V_{IN}=4V, V_{INH} from 0 to 2V, I_{OUT}=5mA, C_{IN}=C_{OUT}=1µF, T_{rise}=5µs

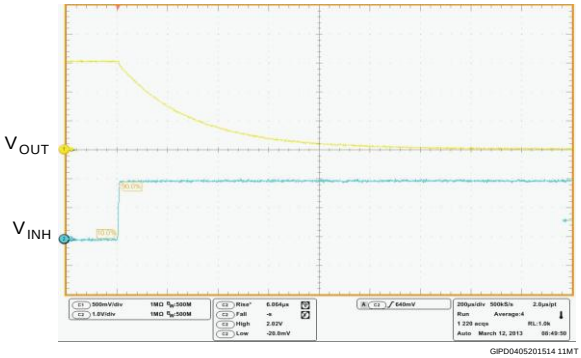


Figure 27: Turn-on time

V_{IN}=from 0 to 12V, V_{INH}=0V, I_{OUT}=5mA, C_{IN}= C_{OUT}=1µF

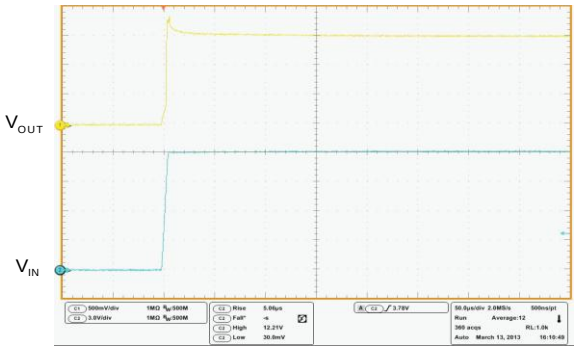


Figure 28: Turn-off time

V_{IN} =from 12 to 0V, V_{INH} =2V, I_{OUT} =5mA, C_{IN} = C_{OUT} =1µF

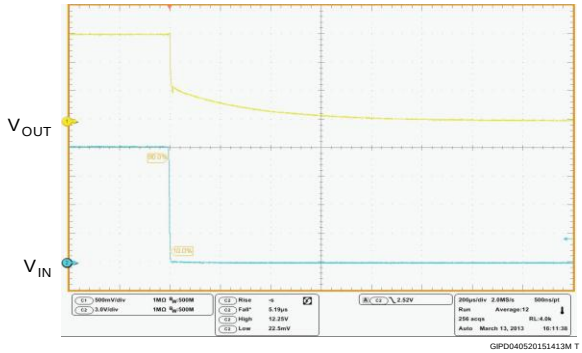


Figure 29: Line transient (V_{IN} from 4 V to 5 V)

I_{OUT} =10mA, C_{OUT} =1µF, T_{rise} =5µs

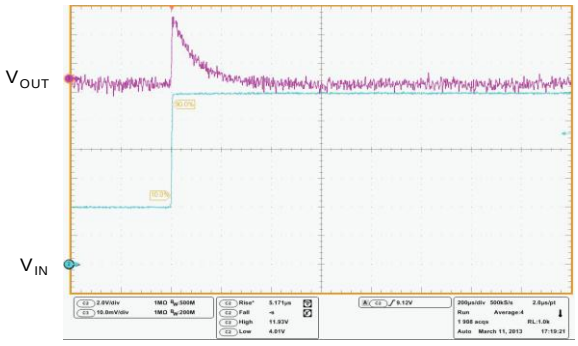


Figure 30: Line transient (V_{IN} from 5 V to 4 V)

I_{OUT} =10mA, C_{OUT} =1µF, T_{fall} =5µs

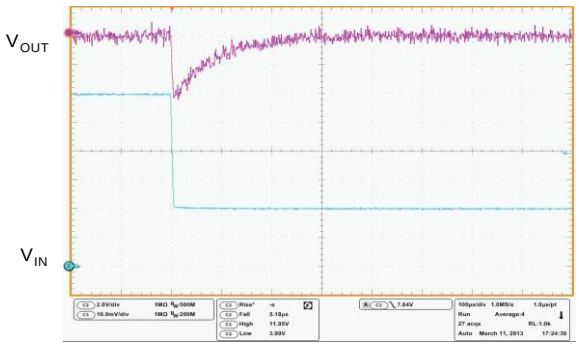


Figure 31: Load transient (I_{OUT} from 5 mA to 1 A)

V_{IN} =4V, C_{IN} = C_{OUT} =1µF, T_{rise} =5µs

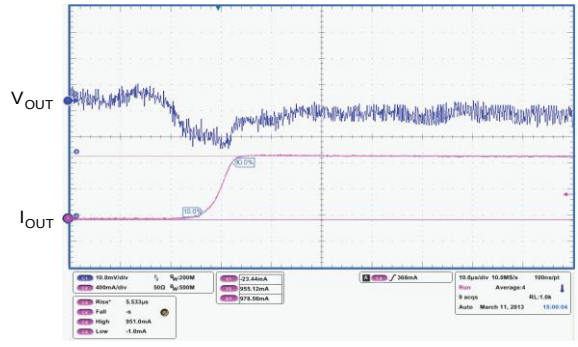


Figure 32: Load transient (I_{OUT} from 1 A to 5 mA)

V_{IN} =4V, C_{IN} = C_{OUT} =1µF, T_{fall} =5µs

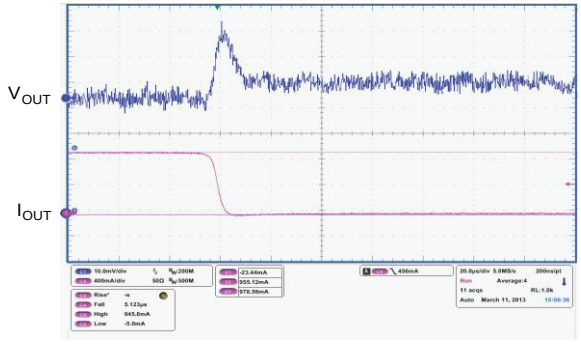


Figure 33: Short-circuit behavior (V_{IN} = 4 V)

C_{IN} =C_{OUT}=2.2µF

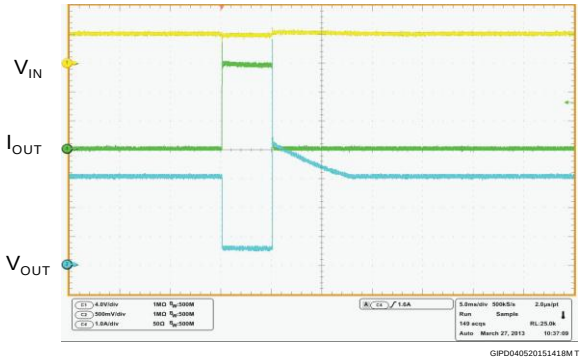


Figure 34: Short-circuit behavior (V_{IN} = 12 V)

C_{IN} =C_{OUT}=2.2µF

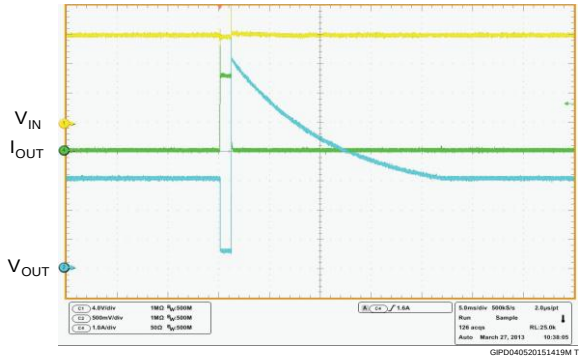


Figure 35: Short-circuit current vs. RSH

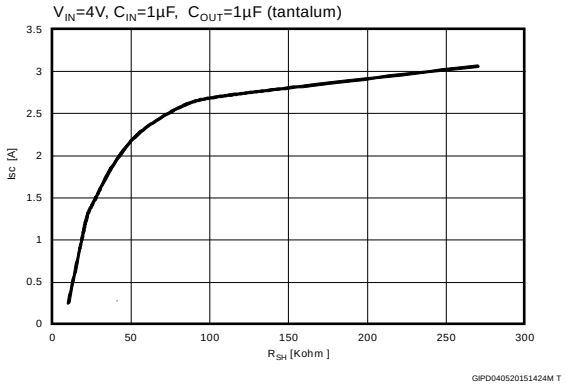


Figure 36: Short-circuit current vs. RSH (magnification)

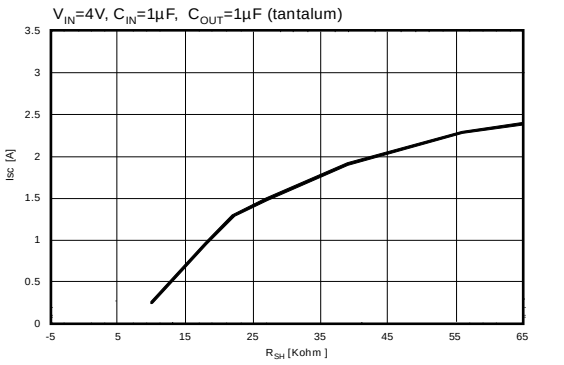


Figure 37: Noise spectral density

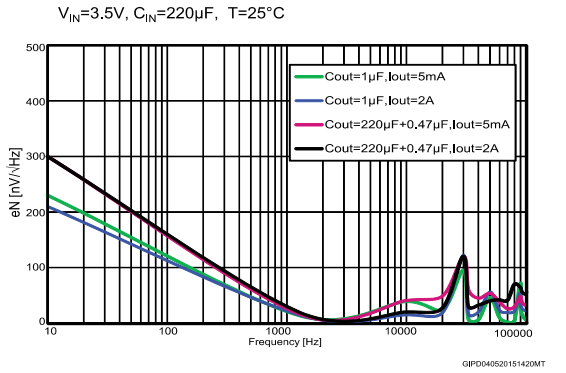


Figure 38: Supply voltage rejection vs. frequency

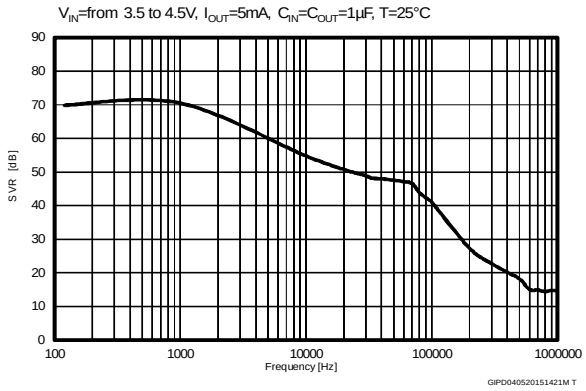


Figure 39: Stability plan vs. (ESR, C_{OUT})

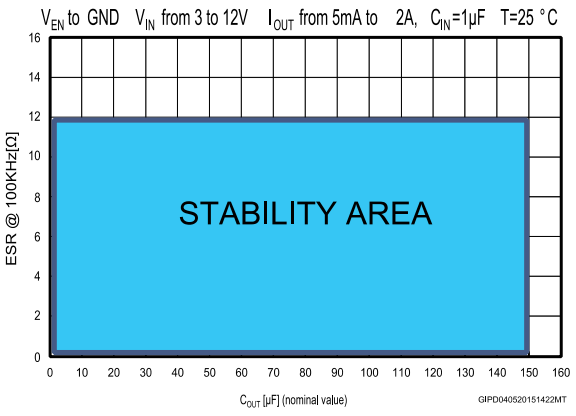
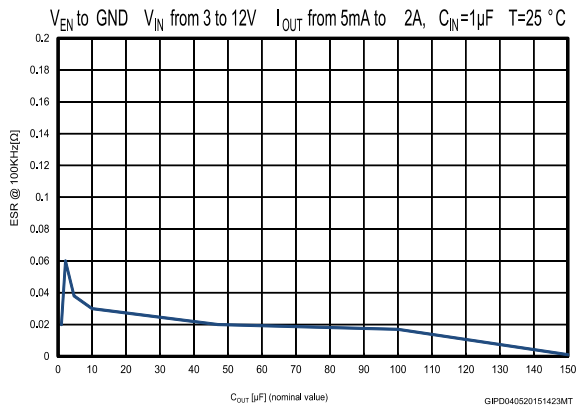


Figure 40: Minimum C_{OUT} ESR for stability



7 Device description

The device fixed voltage contains a PNP type power element controlled by a signal resulting from the amplified comparison between the internal temperature compensated bandgap cell and the fraction of the desired output voltage value. This fractional value is obtained by an internal-to-die resistor divider bridge set by STMicroelectronics. The device embeds current limit and thermal protection circuits.

7.1 Low pin count package limitations

Some functions (INHIBIT, OCM, SENSE) are not available due to lack of pins on the SMD.5 and TO-257 packages. Corresponding die pads are by default connected inside the silicon.

7.2 SENSE pin

The load voltage is connected to SENSE pin by a Kelvin line: voltage feedback comes from the internal divider resistor bridge. Therefore, possible output voltages are set by manufacturer's mask metal options. SENSE pin is not available in 3-pin packages.

7.3 Inhibit ON-OFF control

By setting INHIBIT pin TTL-high, the device switches off the output current and voltage. The device is on when INHIBIT pin is set low. Since INHIBIT pin is internally pulled down, it can be left floating in case inhibit function is not used. INHIBIT pin is not available in 3-pin packages.

7.4 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device goes off at 175 °C and it is again on mode when it is at 135 °C.

When the internal temperature detector reaches 175 °C, the active power element can be at 225 °C: the device reliability cannot be granted in case of extensive operation beyond these conditions.

7.5 Overcurrent protection

An internal foldback short-circuit limitation is set with I_{SHORT} typically higher than 3.8 A (V_O is 0 V). This value can be reduced by an external R_{SH} resistor connected between I_{SC} pin and V_I pin, with a typical value range from 25 kΩ to 200 kΩ. Lower values can be used, but the sample-to-sample spread for the given value increases. This adjustment feature is not available in 3-pin packages. To keep excellent V_O regulation, I_{SHORT} should be set 1.6 times greater than the maximum desired application I_O. When I_O reaches I_{SHORT} – 300 mA, the current limiter overrules regulation, V_O starts to drop and the OCM flag rises. When no current limitation adjustment is required, I_{SC} pin must be left un-biased (as it is in 3-pin packages). To choose the proper value of the R_{SH} resistor, refer to *Figure 35: "Short-circuit current vs. RSH"* and *Figure 36: "Short-circuit current vs. RSH (magnification)"*.

7.6 OCM pin

This pin goes low when current limiter starts to be active, otherwise $V_{OCM} = V_I$. It is bufferized and can sink 10 mA. OCM pin is internally pulled up by a 5 kΩ resistor.

7.7 Notes about Flat-16 package

The bottom of package is metallized to allow user to directly solder the voltage regulator to PCB, no heatsink is needed, in order to optimize heat removal performance. The bottom metallization is disconnected both from the regulator die and package terminals, hence electrically floating.

8 Application information

The device fixed voltage is functional as soon as V_I-V_O voltage difference is slightly above the power element saturation voltage. A minimum 0.5 mA I_O ensures the perfect “no-load” regulation.

All available V_I pins must always be externally interconnected, same thing for all available V_O pins, otherwise the device stability and reliability cannot be granted. All NC pins can be connected to ground. The inhibit function switches off the output current in an electronic manner. According to Lenz’s law, external circuitry reacts with–LdI/dt terms, which can have high amplitude in case series-inductance exists. The effect is a large transient voltage developed on both of the device terminals. Schottky diodes protect the device against negative voltage excursions. In the worst case, a 14 V Zener diode could protect the device input.

The device has been designed for high stability and low-drop out operation: minimum 1 µF input and output tantalum capacitors are therefore mandatory. The range of the capacitor ESR analysed at 100 kHz is from 0.01 Ω to over 20 Ω. This range is useful when ESR increases in case of low temperatures. The measured stability plane, versus capacitance and ESR are depicted in *Figure 39: "Stability plan vs. (ESR, COUT)"* and *Figure 40: "Minimum COUT ESR for stability"* . When large transient currents are expected, larger value capacitors are necessary.

In case of high current operation with expected short-circuit events, capacitors must be connected as close as possible to the device terminals. As some tantalum capacitors may permanently fail when submitted to high charge surge currents, it is recommended to decouple them with 470 nF polyester capacitors.

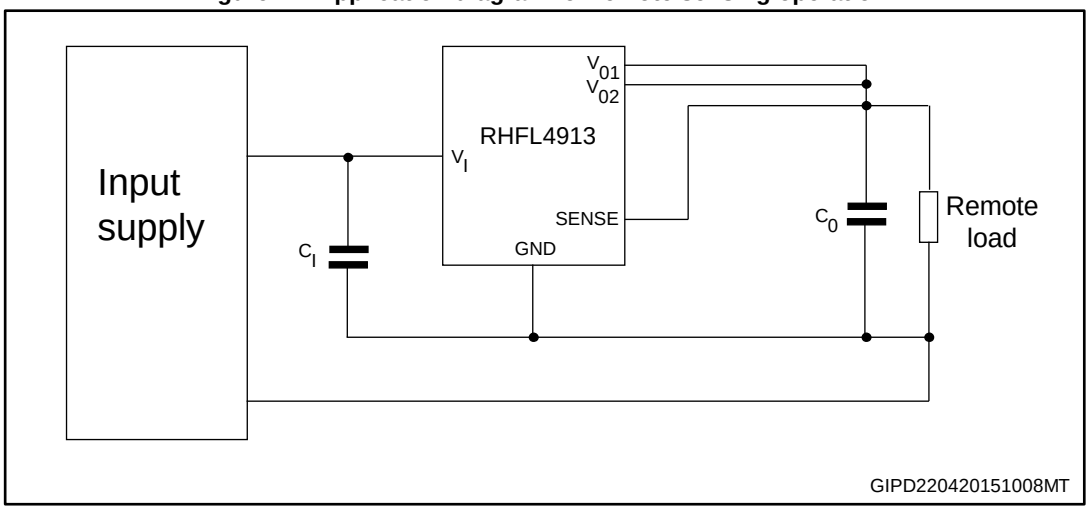
Being the device fixed voltage manufactured with very high speed bipolar technology (6 GHz f_T transistors), the PCB layout must be performed with extreme attention, very low inductance, low coupling lines, otherwise high frequency parasitic signals may be picked up by the device resulting into self-oscillation. The benefit for the user is an SVR performance extended to higher frequencies.

8.1 Remote sensing operation (Flat-16 only)

If the load is placed far from the regulator, the diagram shown in *Figure 41: "Application diagram for remote sensing operation"* has to be followed. To obtain the best regulation, the wire, which connects the SENSE pin to the load end, must not be crossed by the load current (Kelvin's sense). The two V_{OUT} pins and the SENSE pin must be connected as close as possible to the load in order to avoid the inclusion, into the regulation loop, of parasitic resistive drops related to the load current. The same applies to the ground return path, where unwanted drops across the wire resistance may appear (please refer to *Section 5.3.1: "Ground connections"* for additional guidelines about the suggested ground connection strategies).

The noise captured by the wires between the load and the chip could bring a noisy output voltage. In this case, shielded cables are used for these connections. It is also recommended to place 1 µF tantalum capacitors between output and ground close to the device and another 1 µF next to the load.

Figure 41: Application diagram for remote sensing operation



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

9.1 Flat-16 package information

Figure 42: Flat-16 package outline

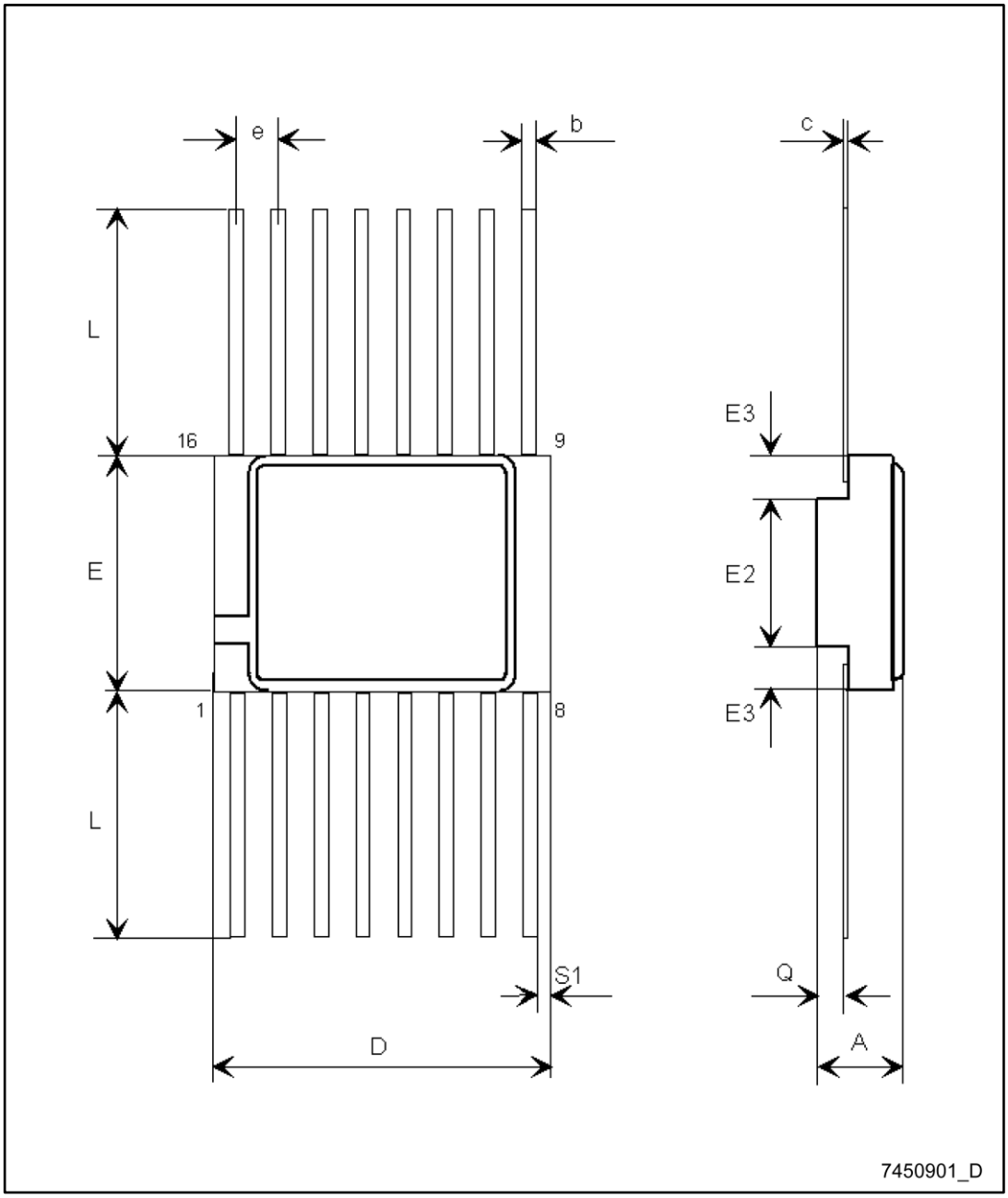


Table 9: Flat-16 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.42		2.88
b	0.38		0.48
c	0.10		0.18
D	9.71		10.11
E	6.71		7.11
E2	3.30	3.45	3.60
E3	0.76		
e		1.27	
L	6.35		7.36
Q	0.66		1.14
S1	0.13		

9.2 SMD.5 package information

Figure 43: SMD.5 package outline

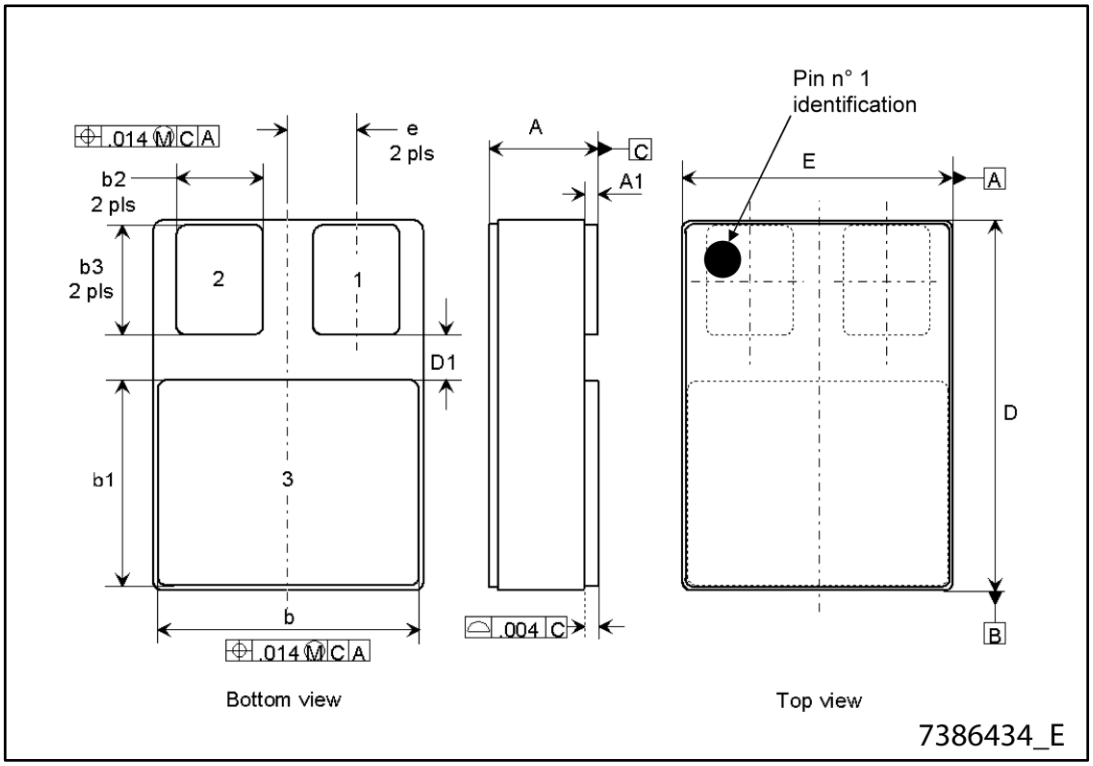


Table 10: SMD.5 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.84	3.00	3.15
A1	0.25	0.38	0.51
b	7.13	7.26	7.39
b1	5.58	5.72	5.84
b2	2.28	2.41	2.54
b3	2.92	3.05	3.18
D	10.03	10.16	10.28
D1	0.76		
E	7.39	7.52	7.64
e		1.91	

9.3 TO-257 package information

Figure 44: TO-257 package outline

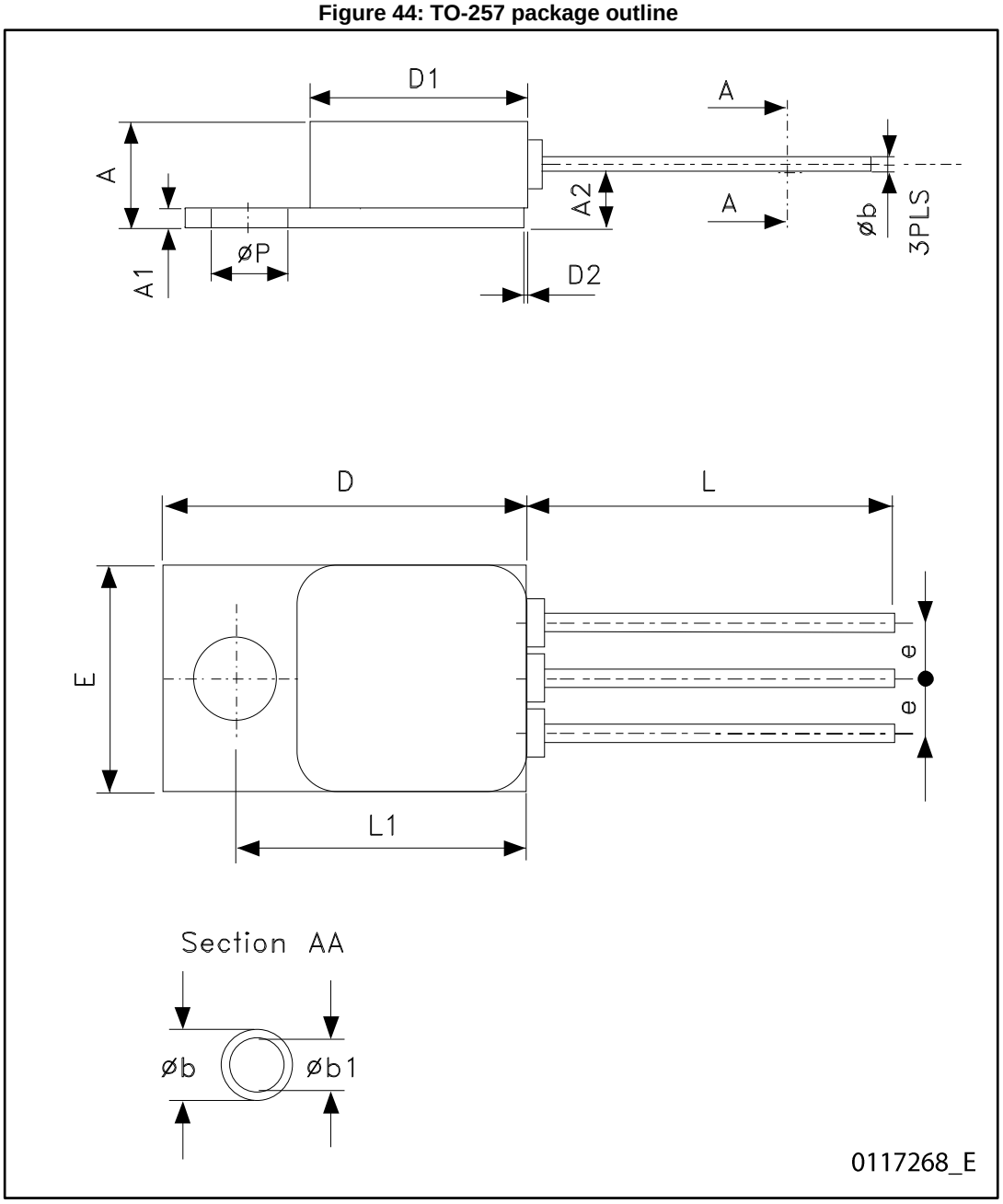


Table 11: TO-257 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.83		5.08
A1	0.89		1.14
A2		3.05	
b	0.64		1.02
b1	0.64	0.76	0.89
D	16.38		16.89
D1	10.41		10.92
D2	-	-	0.97
e		2.54	
E	10.41		10.67
L	12.70		19.05
L1	13.39		13.64
P	3.56		3.81

10 Ordering information

Table 12: Order codes

Flat-16	SMD.5	TO-257	Terminal finish	Output voltage	Quality level
RHFL4913KP15-01V (1)	RHFL4913S15-03V (1)	RHFL4913ESY1505V	Gold	1.5 V	QML-V
		RHFL4913ESY1506V	Solder	1.5 V	QML-V
RHFL4913KP151	RHFL4913S151	RHFL4913ESY151	Gold	1.5 V	EM1

Notes:

(1)QML-V qualification is currently in progress.

11 Revision history

Table 13: Document revision history

Date	Revision	Changes
31-Jul-2015	1	Initial release

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