# ON Semiconductor

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# NTD32N06

# Power MOSFET

## 32 Amps, 60 Volts, N−Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Pb−Free Packages are Available
- Smaller Package than MTB36N06V
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Total Gate Charge
- Lower and Tighter $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain−to−Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate−to−Source Voltage, Continuous<br>− Non−Repetitive ($t_p \le 10$ ms) | $V_{GS}$<br>$V_{GS}$ | ±20<br>±30 | Vdc |
| Drain Current<br>− Continuous @ $T_A$ = 25°C<br>− Continuous @ $T_A$ = 100°C<br>− Single Pulse ($t_p \le 10$ μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>32<br>22<br>90 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2) | $P_D$ | 93.75<br>0.625<br>2.88<br>1.5 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +175 | °C |
| Single Pulse Drain−to−Source Avalanche Energy − Starting $T_J$ = 25°C (Note 3) ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, L = 1.0 mH, $I_{L(pk)}$ = 25 A, $V_{DS}$ = 60 Vdc, $R_G$ = 25 Ω) | $E_{AS}$ | 313 | mJ |
| Thermal Resistance − Junction−to−Case<br>− Junction−to−Ambient (Note 1)<br>− Junction−to−Ambient (Note 2) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 1.6<br>52<br>100 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 $in^2$).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 $in^2$).
3. Repetitive rating; pulse width limited by maximum junction temperature.

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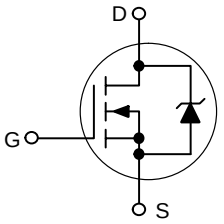
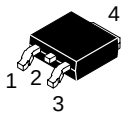
| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| 60 V | 26 mΩ | 32 A |

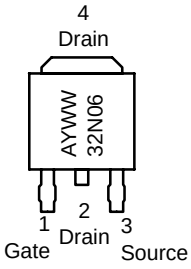
**N−Channel**

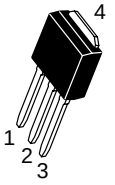



**MARKING DIAGRAMS**

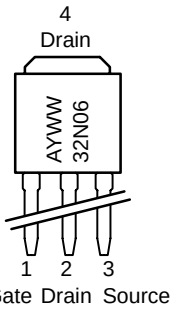



**DPAK**
**CASE 369C**
**STYLE 2**




**DPAK−3**
**CASE 369D**
**STYLE 2**




| | |
|---|---|
| 32N06 | = Device Code |
| A | = Assembly Location |
| Y | = Year |
| WW | = Work Week |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage (Note 4)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>− | <br>70<br>41.6 | <br>−<br>− | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>−<br>− | <br>−<br>− | <br>1.0<br>10 | μAdc |
| Gate−Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | − | − | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 4) | | | | | | |
| Gate Threshold Voltage (Note 4)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>− | <br>2.8<br>7.0 | <br>4.0<br>− | Vdc<br><br>mV/°C |
| Static Drain−to−Source On−Resistance (Note 4)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | <br>− | <br>21 | <br>26 | mΩ |
| Static Drain−to−Source On−Voltage (Note 4)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 32 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>−<br>−<br>− | <br>0.417<br>0.680<br>0.633 | <br>0.62<br>−<br>− | Vdc |
| Forward Transconductance (Note 4) ($V_{DS}$ = 6 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | − | 21.1 | − | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | − | 1231 | 1725 | pF |
| Output Capacitance | | $C_{oss}$ | − | 346 | 485 | |
| Transfer Capacitance | | $C_{rss}$ | − | 77 | 160 | |
| **SWITCHING CHARACTERISTICS** (Note 5) | | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 4) | $t_{d(on)}$ | − | 10 | 25 | ns |
| Rise Time | | $t_r$ | − | 84 | 180 | |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 31 | 70 | |
| Fall Time | | $t_f$ | − | 93 | 200 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc) (Note 4) | $Q_T$ | − | 33 | 60 | nC |
| | | $Q_1$ | − | 6.0 | − | |
| | | $Q_2$ | − | 15 | − | |
| **SOURCE−DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On−Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) (Note 4)<br>($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc) (Note 4)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | <br>−<br>−<br>− | <br>0.89<br>0.96<br>0.75 | <br>1.0<br>−<br>− | Vdc |
| Reverse Recovery Time | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 4) | $t_{rr}$ | − | 52 | − | ns |
| | | $t_a$ | − | 37 | − | |
| | | $t_b$ | − | 14.3 | − | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | − | 0.095 | − | μC |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

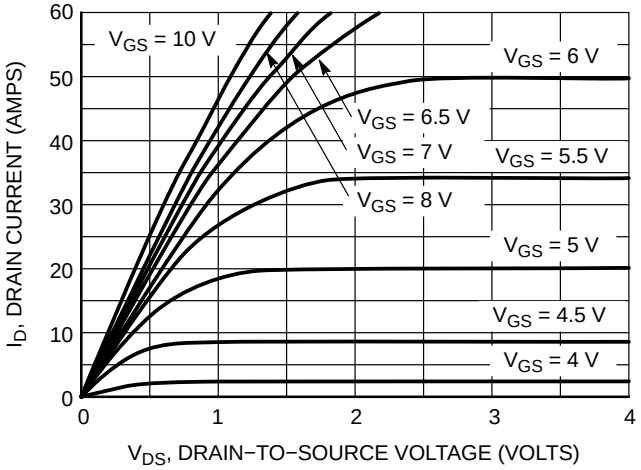



**Figure 1. On−Region Characteristics**

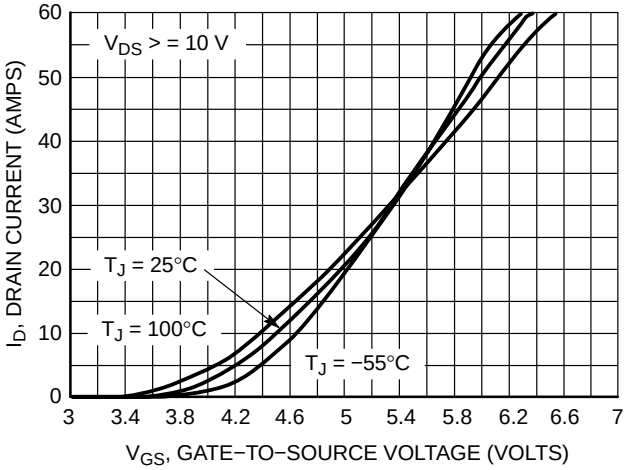



**Figure 2. Transfer Characteristics**

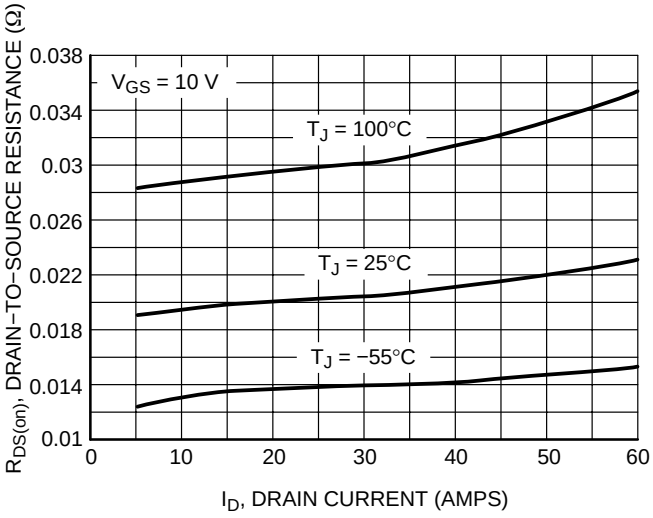



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

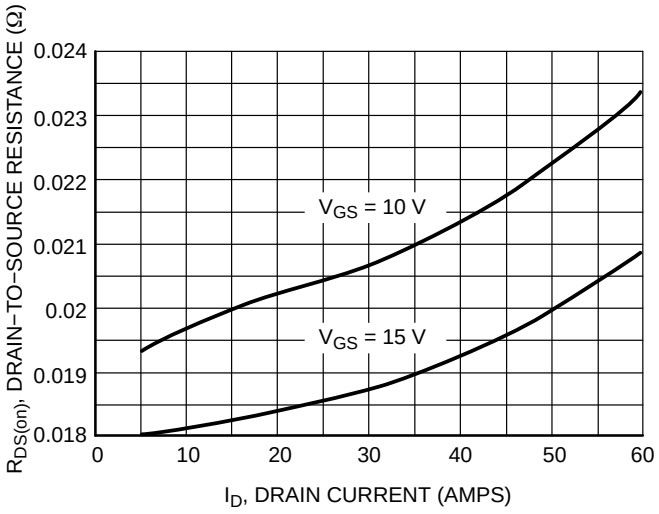



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

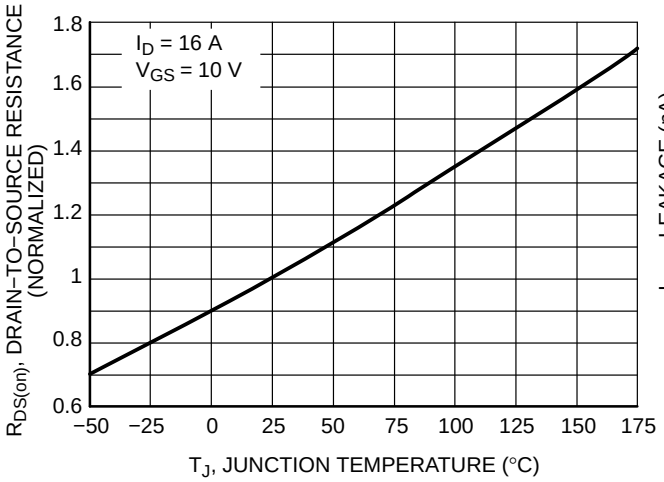



**Figure 5. On−Resistance Variation with Temperature**

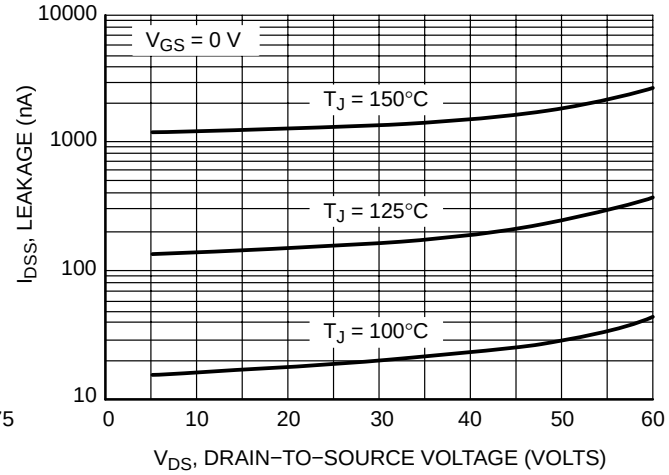



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

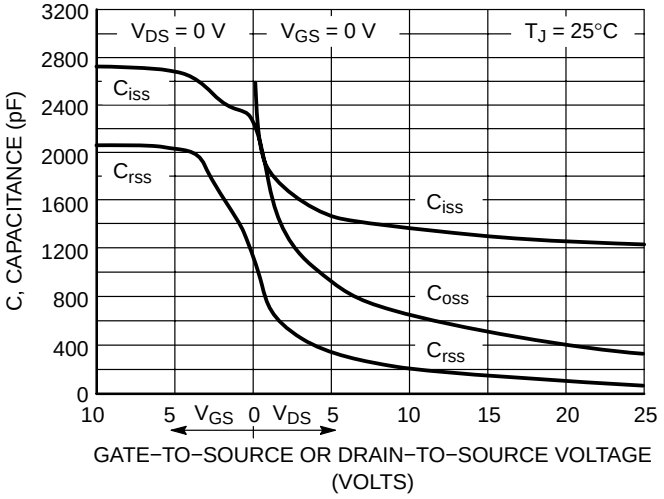



**Figure 7. Capacitance Variation**

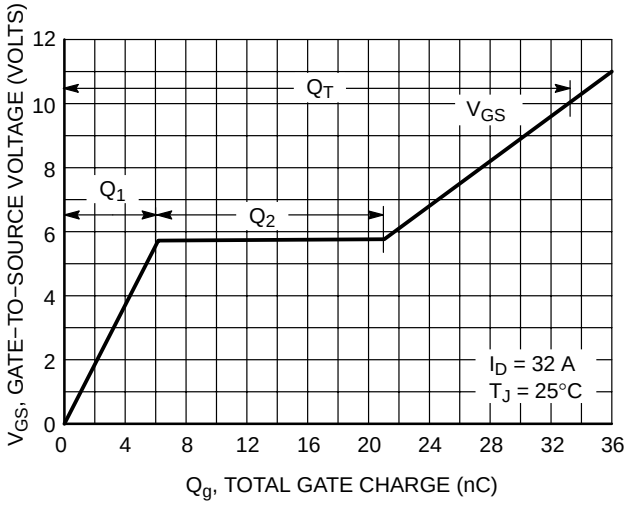



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

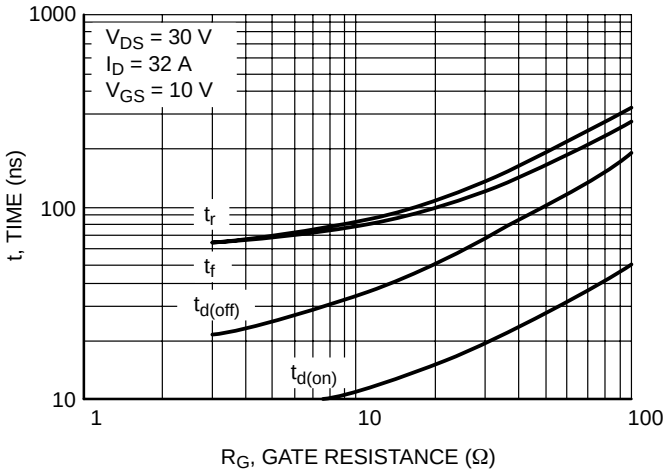



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

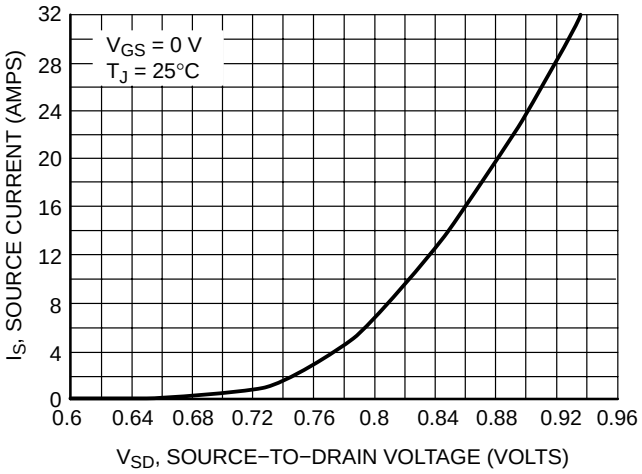



**Figure 10. Diode Forward Voltage vs. Current**

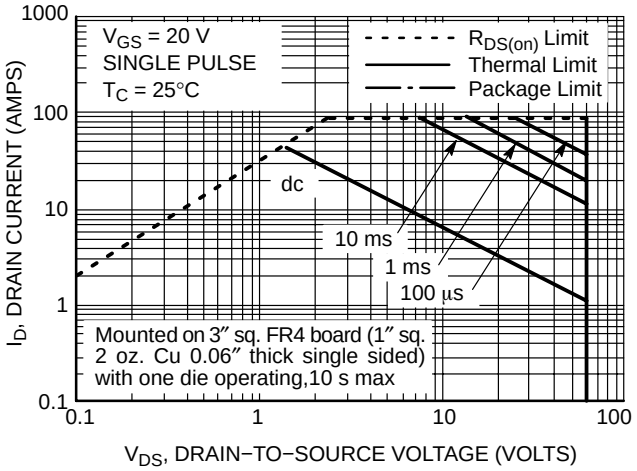



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

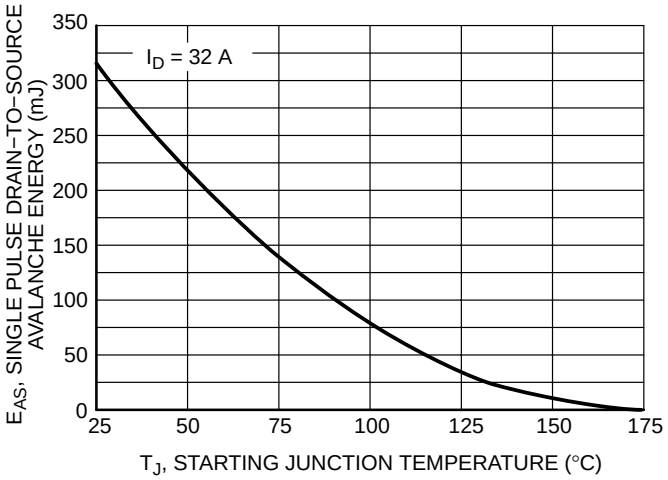



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

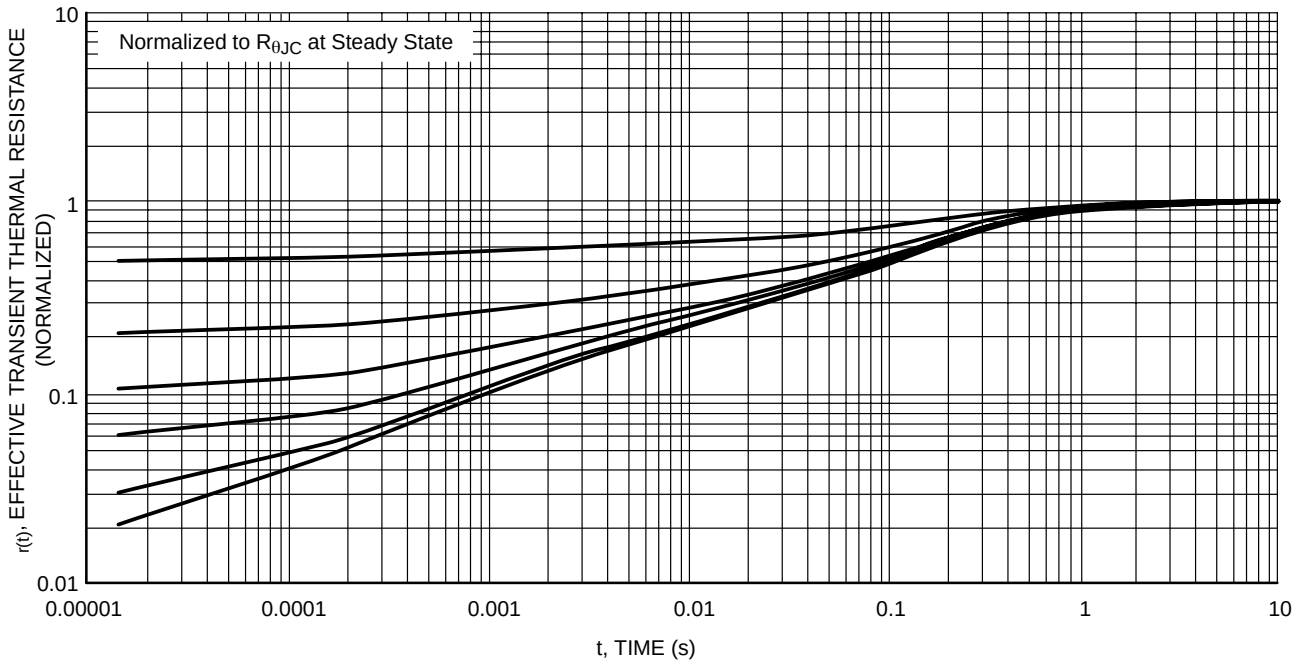



**Figure 13. Thermal Response**

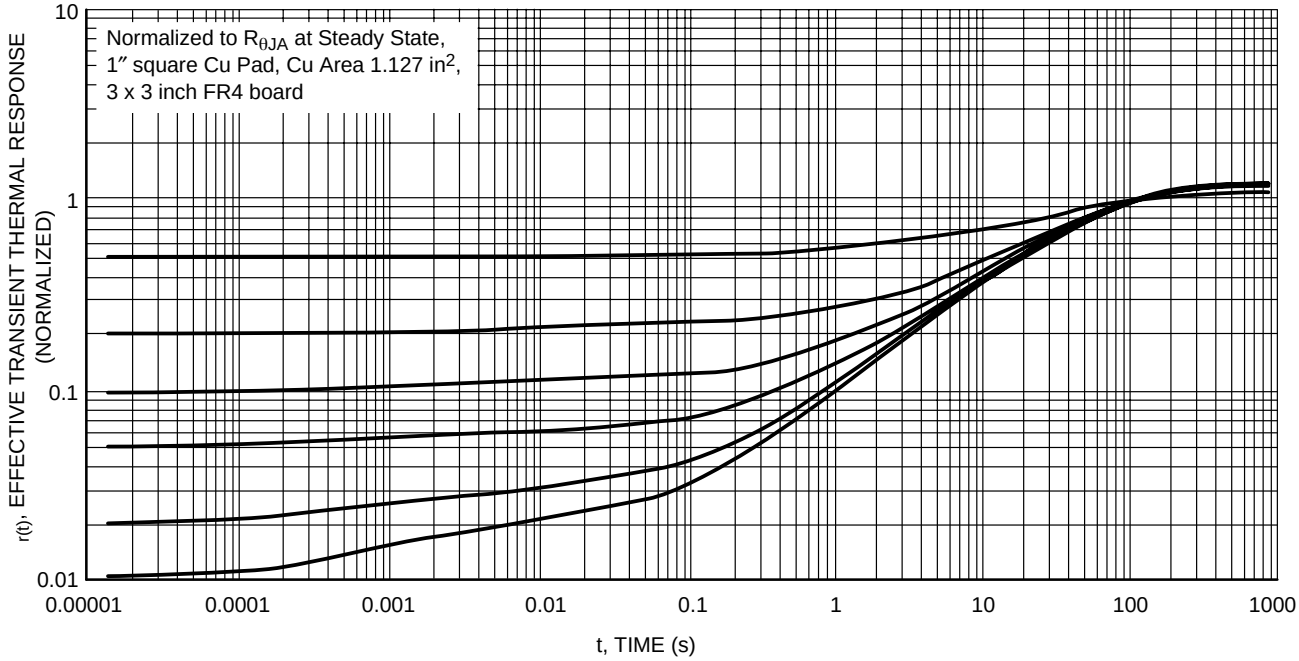



**Figure 14. Thermal Response**

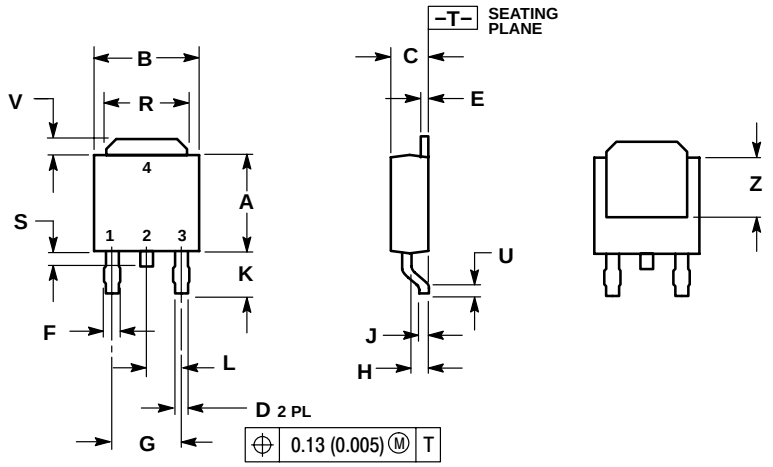
## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTD32N06 | DPAK | 75 Units/Rail |
| NTD32N06G | DPAK (Pb−Free) | 75 Units/Rail |
| NTD32N06−1 | DPAK−3 | 75 Units/Rail |
| NTD32N06−1G | DPAK−3 (Pb−Free) | 75 Units/Rail |
| NTD32N06T4 | DPAK | 2500 Tape & Reel |
| NTD32N06T4G | DPAK (Pb−Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

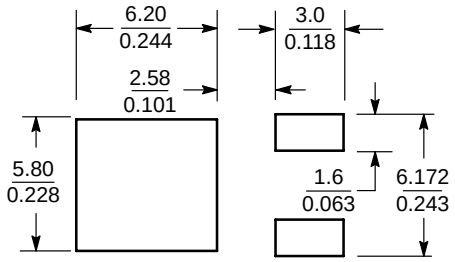
**DPAK**
CASE 369C−01
ISSUE O




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.180 BSC | | 4.58 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC | | 2.29 BSC | |
| R | 0.180 | 0.215 | 4.57 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | −−− | 0.51 | −−− |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

## SOLDERING FOOTPRINT*

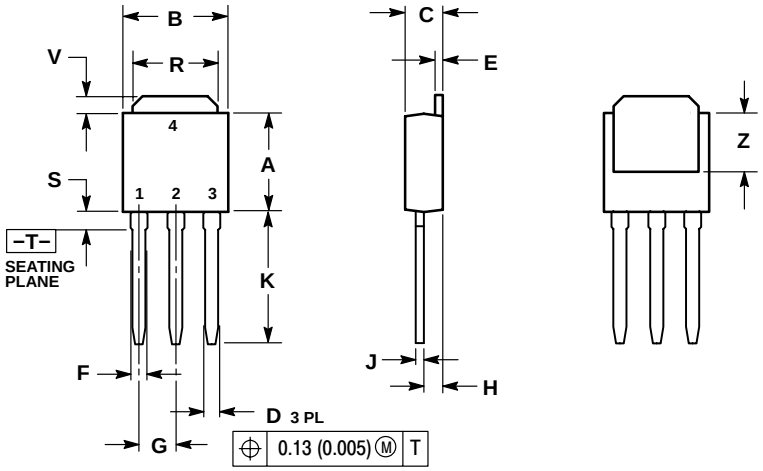



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## PACKAGE DIMENSIONS

**DPAK−3**
CASE 369D−01
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.037 | 0.045 | 0.94 | 1.14 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.180 | 0.215 | 4.45 | 5.45 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | −−− | 3.93 | −−− |

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



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**NTD32N06/D**