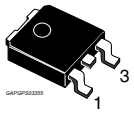
RVND14NV04

OMNIFETII fully autoprotected Power MOSFET

Datasheet - production data



TO-252 (DPAK)

Features

TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
RVND14NV04	35 mΩ	12 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
  - Compatible with standard Power MOSFET
- Aerospace and Defense features
  - Dedicated traceability and part marking
  - Production parts approval documents available
  - Adapted Extended life time and obsolescence management
  - Extended Product Change Notification process
  - Designed and manufactured to meet sub ppm quality goals
  - Advanced mold and frame designs for Superior resilience to harsh environment (acceleration, EMI, thermal, humidity)
  - Single Fabrication, Assembly and Test site
  - Dual internal production source capability

Applications

- All types of resistive, inductive and capacitive loads in Aerospace and Defense applications.

Description

The RVND14NV04 is a monolithic device made using STMicroelectronics VIPower® M0-technology, intended for replacement of standard Power MOSFETS in DC to 50 KHz applications.

Built-in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Order code	Package	Packing
RVND14NV04TR	TO-252 (DPAK)	Tape and reel

This is information on a product in full production. www.st.com

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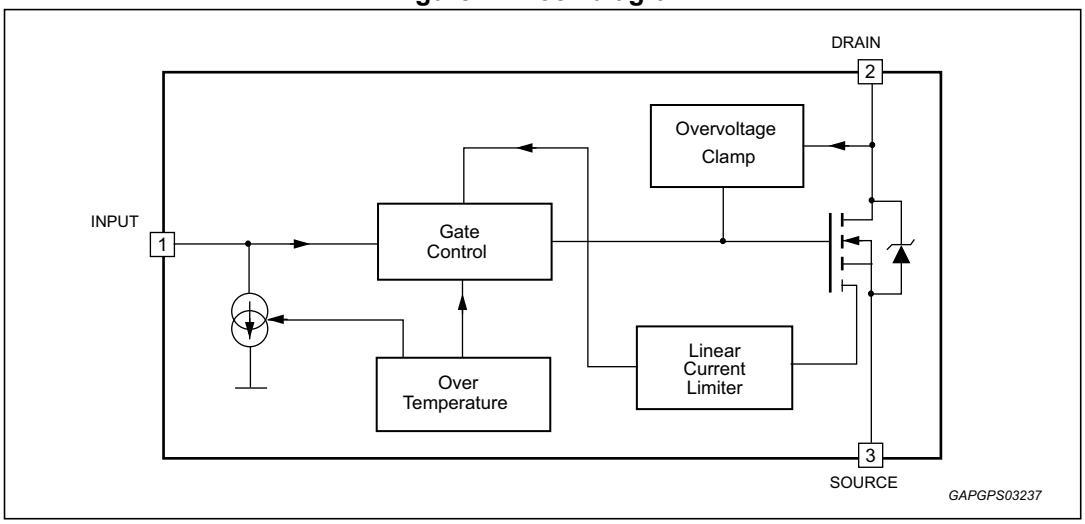
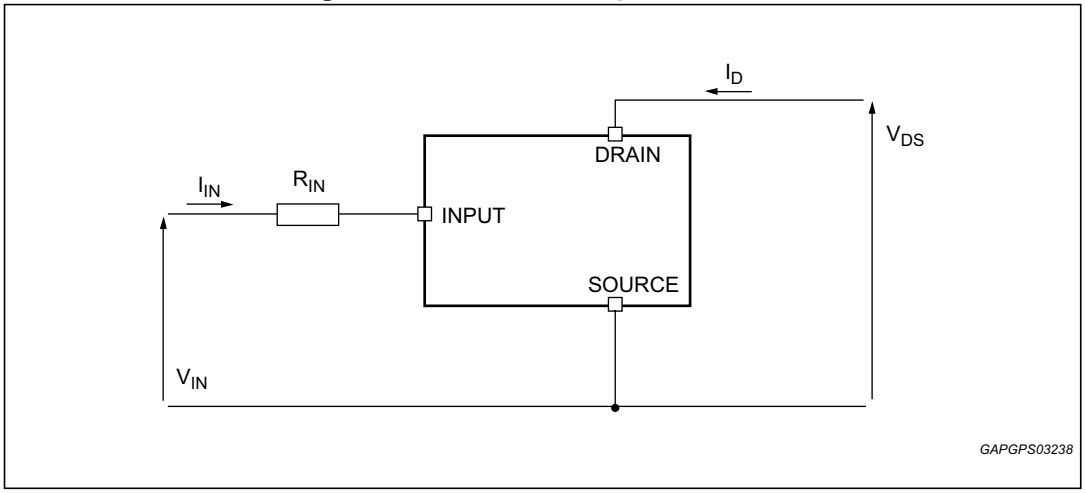
1 Block diagram

Figure 1. Block diagram



2 Electrical specification

Figure 2. Current and voltage conventions



2.1 Absolute maximum rating

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{IN} = 0 V)	Internally clamped	V
V_{IN}	Input voltage	Internally clamped	V
I_{IN}	Input current	±20	mA
$R_{IN\ MIN}$	Minimum input series impedance	10	Ω
I_D	Drain current	Internally limited	A
I_R	Reverse DC output current	-15	A
V_{ESD1}	Electrostatic discharge (R = 1.5 kΩ, C = 100 pF)	4000	V
V_{ESD2}	Electrostatic discharge on output pin only (R = 330 Ω, C = 150 pF)	16500	V
P_{tot}	Total dissipation at T_c = 25 °C	74	W
E_{MAX}	Maximum switching energy (L = 0.4 mH; R_L = 0 Ω; V_{bat} = 13.5 V; T_{jstart} = 150 °C; I_L = 18 A)	93	mJ
T_j	Operating junction temperature	Internally limited	°C
T_c	Case operating temperature	Internally limited	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.7	°C/W
$R_{thj\text{-}lead}$	Thermal resistance junction-lead max		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	65(1)	°C/W

1. When mounted on a standard single-sided FR4 board with 0.5 cm^2 of Cu (at least 35 µm thick) connected to all DRAIN pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

-40 < T_j < 150 °C unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Off						
V_{CLAMP}	Drain-source clamp voltage	V_{IN} = 0 V; I_D = 7 A	40	45	55	V
V_{CLTH}	Drain-source clamp threshold voltage	V_{IN} = 0 V; I_D = 2 mA	36	-	-	V
V_{INTH}	Input threshold voltage	V_{DS} = V_{IN}; I_D = 1 mA	0.5	-	2.5	V
I_{ISS}	Supply current from input pin	V_{DS} = 0 V; V_{IN} = 5 V	-	100	150	µA
V_{INCL}	Input-source clamp voltage	I_{IN} = 1 mA	6	6.8	8	V
		I_{IN} = -1 mA	-1.0	-	-0.3	V
I_{DSS}	Zero input voltage drain current (V_{IN} = 0 V)	V_{DS} = 13 V; V_{IN} = 0 V; T_j = 25 °C	-	-	30	µA
		V_{DS} = 25 V; V_{IN} = 0 V	-	-	75	µA
On						
$R_{DS(on)}$	Static drain-source on resistance	V_{in} = 5 V; I_D = 7 A; T_j = 25 °C	-	-	35	mΩ
		V_{in} = 5 V; I_D = 7 A	-	-	70	mΩ
Dynamic (T_j = 25°C, unless otherwise specified)						
g_f (1)	Forward transconductance	V_{DD} = 13 V; I_D = 7 A	-	18	-	S
C_{oss}	Output capacitance	V_{DS} = 13 V; f = 1 MHz V_{IN} = 0 V	-	400	-	pF
Switching						
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_D = 7 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 10 Ω; (see *Figure 3*)	-	80	250	ns
t_r	Rise time		-	350	1000	ns
$t_{d(off)}$	Turn-off delay time		-	450	1350	ns
t_f	Fall time		-	150	500	ns

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 15 V; I_d = 7 A; V_{gen} = 5 V; R_{gen} = 2.2 kΩ (see *Figure 3*)	-	1.5	4.5	µs
t_r	Rise time		-	9.7	30.0	µs
$t_{d(off)}$	Turn-off delay time		-	-	25.0	µs
t_f	Fall time		-	10.2	30.0	µs
$(di/dt)_{on}$	Turn-on current slope	V_{DD} = 15 V; I_D = 7 A; V_{gen} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 10 Ω	-	16	-	A/µs
Q_i	Total input charge	V_{DD} = 12 V; I_D = 7 A; V_{in} = 5 V; I_{gen} = 2.13 mA (see *Figure 7*)	-	36.8	-	nC
Source drain diode						
V_{SD} (1)	Forward on voltage	I_{SD} = 7 A; V_{in} = 0 V	-	0.8	-	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A; di/dt = 40 A/µs; V_{DD} = 30 V; L = 200 µH (see test circuit, *Figure 4*)	-	300	-	ns
Q_{rr}	Reverse recovery charge		-	0.8	-	µC
I_{RRM}	Reverse recovery current		-	5	-	A
Protection						
I_{lim}	Drain current limit	V_{IN} = 5 V; V_{DS} = 13 V	12	18	24	A
t_{dlim}	Step response current limit	V_{IN} = 5 V; V_{DS} = 13 V	-	45	-	µs
T_{jsh}	Over temperature shutdown	-	150	175	200	°C
T_{jrs}	Over temperature reset	-	135	-	-	°C
I_{gf}	Fault sink current	V_{IN} = 5 V; V_{DS} = 13 V; T_j = T_{jsh}	10	15	20	mA
E_{as}	Single pulse avalanche energy	Starting T_j = 25 °C; V_{DD} = 24 V; V_{IN} = 5 V; R_{gen} = $R_{IN\ MIN}$ = 10 Ω; L = 24 mH (see *Figure 5* and *Figure 6*)	400	-	-	mJ

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

3 Protection features

During normal operation, the input pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC up to 50 kHz. The only difference from the user's standpoint is that a small DC current I_{ISS} (typ. 100 µA) flows into the input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 45 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the input pin voltages. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the over temperature threshold T_{jsh}.
- Over temperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Over temperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15 °C below shutdown temperature.
- Status feedback: in the case of an over temperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current Igf through the input pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the input pin driver is not able to supply the current I_{gf}, the input pin will fall to 0 V. This will not however affect the device operation: no requirement is put on the current capability of the input pin driver except to be able to supply the normal operation drive current I_{ISS}.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Figure 3. Switching time test circuit for resistive load

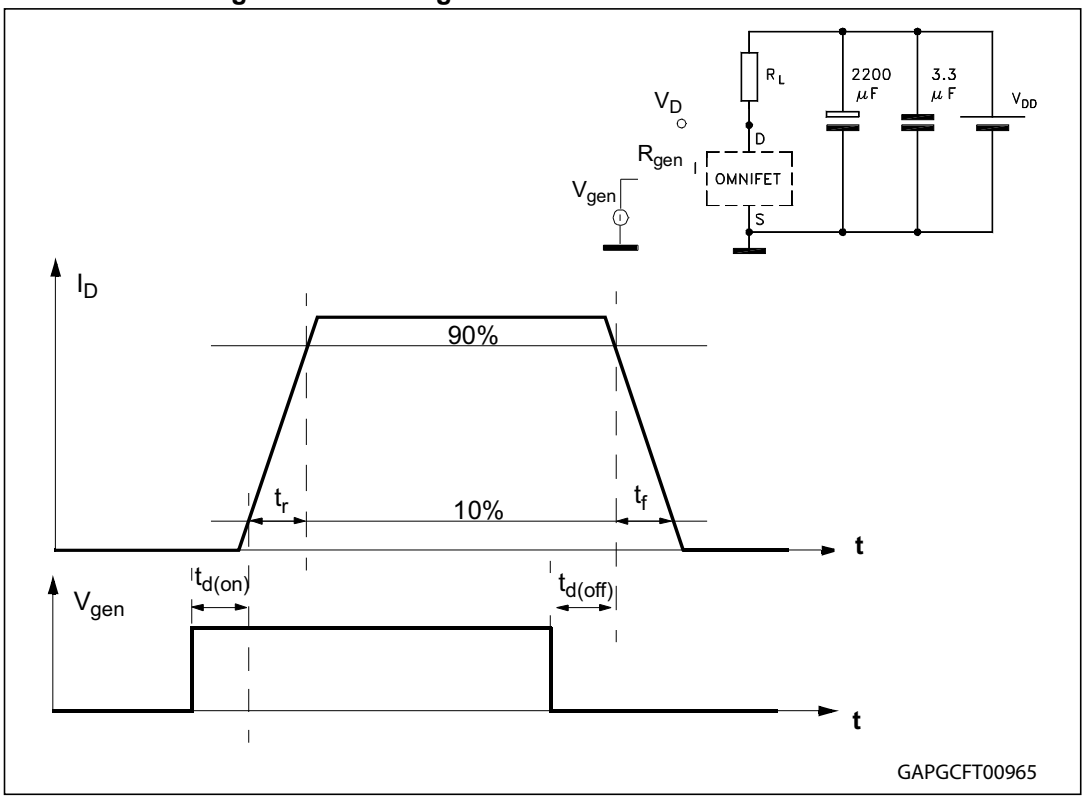


Figure 4. Test circuit for diode recovery times

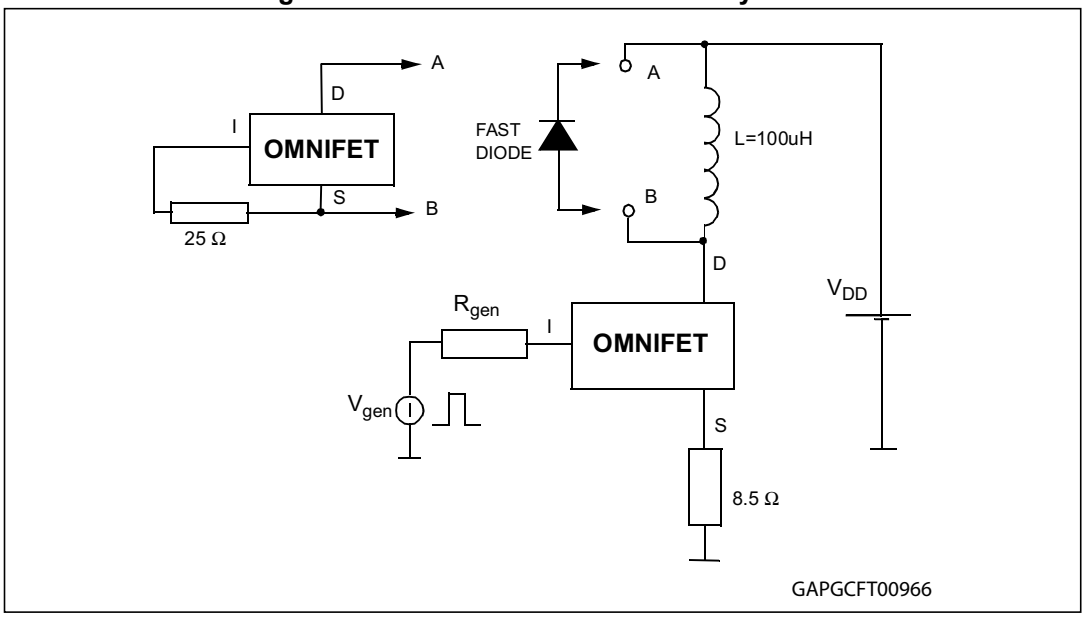


Figure 5. Unclamped inductive load test circuits

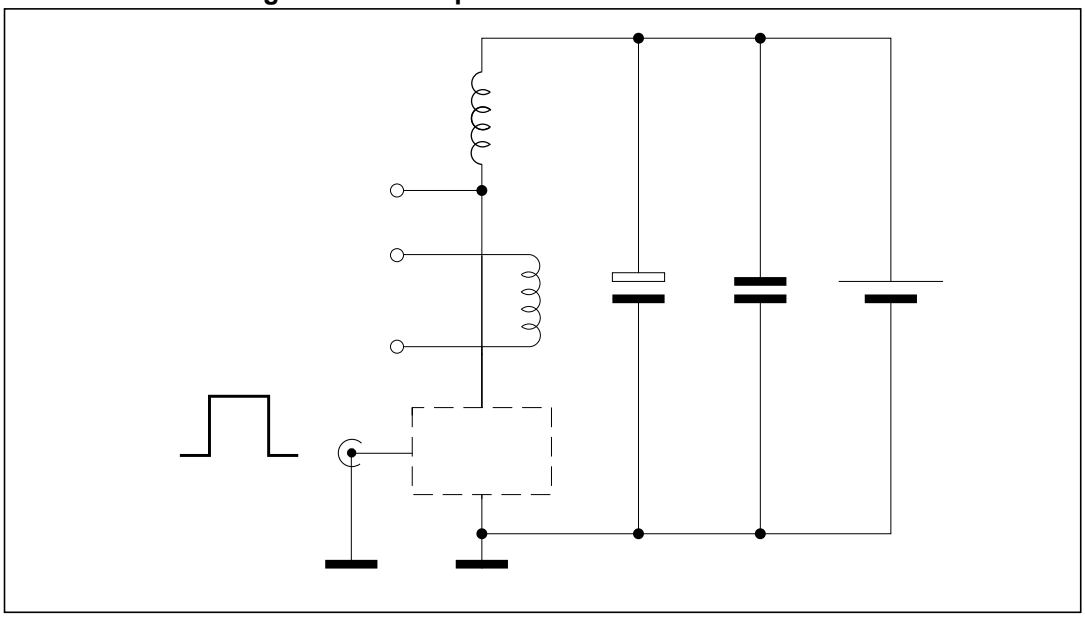


Figure 6. Unclamped inductive waveforms

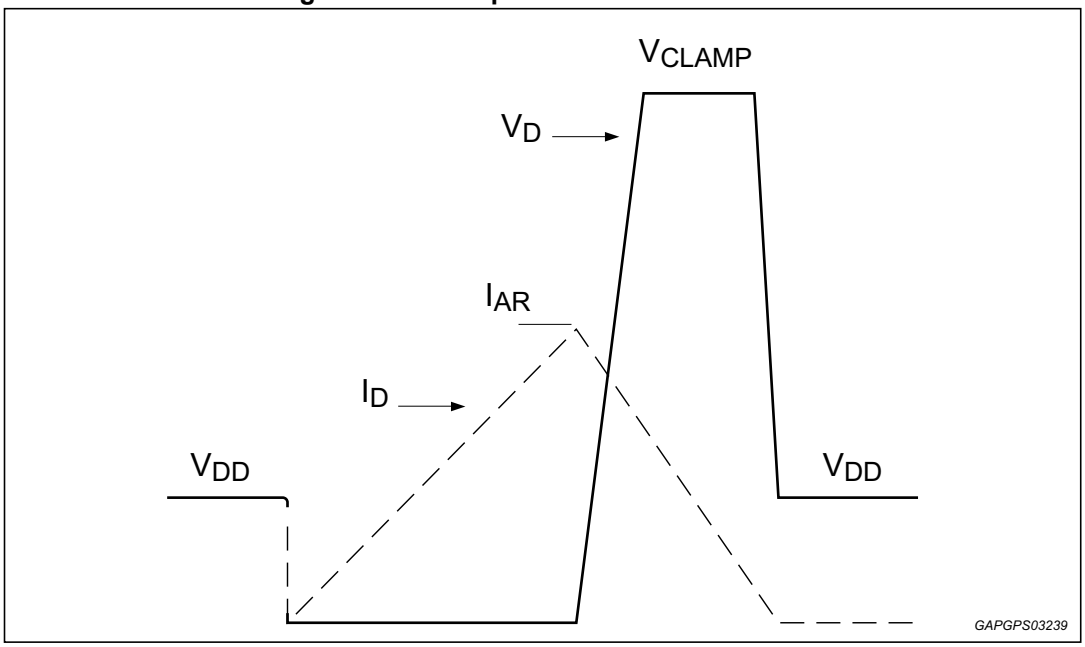
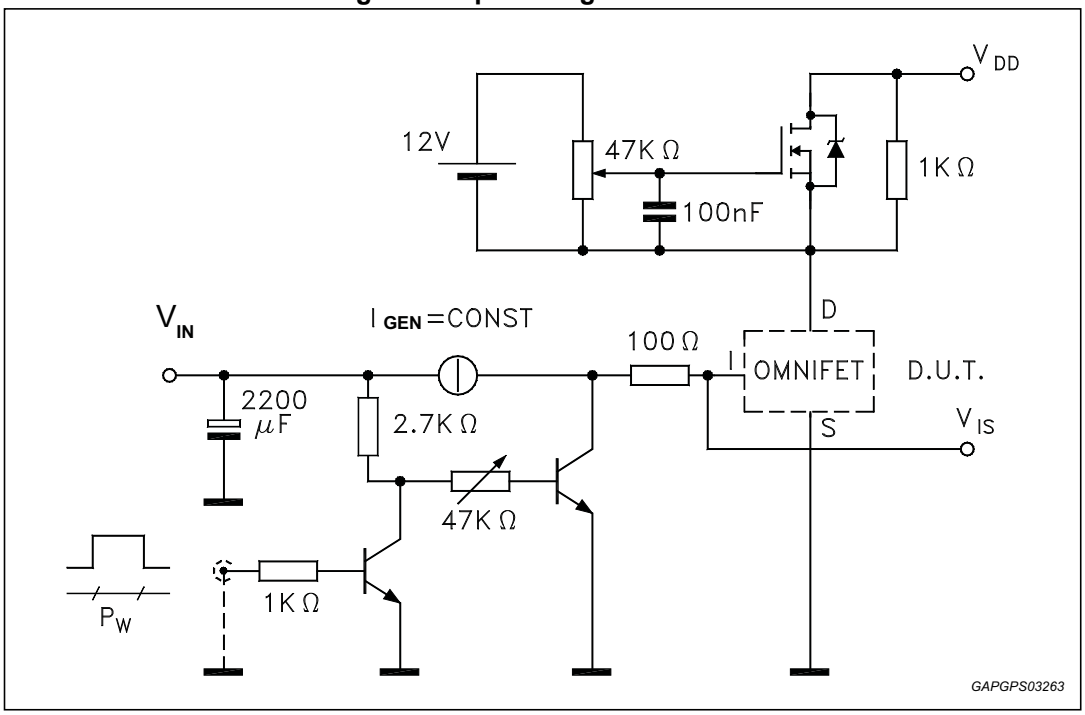


Figure 7. Input charge test circuit



3.1 Electrical characteristics curves

Figure 8. Source-drain diode forward characteristics

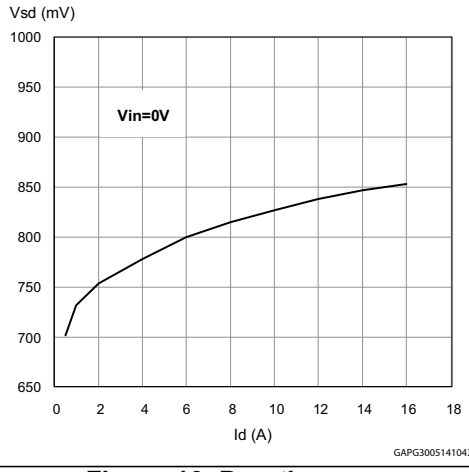


Figure 9. Static drain source on resistance

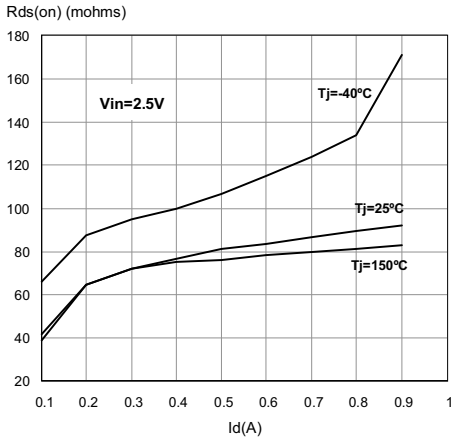


Figure 10. Derating curve

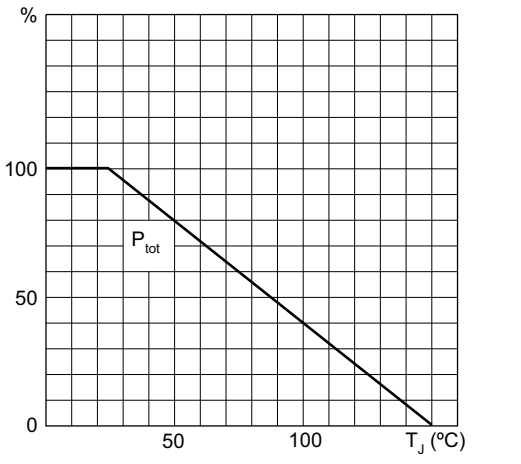


Figure 11. Static drain-source on resistance vs. input voltage (part 1/2)

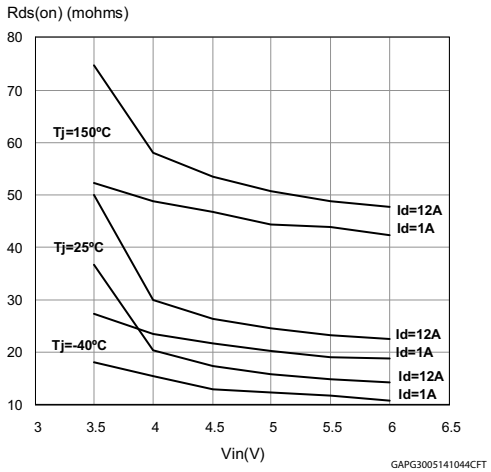


Figure 12. Static drain-source on resistance vs. input voltage (part 2/2)

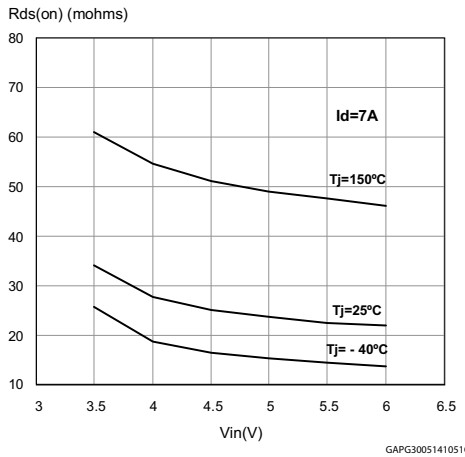


Figure 13. Transconductance

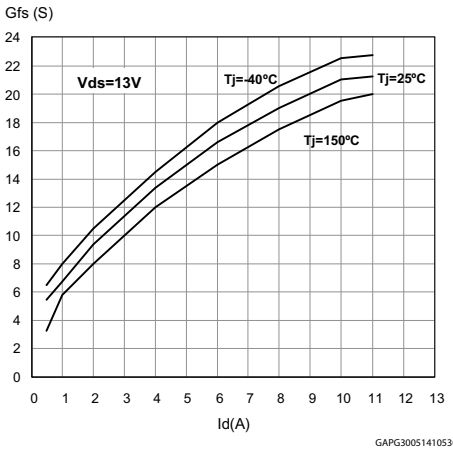


Figure 14. Static drain-source on resistance vs. id

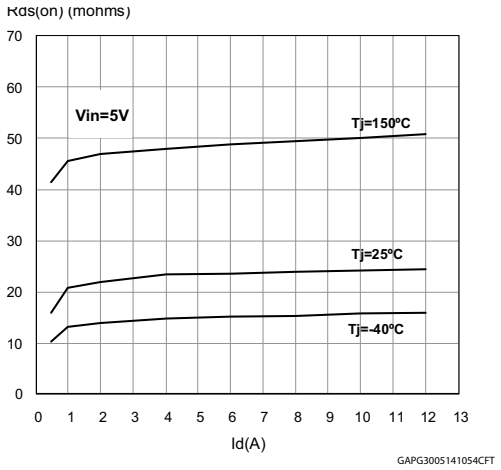


Figure 15. Transfer characteristics

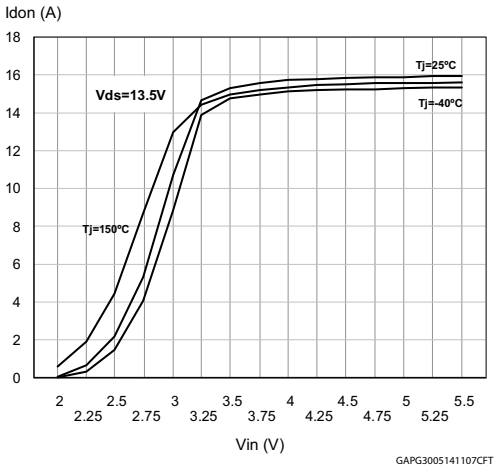


Figure 16. Turn-on current slope (part 1/2)

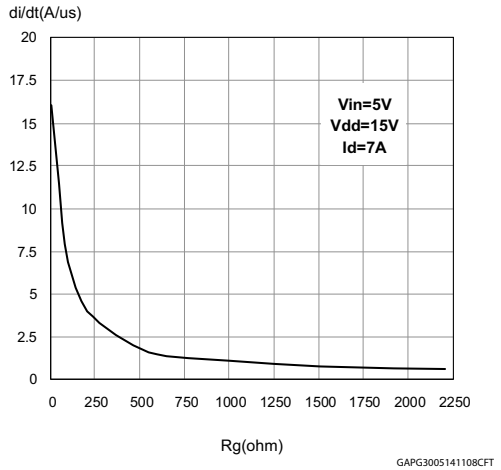


Figure 17. Turn-on current slope (part 2/2)

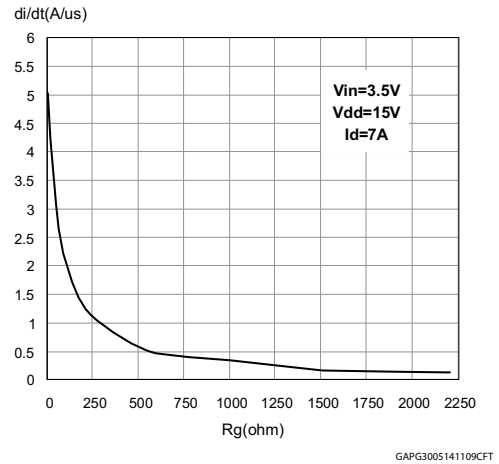


Figure 18. Input voltage vs. input charge

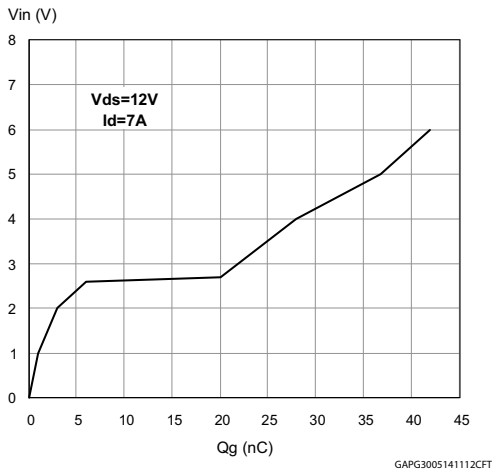


Figure 19. Turn-off drain source voltage slope (part 1/2)

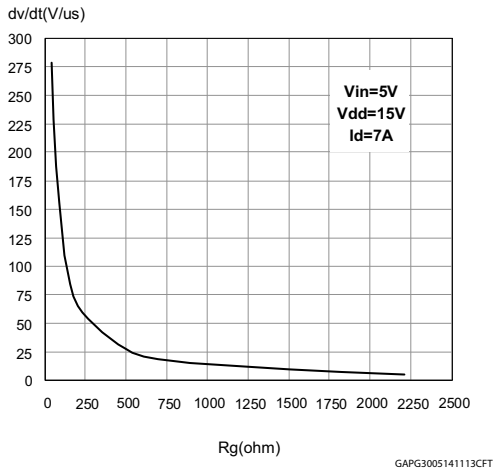


Figure 20. Turn-off drain source voltage slope (part 2/2)

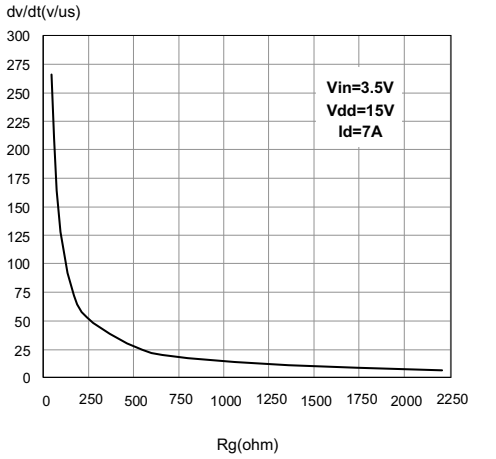


Figure 21. Capacitance variations

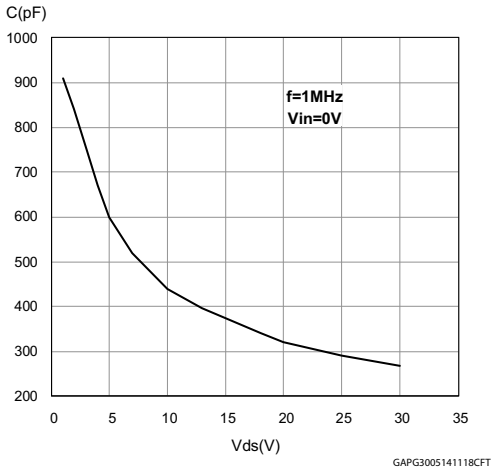


Figure 22. Switching time resistive load (part 1/2)

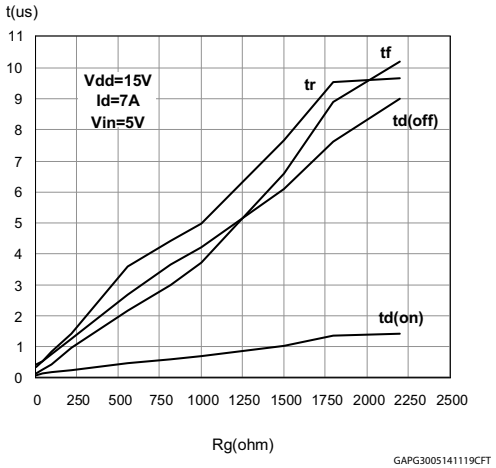


Figure 23. Switching time resistive load (part 2/2)

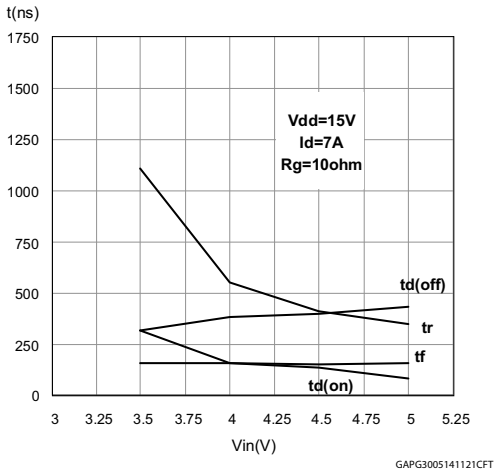


Figure 24. Output characteristics

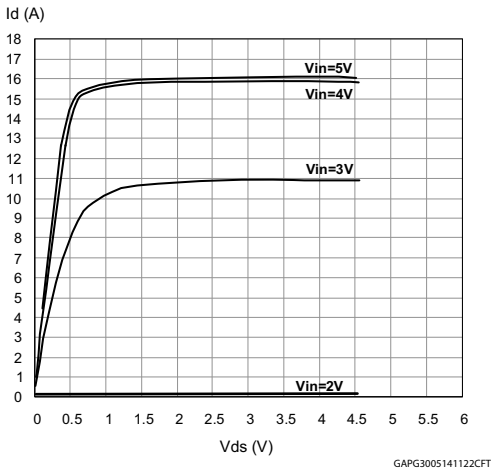


Figure 25. Normalized on resistance vs. temperature

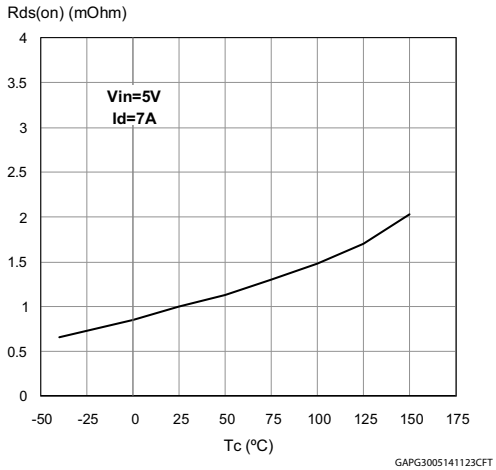


Figure 26. Normalized input threshold voltage vs. temperature

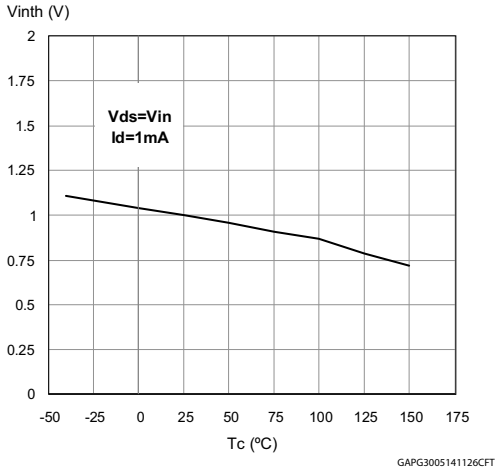


Figure 27. Current limit vs. junction temperatures

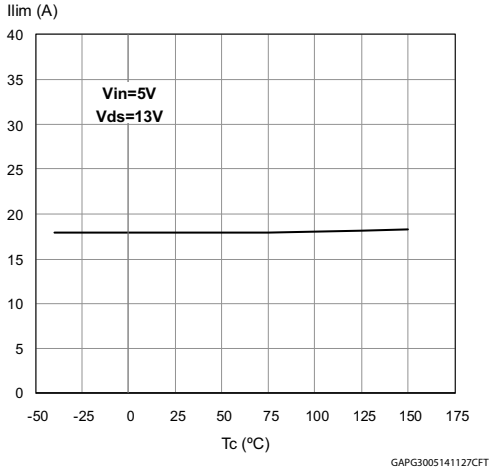


Figure 28. Step response current limit

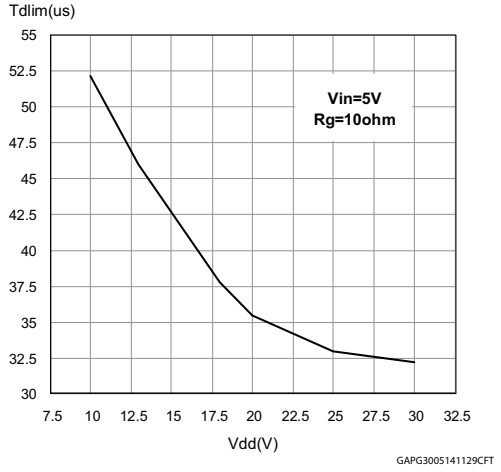
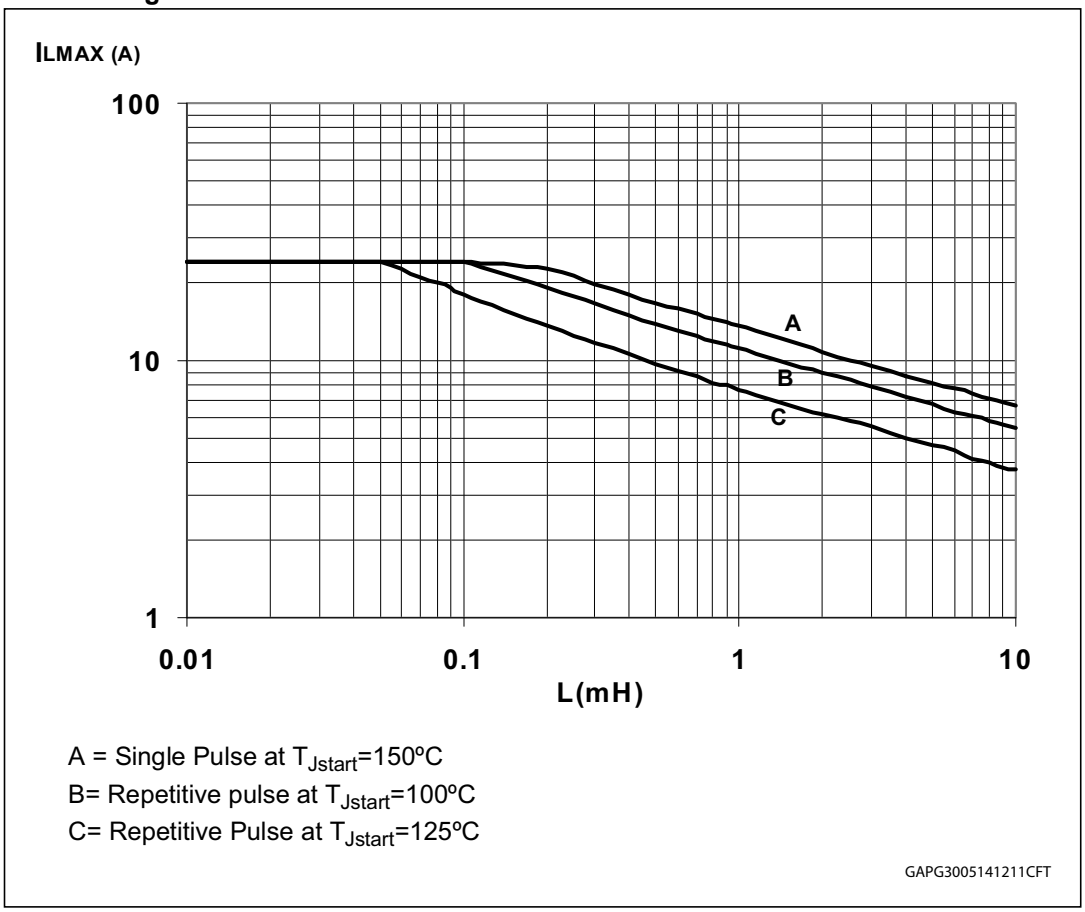


Figure 29. DPAK maximum turn-off current versus load inductance

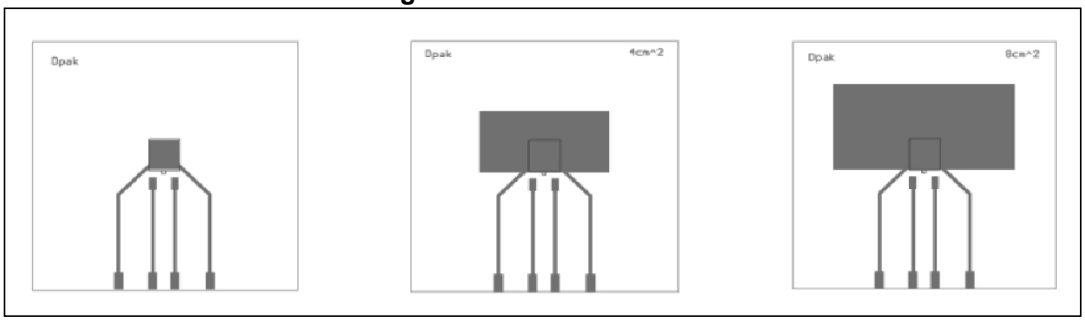


1. Conditions: V_{CC}=13.5 V; Values are generated with R_L=0 Ω. In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package thermal data

4.1 DPAK thermal data

Figure 30. DPAK PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 60 mm x 60 mm, PCB thickness=2 mm, Cu thickness=35 µm, Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 31. DPAK $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

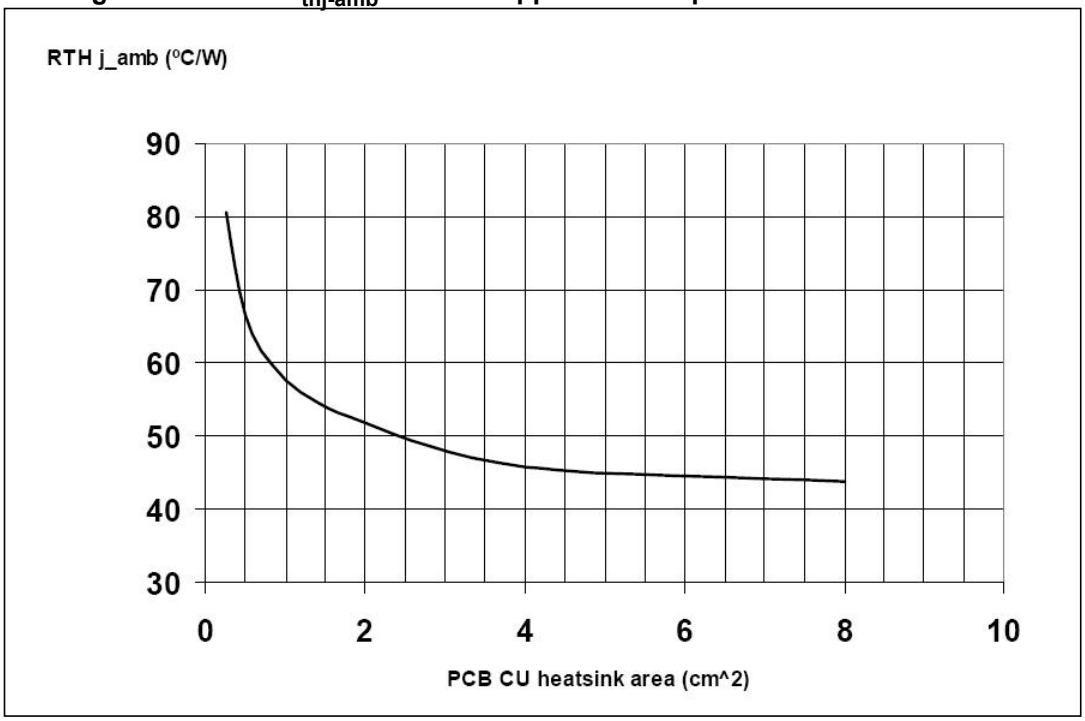


Figure 32. DPAK thermal impedance junction ambient single pulse

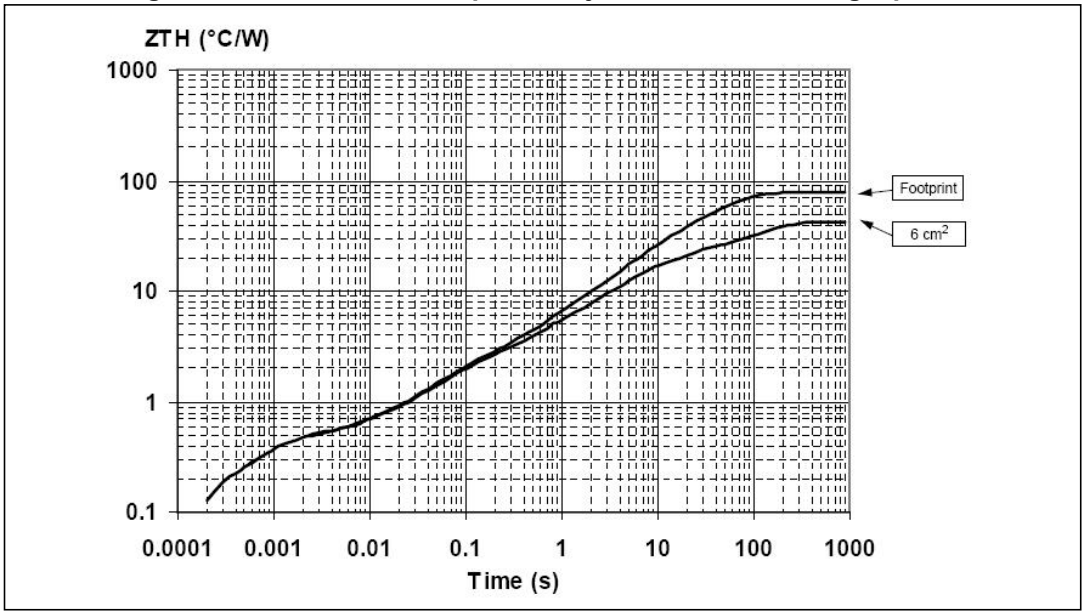
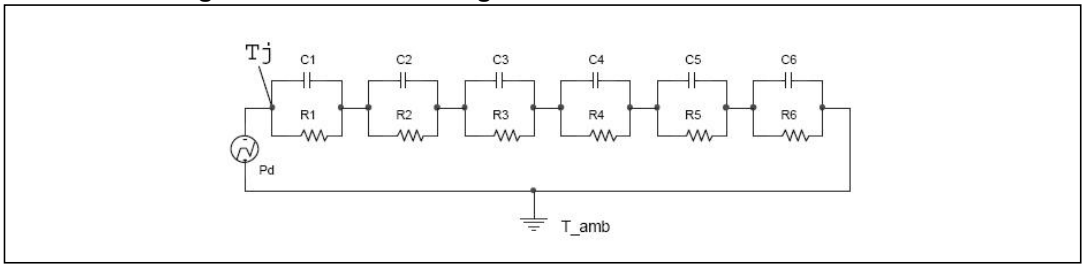


Figure 33. Thermal fitting model of an OMNIFET II in DPAK



Pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 5. DPAK thermal parameter

Area/island(cm²)	Footprint	6
R1 (°C/W)	0.1	
R2 (°C/W)	0.35	
R3 (°C/W)	1.20	
R4 (°C/W)	2	
R5 (°C/W)	15	
R6 (°C/W)	61	24
C1 (W.s/°C)	0.0006	
C2 (W.s/°C)	0.0021	
C3 (W.s/°C)	0.05	

Table 5. DPAK thermal parameter (continued)

Area/island(cm^2)	Footprint	6
C4 (W.s/°C)	0.3	
C5 (W.s/°C)	0.45	
C6 (W.s/°C)	0.8	5

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

5.2 TO-252 (DPAK) mechanical data

Figure 34. TO-252 (DPAK) package dimension

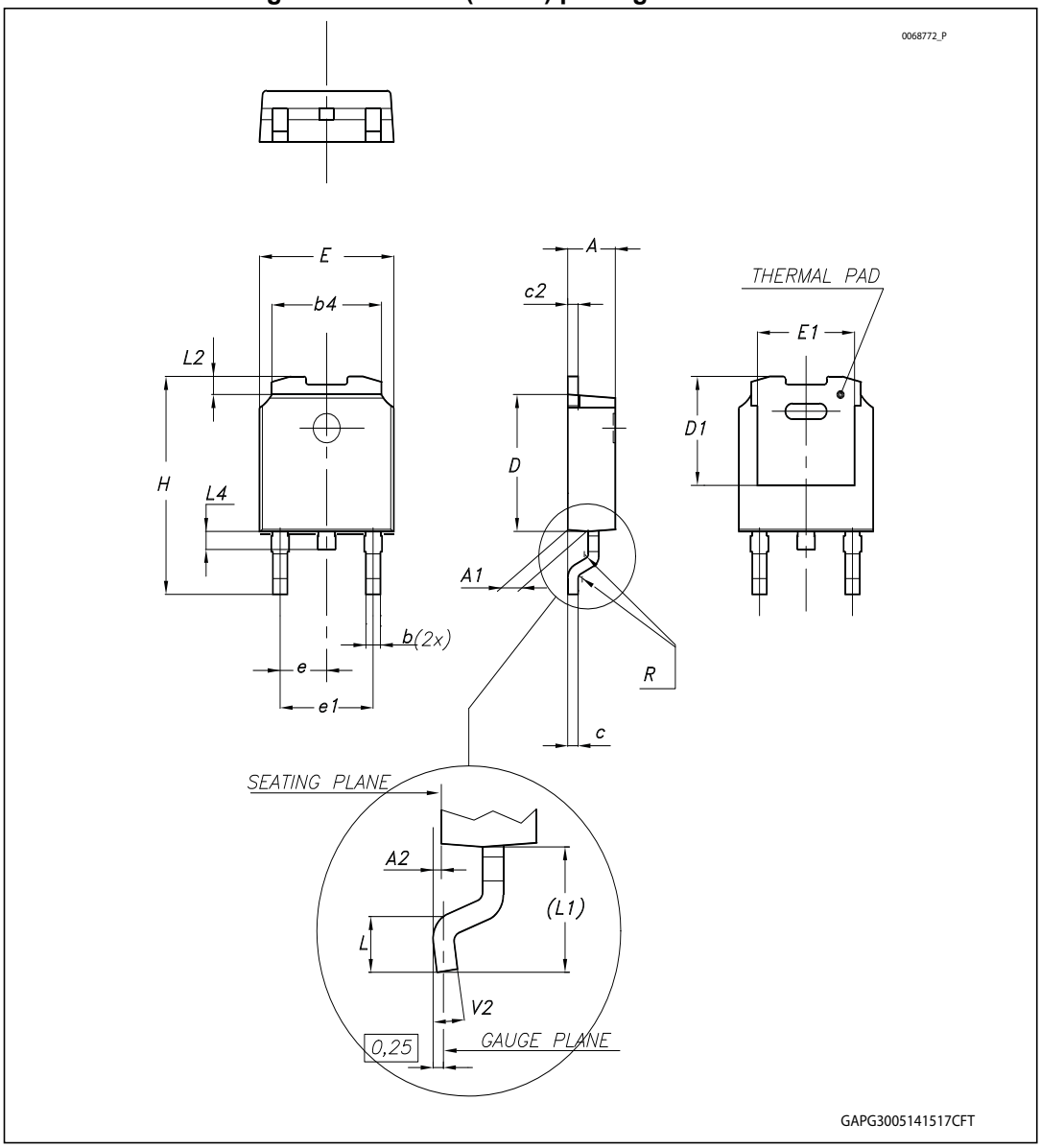


Table 6. TO-252 (DPAK) mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
B	0.64		0.90
B2	5.20		5.40
C	0.45		0.60
C2	0.48		0.60
D	6		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
G	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°	8°	
Package weight	Gr. 0.29		

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
29-Sep-2014	1	Initial release.