VN772K-E

QUAD SMART POWER SOLID STATE RELAY FOR COMPLETE H BRIDGE CONFIGURATIONS

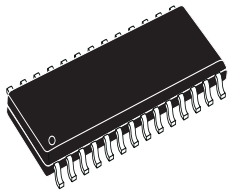
Table 1. General Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN772K-E	120mΩ (*)	9A (**)	36V

Note: (*) Total resistance of one side in bridge configuration
Note: (**) Typical current limitation value

- SUITED AS LOW VOLTAGE BRIDGE
- LINEAR CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- SHORT CIRCUIT PROTECTED
- DOUBLE STATUS FLAG DIAGNOSTIC (OPEN DRAIN)
- INTEGRATED CLAMPING CIRCUITS
- UNDERVOLTAGE PROTECTION
- ESD PROTECTION
- IN COMPLIANCE WITH THE 2002/95/EC EUROPEAN DIRECTIVE

Figure 1. Package



SO-28

DESCRIPTION

The VN772K-E is a device formed by three monolithic chips housed in a standard SO-28 package: a double high side and two low side switches. Both the double high side and low side switches are made using STMicroelectronics VIPower™ M0-3 Technology. This device is suitable to drive a DC motor in a bridge configuration as well as to be used as a quad switch for any low voltage application.

The high side switches have built-in thermal shutdown to protect the chips from overtemperature and current limiter blocks to protect the device from short circuit. Status output is provided to indicate open load in off and on state and overtemperature. The low side switches are two OMNIFET II types (fully autoprotected Power MOSFET in VIPower™ technology). They have built-in thermal shutdown, linear current limitation and overvoltage clamping. Fault feedback for thermal intervention can be detected by monitoring the voltage at the input pin.

Table 2. Order Codes

Package	Tube	Tape and Reel
SO-28	VN772K-E	VN772KTR-E

Figure 2. Block Diagram

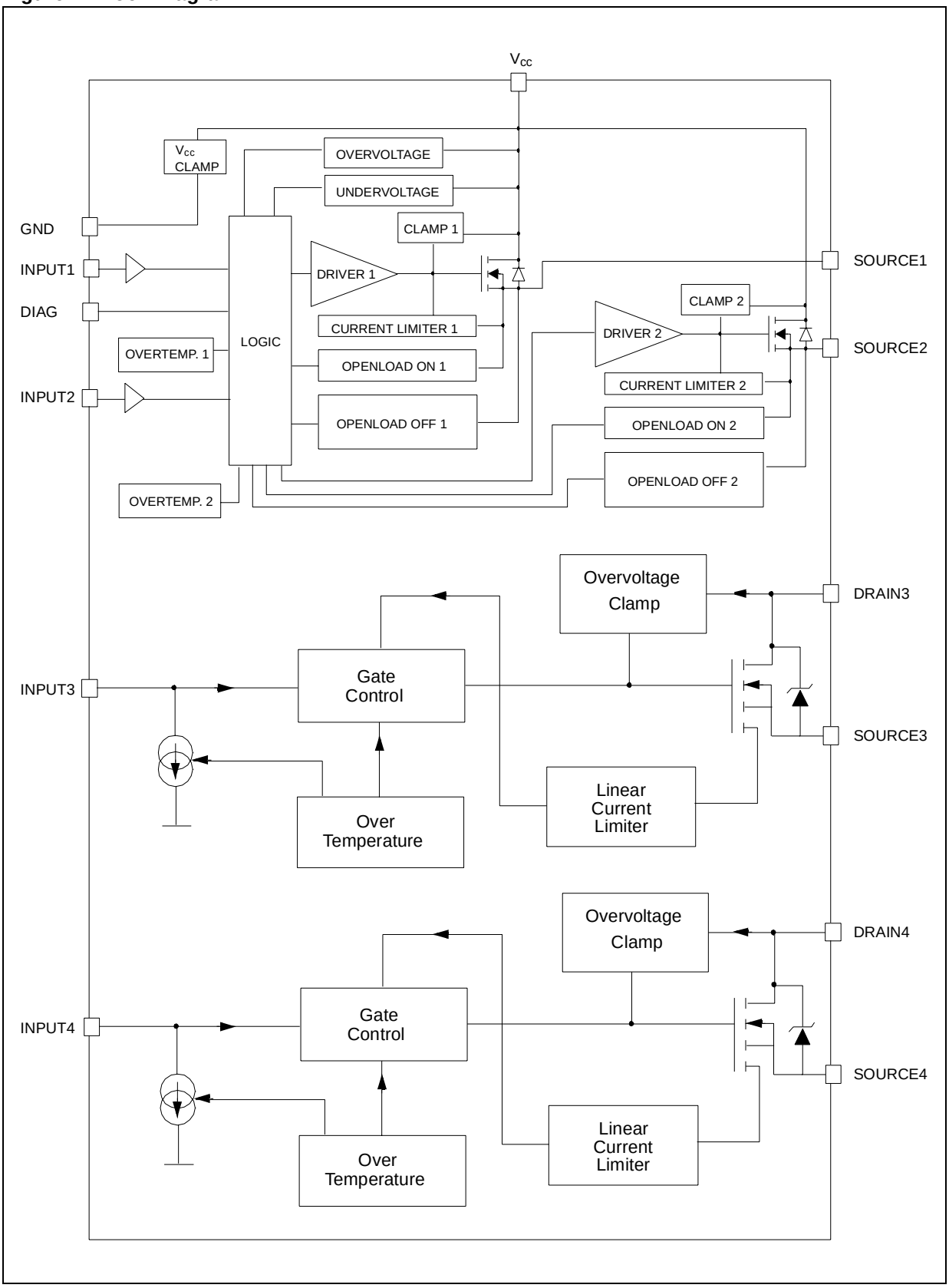


Table 3. Pin Function

No	NAME	FUNCTION
1, 3, 25, 28	DRAIN 3	Drain of Switch 3 (low-side switch)
2	INPUT 3	Input of Switch 3 (low-side switch)
4, 11	N.C.	Not Connected
5, 10, 19, 24	V_{CC}	Drain of Switches 1 and 2 (high-side switches) and Power Supply Voltage
6	GND	Ground of Switches 1 and 2 (high-side switches)
7	INPUT 1	Input of Switch 1 (high-side switches)
8	DIAGNOSTIC	Diagnostic of Switches 1 and 2 (high-side switches)
9	INPUT 2	Input of Switch 2 (high-side switch)
12, 14, 15, 18	DRAIN 4	Drain of switch 4 (low-side switch)
13	INPUT 4	Input of Switch 4 (low-side switch)
16, 17	SOURCE 4	Source of Switch 4 (low-side switch)
20, 21	SOURCE 2	Source of Switch 2 (high-side switch)
22, 23	SOURCE 1	Source of Switch 1 (high-side switch)
26, 27	SOURCE 3	Source of Switch 3 (low-side switch)

Figure 3. Configuration Diagram (Top View)

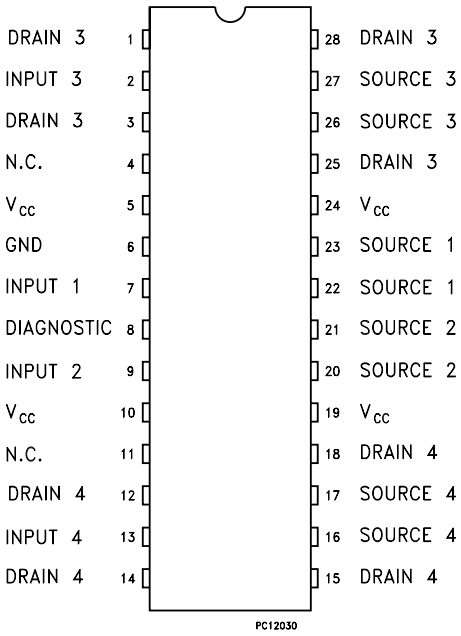


Table 4. Thermal Data

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case (High-side switch)	MAX	20	°C/W
$R_{thj\text{-}case}$	Thermal Resistance Junction-case (Low-side switch)	MAX	20	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	MAX	60	°C/W

ABSOLUTE MAXIMUM RATINGS

Table 5. Dual High Side Switch

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	41	V
- V_{CC}	Reverse DC Supply Voltage	- 0.3	V
- I_{GND}	DC Reverse Ground Pin Current	- 200	mA
I_{OUT}	DC Output Current	Internally Limited	A
- I_{OUT}	Reverse DC Output Current	- 6	A
I_{IN}	DC Input Current	+/- 10	mA
I_{STAT}	DC Status Current	+/- 10	mA
V_{ESD}	Electrostatic Discharge (Human Body Model: R=1.5KΩ; C=100pF) - INPUT - STATUS - OUTPUT - V_{CC}	 4000 4000 5000 5000	 V V V V
P_{tot}	Power Dissipation T_c=25°C	6	W
T_j	Junction Operating Temperature	Internally Limited	°C
T_c	Case Operating Temperature	- 40 to 150	°C
T_{stg}	Storage Temperature	- 55 to 150	°C

Table 6. Low Side Switch

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{IN}=0V)	Internally Clamped	V
V_{IN}	Input Voltage	Internally Clamped	V
I_{IN}	Input Current	+/-20	mA
$R_{IN\ MIN}$	Minimum Input Series Impedance	150	Ω
I_D	Drain Current	Internally Limited	A
I_R	Reverse DC Output Current	-10.5	A
V_{ESD1}	Electrostatic Discharge (R=1.5KΩ, C=100pF)	4000	V
V_{ESD2}	Electrostatic Discharge on output pin only (R=330Ω, C=150pF)	16500	V
P_{tot}	Power Dissipation (T_C=25°C)	6	W
T_j	Operating Junction Temperature	Internally limited	°C

ELECTRICAL CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH

(8V<V_{CC}<36V; -40°C< T_j <150°C, unless otherwise specified) (Per each channel)

Table 7. Power Outputs

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC} (1)	Operating Supply Voltage		5.5	13	36	V
V_{USD} (1)	Undervoltage Shut-down		3	4	5.5	V
V_{OV} (1)	Overvoltage Shut-down		36			V
$R_{DS(on)}$	On State Resistance	I_{OUT}=2A; T_j=25°C I_{OUT}=2A; V_{CC}>8V			60 120	mΩ mΩ
I_S (1)	Supply Current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V Off State; V_{CC}=13V; T_j =25°C; V_{IN}=V_{OUT}=0V On State; V_{CC}=13V		12 12 5	40 25 7	µA µA mA
$I_{L(off1)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=36V; T_j=125°C	0		50	µA
$I_{L(off2)}$	Off State Output Current	V_{IN}=0V; V_{OUT}=3.5V	-75		0	µA
$I_{L(off3)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =125°C			5	µA
$I_{L(off4)}$	Off State Output Current	V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j =25°C			3	µA

Note: (1) Per device.

Table 8. Switching (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	R_L=6.5Ω from V_{IN} rising edge to V_{OUT}=1.3V		30		µs
$t_{d(off)}$	Turn-off Delay Time	R_L=6.5Ω from V_{IN} falling edge to V_{OUT}=11.7V		30		µs
$dV_{OUT}/dt_{(on)}$	Turn-on Voltage Slope	R_L=6.5Ω from V_{OUT}=1.3V to V_{OUT}=10.4V		See relative diagram		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off Voltage Slope	R_L=6.5Ω from V_{OUT}=11.7V to V_{OUT}=1.3V		See relative diagram		V/µs

Table 9. Logic Input

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Level				1.25	V
I_{IL}	Low Level Input Current	V_{IN} = 1.25V	1			µA
V_{IH}	Input High Level		3.25			V
I_{IH}	High Level Input Current	V_{IN} = 3.25V			10	µA
$V_{I(hyst)}$	Input Hysteresis Voltage		0.5			V
V_{ICL}	Input Clamp Voltage	I_{IN} = 1mA I_{IN} = -1mA	6	6.8 -0.7	8	V V

Table 10. Status Pin

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{STAT}	Status Low Output Voltage	I_{STAT}= 1.6 mA			0.5	V
I_{LSTAT}	Status Leakage Current	Normal Operation; V_{STAT}= 5V			10	µA
C_{STAT}	Status Pin Input Capacitance	Normal Operation; V_{STAT}= 5V			100	pF
V_{SCL}	Status Clamp Voltage	I_{STAT}= 1mA I_{STAT}= - 1mA	6	6.8 -0.7	8	V V

ELECTRICAL CHARACTERISTICS FOR DUAL HIGH SIDE SWITCH (continued)

Table 11. Protections

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{TSD}	Shut-down Temperature		150	175	200	°C
T_R	Reset Temperature		135			°C
T_{hyst}	Thermal Hysteresis		7	15		°C
t_{SDL}	Status Delay in Overload Conditions	$T_j>T_{TSD}$			20	µs
I_{lim}	Current limitation	T_j=125°C 5.5V<V_{CC}<36V	6 8.5	9	15 15 15	A A A
V_{demag}	Turn-off Output Clamp Voltage	I_{OUT}=2A; L= 6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V

Table 12. Openload Detection

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{OL}	Openload ON State Detection Threshold	V_{IN}=5V	50	100	200	mA
$t_{DOL(on)}$	Openload ON State Detection Delay	I_{OUT}=0A			200	µs
V_{OL}	Openload OFF State Voltage Detection Threshold	V_{IN}=0V	1.5	2.5	3.5	V
$T_{DOL(off)}$	Openload Detection Delay at Turn Off				1000	µs

ELECTRICAL CHARACTERISTICS FOR LOW SIDE SWITCHES

(-40°C < T_j < 150°C, unless otherwise specified)

Table 13. Off

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CLAMP}	Drain-source Clamp Voltage	V_{IN}=0V; I_D=3.5A	40	45	55	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	V_{IN}=0V; I_D=2mA	36			V
V_{INTH}	Input Threshold Voltage	V_{DS}=V_{IN}; I_D=1mA	0.5		2.5	V
I_{ISS}	Supply Current from Input Pin	V_{DS}=0V; V_{IN}=5V		100	150	µA
V_{INCL}	Input-Source Clamp Voltage	I_{IN}=1mA I_{IN}=-1mA	6 -1.0	6.8	8 -0.3	V
I_{DSS}	Zero Input Voltage Drain Current (V_{IN}=0V)	V_{DS}=13V; V_{IN}=0V; T_j=25°C V_{DS}=25V; V_{IN}=0V			30 75	µA

Table 14. On

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$R_{DS(on)}$	Static Drain-source On Resistance	V_{IN}=5V; I_D=3.5A; T_j=25°C V_{IN}=5V; I_D=3.5A			60 120	mΩ

ELECTRICAL CHARACTERISTICS FOR LOW SIDE SWITCHES (continued)

(T_j=25°C, unless otherwise specified)

Table 15. Dynamic

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs} (*)	Forward Transconductance	V_{DD}=13V; I_D=3.5A		9		S
C_{OSS}	Output Capacitance	V_{DS}=13V; f=1MHz; V_{IN}=0V		220		pF

Table 16. Switching

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=15V; I_D=3.5A V_{gen}=5V; R_{gen}=$R_{IN\ MIN}$=150Ω		100	300	ns
t_r	Rise Time			470	1500	ns
$t_{d(off)}$	Turn-off Delay Time			500	1500	ns
t_f	Fall Time			350	1000	ns
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=15V; I_D=3.5A V_{gen}=5V; R_{gen}=2.2KΩ		0.75	2.3	µs
t_r	Rise Time			4.6	14.0	µs
$t_{d(off)}$	Turn-off Delay Time			5.4	16.0	µs
t_f	Fall Time			3.6	11.0	µs
$(dI/dt)_{on}$	Turn-on Current Slope	V_{DD}=15V; I_D=3.5A V_{gen}=5V; R_{gen}=$R_{IN\ MIN}$=150Ω		6.5		A/µs
Q_i	Total Input Charge	V_{DD}=12V; I_D=3.5A; V_{IN}=5V I_{gen}=2.13mA		18		nC

Table 17. Source Drain Diode

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD} (*)	Forward On Voltage	I_{SD}=3.5A; V_{IN}=0V		0.8		V
t_{rr}	Reverse Recovery Time	I_{SD}=3.5A; dI/dt=20A/µs V_{DD}=30V; L=200µH		220		ns
Q_{rr}	Reverse Recovery Charge			0.28		µC
I_{RRM}	Reverse Recovery Current			2.5		A

Note: (*) Pulsed: Pulse duration = 300µs, duty cycle 1.5%

Table 18. Protections (-40°C < T_j < 150°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	V_{IN}=5V; V_{DS}=13V V_{IN}=5V; V_{DS}=13V; T_j=125°C	6 6.5	9	12 12	A A
t_{dlim}	Step Response Current Limit	V_{IN}=5V; V_{DS}=13V		4.0		µs
T_{jsh}	Overtemperature Shutdown		150	175		°C
T_{jrs}	Overtemperature Reset		135			°C
I_{gf}	Fault Sink Current	V_{IN}= 5V; V_{DS}=13V; T_j=T_{jsh}		15		mA
E_{as}	Single Pulse Avalanche Energy	starting T_j=25°C; V_{DD}=24V V_{IN}=5V; R_{gen}=$R_{IN\ MIN}$=150Ω; L=24mH	200			mJ

DUAL HIGH-SIDE SWITCH

Figure 4. Switching Time Waveforms

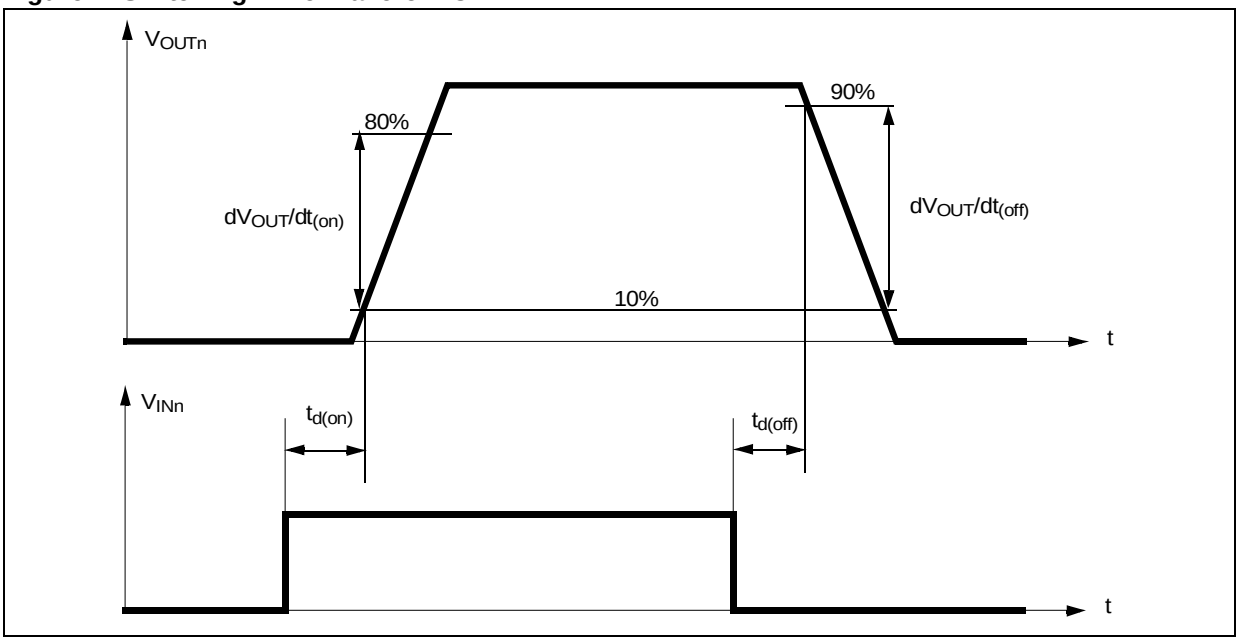


Table 19. Truth Table

CONDITIONS	INPUT	OUTPUT	STATUS
Normal Operation	L H	L H	H H
Current Limitation	L H H	L X X	H ($T_j < T_{TSD}$) H ($T_j > T_{TSD}$) L
Overtemperature	L H	L L	H L
Undervoltage	L H	L L	X X
Overvoltage	L H	L L	H H
Output Voltage > V_{OL}	L H	H H	L H
Output Current < I_{OL}	L H	L H	H L

Figure 5.

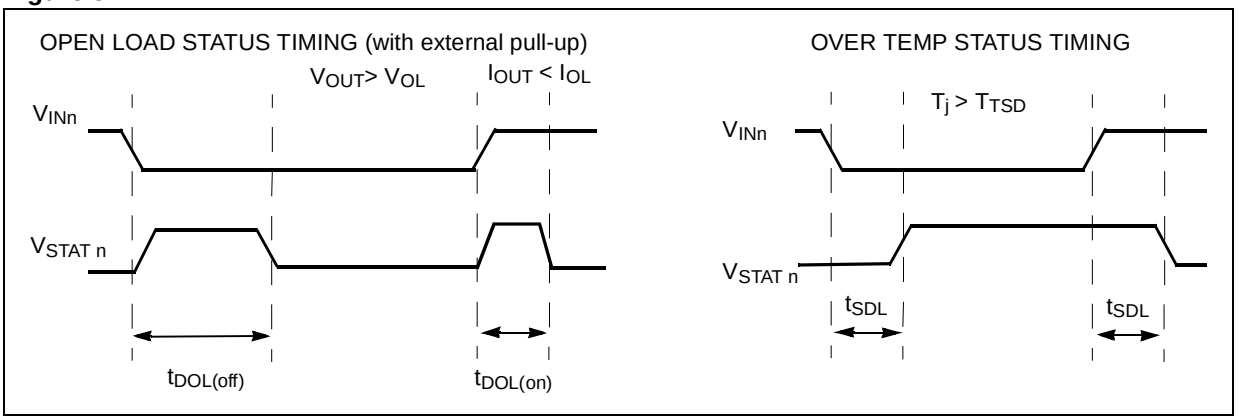


Figure 6. Typical Application Diagram

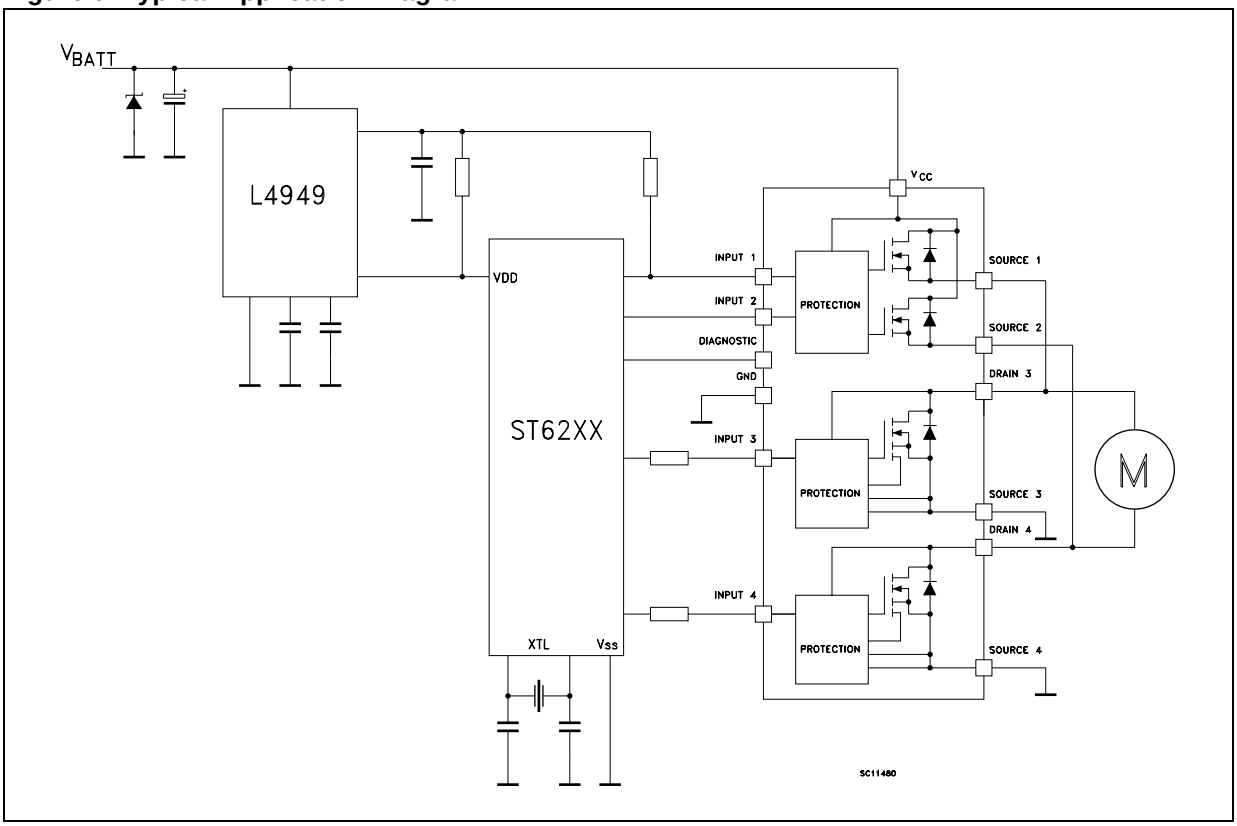
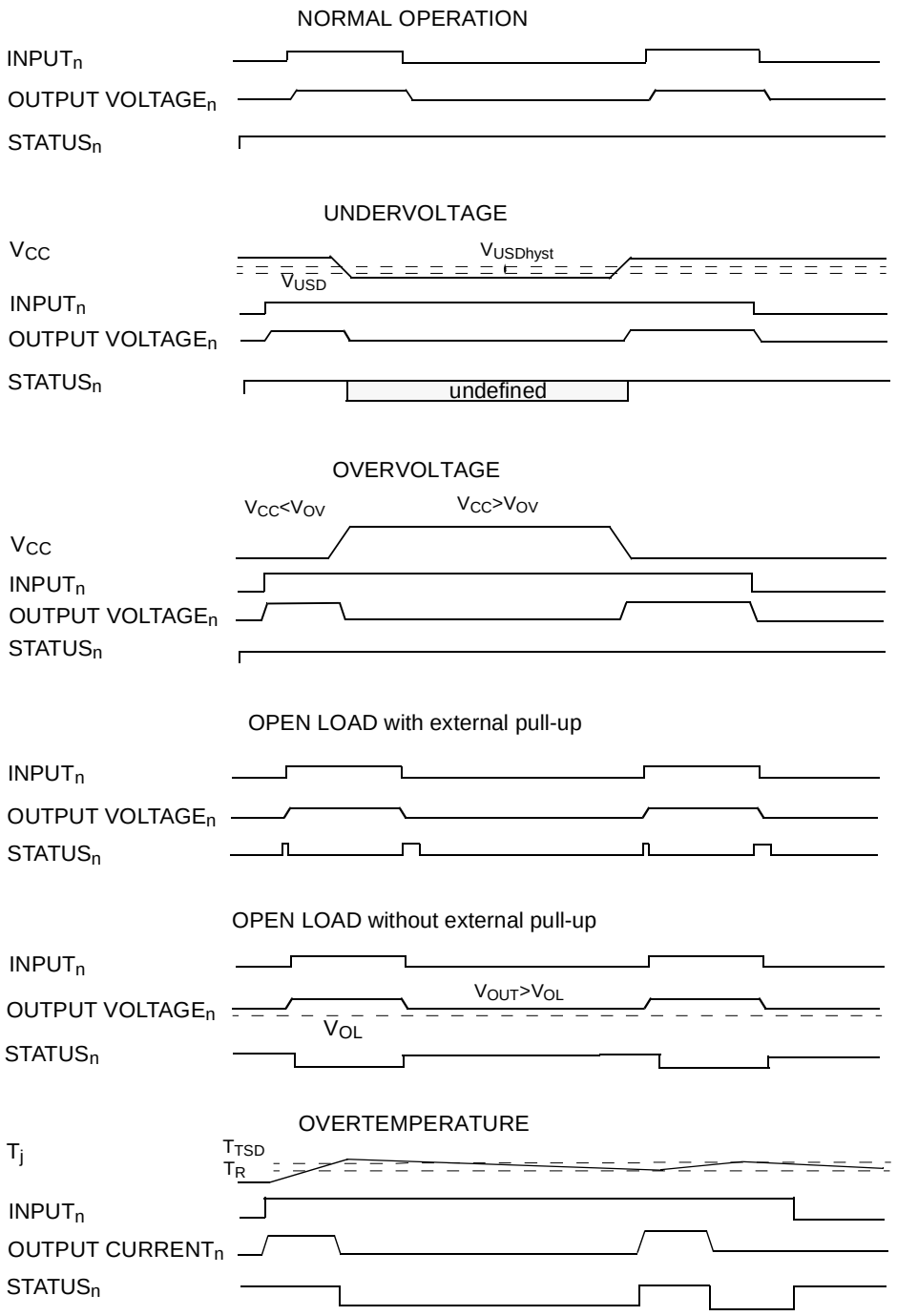


Figure 7. Waveforms



Electrical Characterization For Dual High Side Switch

Figure 8. Off State Output Current

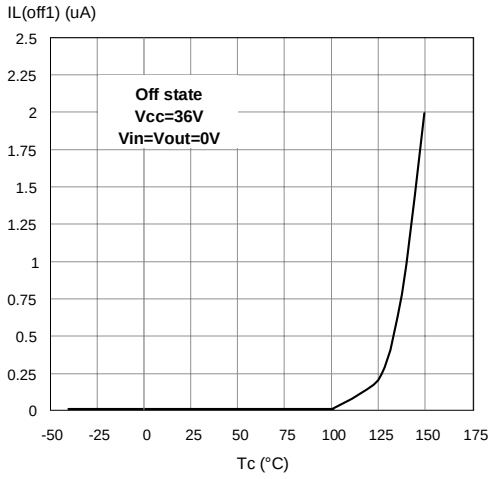


Figure 9. High Level Input Current

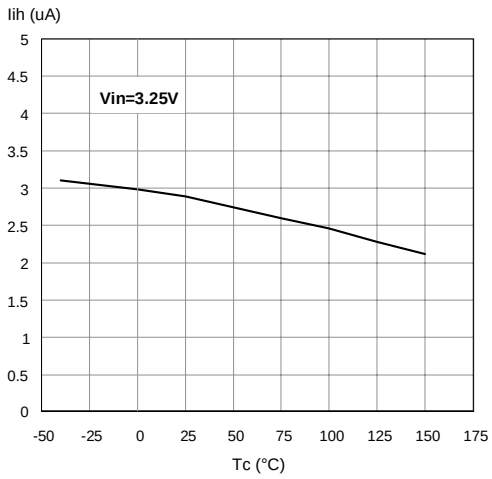


Figure 10. Input Low Level

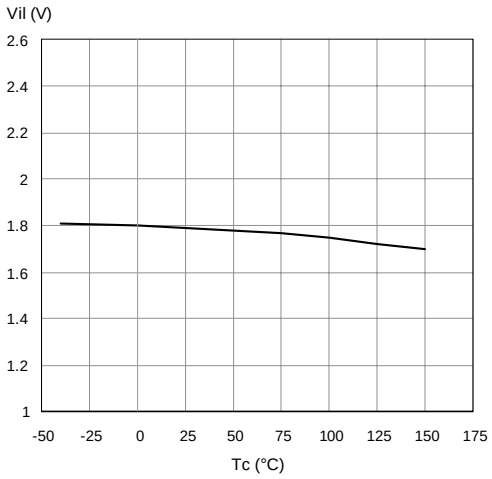


Figure 11. Input Clamp Voltage

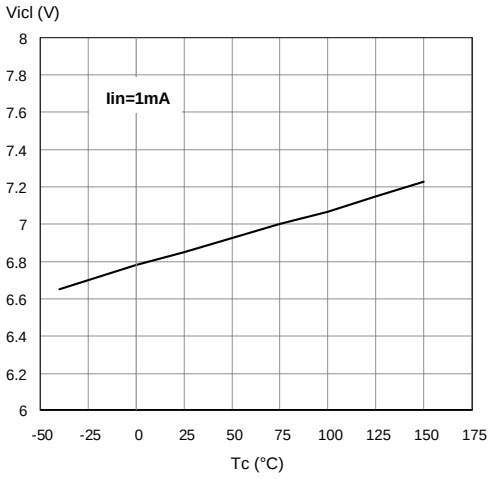


Figure 12. Input High Level

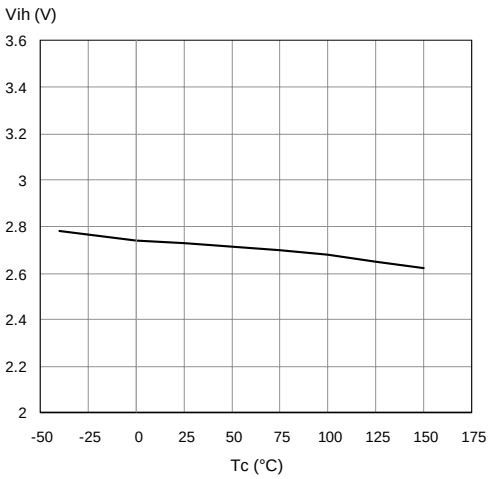
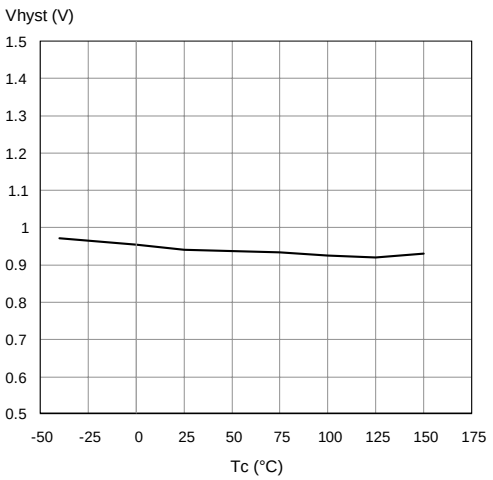


Figure 13. Input Hysteresis Voltage



Electrical Characterization For Dual High Side Switch (continued)

Figure 14. Overvoltage Shutdown

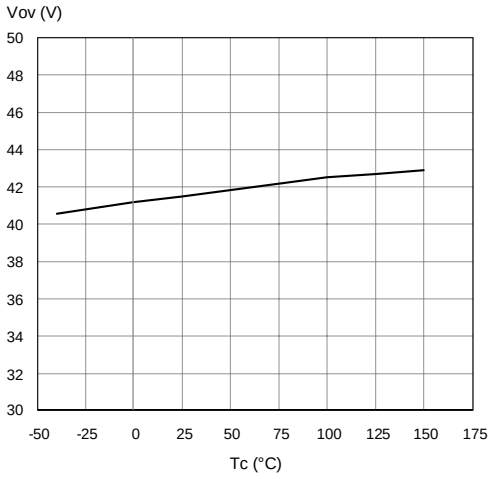


Figure 15. Turn-on Voltage Slope

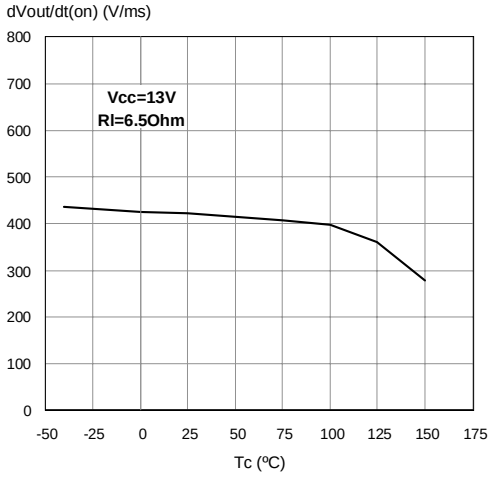


Figure 16. On State Resistance Vs T_{case}

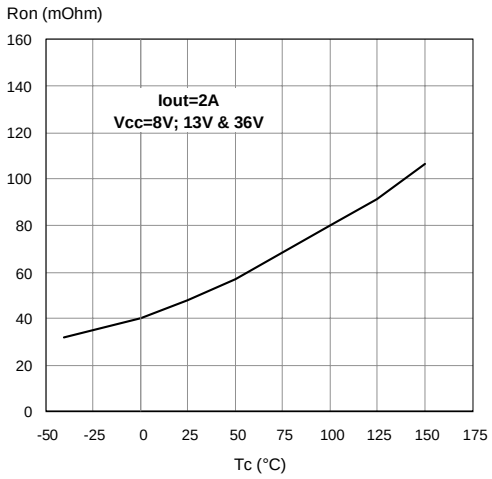


Figure 17. I_{LIM} Vs T_{case}

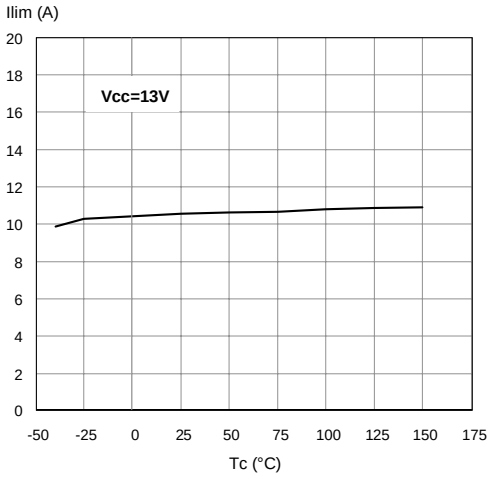


Figure 18. Turn-off Voltage Slope

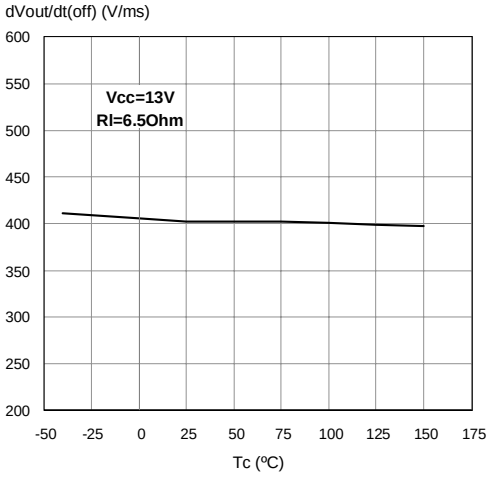
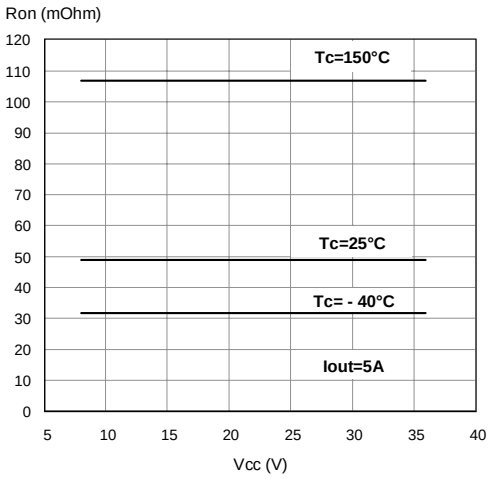


Figure 19. On State Resistance Vs V_{CC}



Electrical Characterization For Dual High Side Switch (continued)

Figure 20. Status Leakage Current

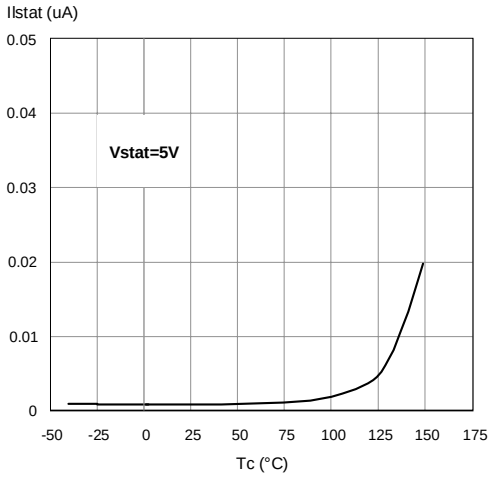


Figure 21. Openload On State Detection Threshold

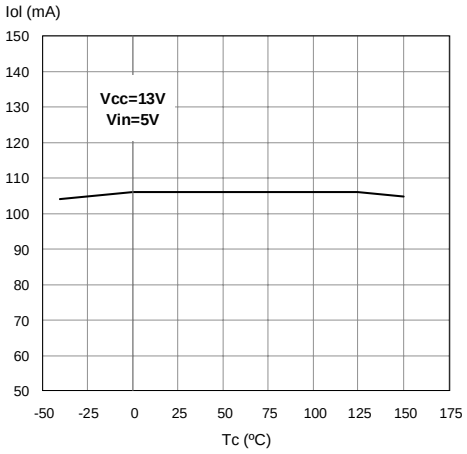


Figure 22. Status Clamp Voltage

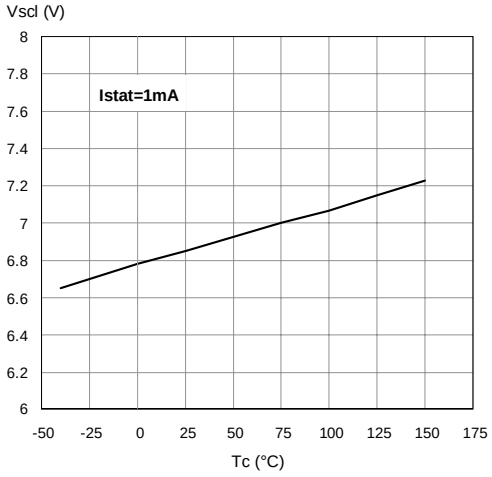


Figure 23. Status Low Output Voltage

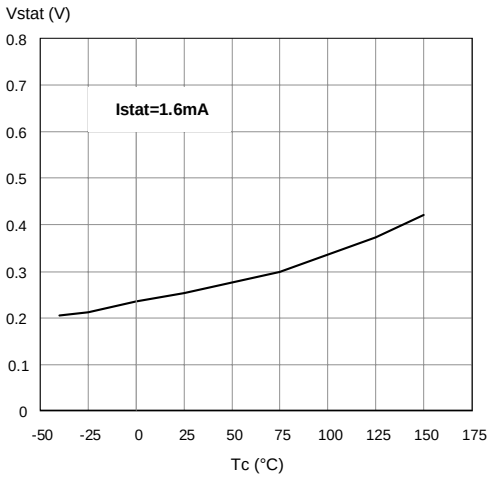
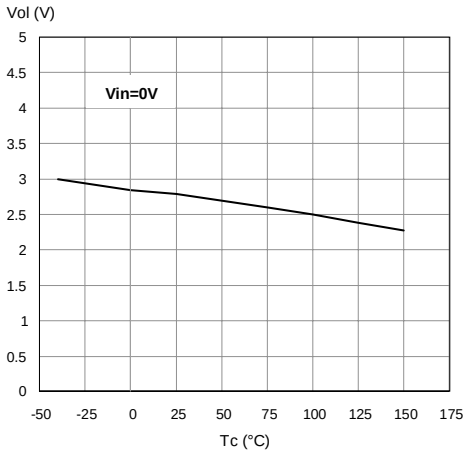


Figure 24. Openload Off State Voltage Detection Threshold



Electrical Characterization For Low Side Switches

Figure 25. Static Drain Source On Resistance

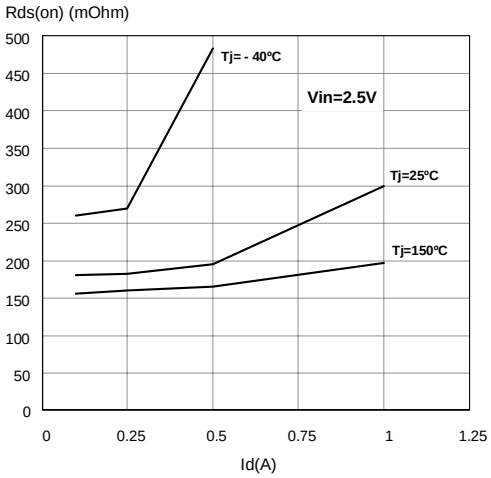


Figure 26. Transconductance

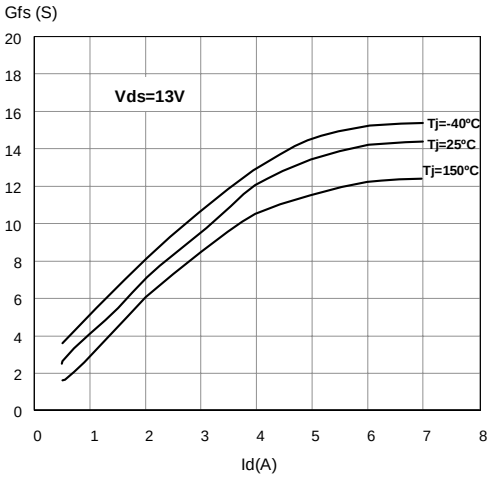


Figure 27. Turn On Current Slope

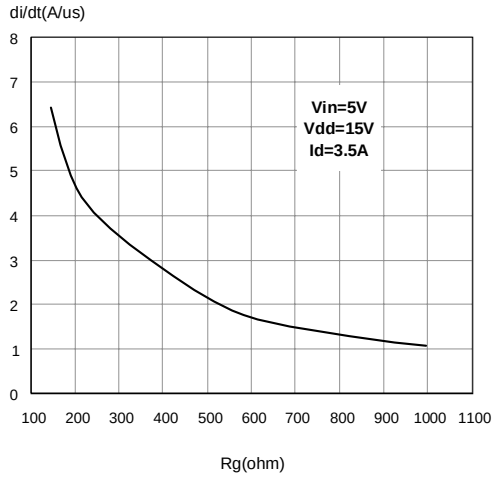


Figure 28. Derating Curve

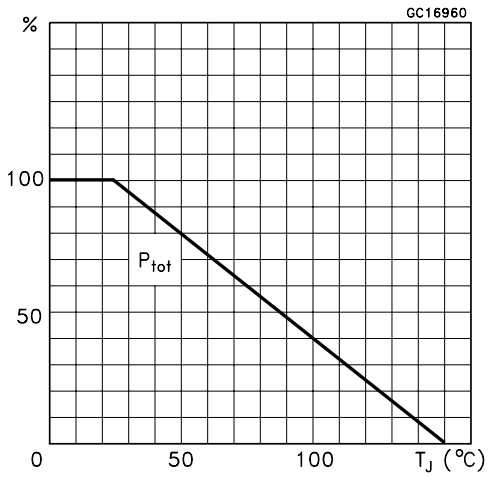


Figure 29. Transfer Characteristics

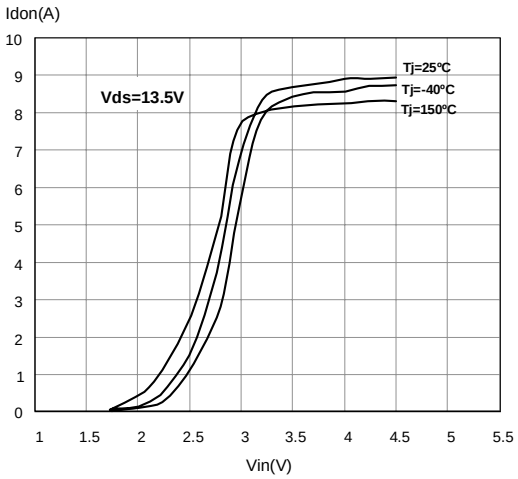
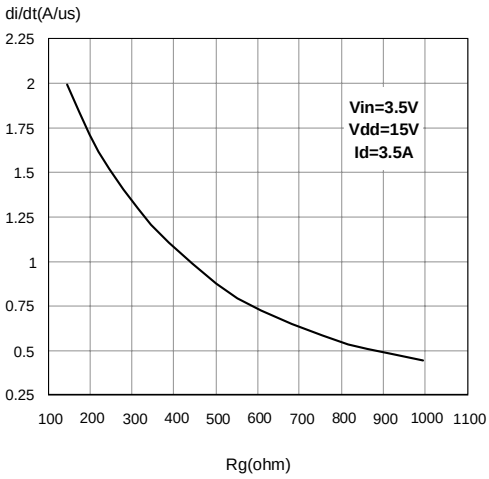


Figure 30. Turn On Current Slope



Electrical Characterization For Low Side Switches (continued)

Figure 31. Input Voltage Vs. Input Charge

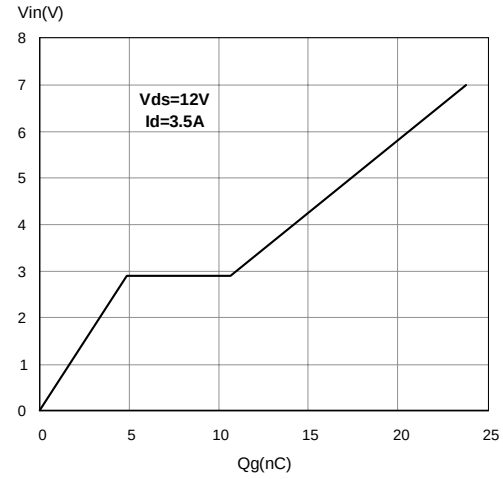


Figure 32. Switching Time Resistive Load

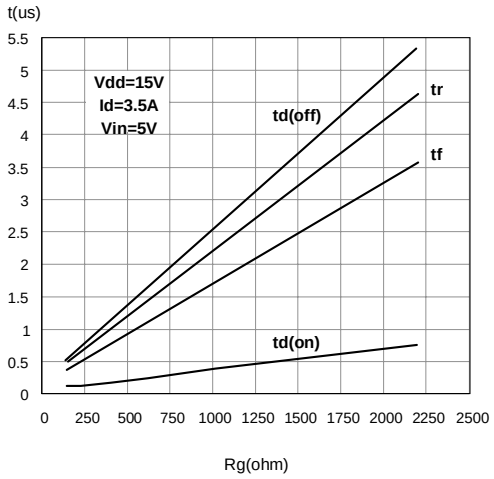


Figure 33. Output Characteristics

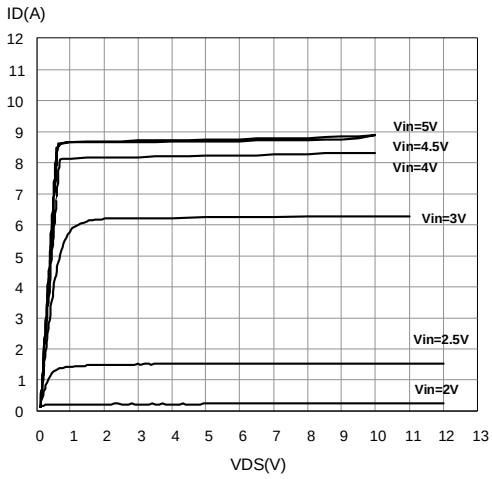


Figure 34. Capacitance Variations

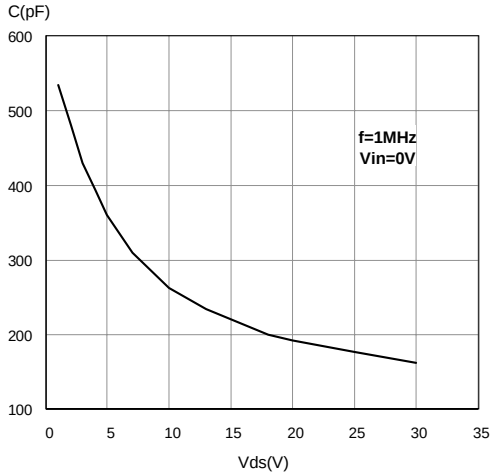


Figure 35. Switching Time Resistive Load

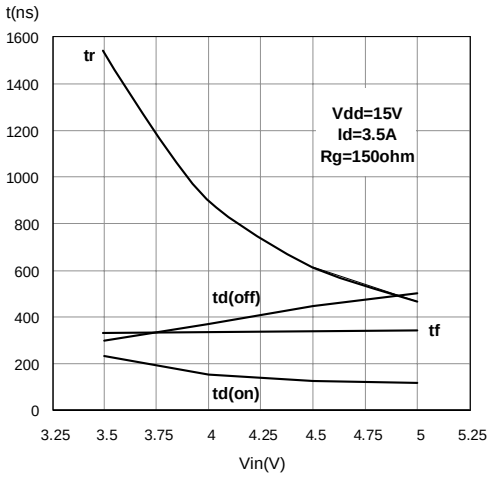
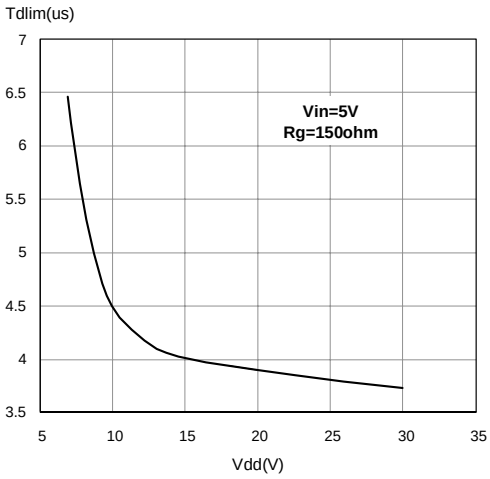


Figure 36. Step Response Current Limit



Electrical Characterization For Low Side Switches (continued)

Figure 37. Source-Drain Diode Forward Characteristics

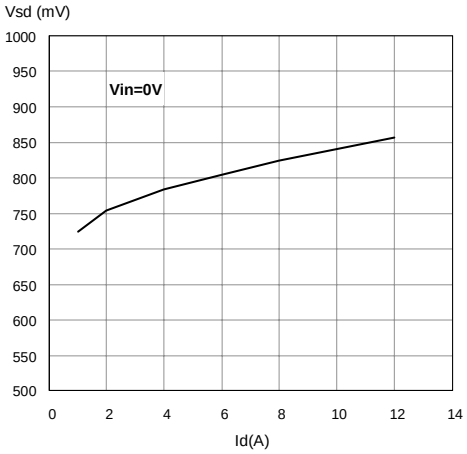


Figure 38. Static Drain-Source On resistance Vs. Input Voltage

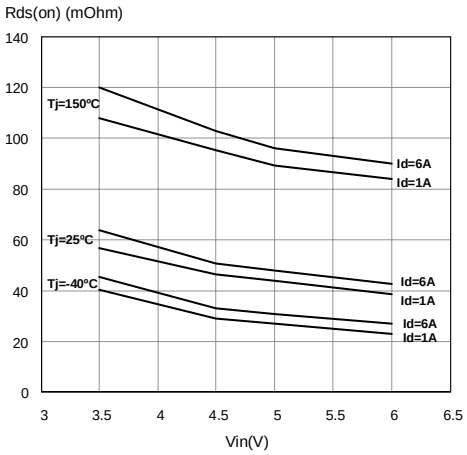


Figure 39. Normalized Input Threshold Voltage Vs. Temperature

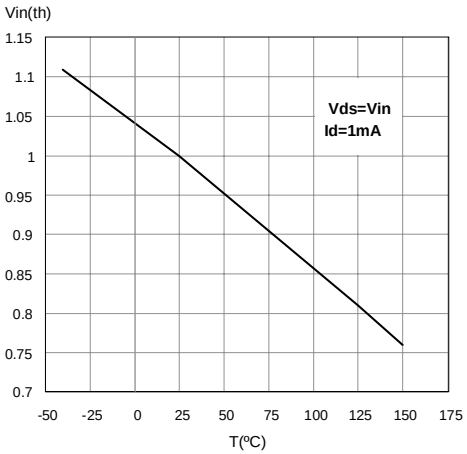


Figure 40. Static Drain-Source On Resistance Vs. Id

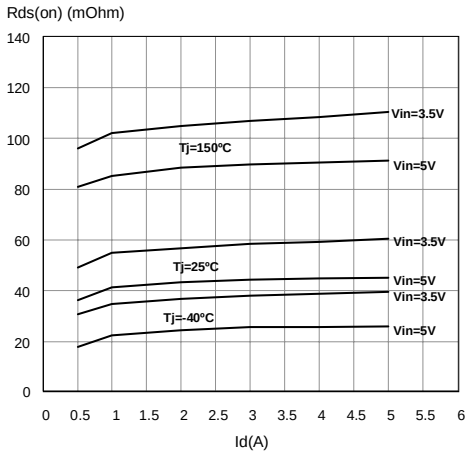


Figure 41. Static Drain-Source On resistance Vs. Input Voltage

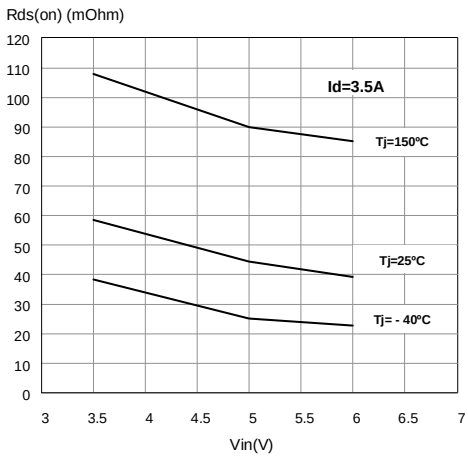
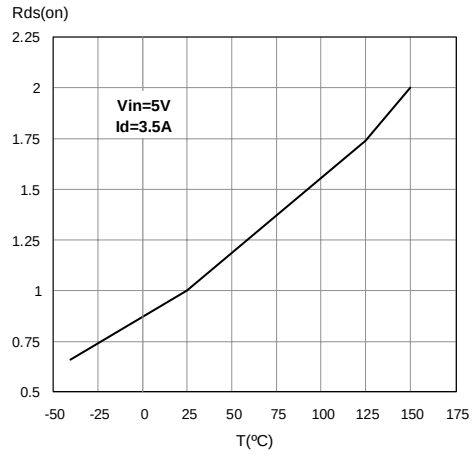


Figure 42. Normalized On Resistance Vs. Temperature



Electrical Characterization For Low Side Switches (continued)

Figure 43. Turn off drain source voltage slope

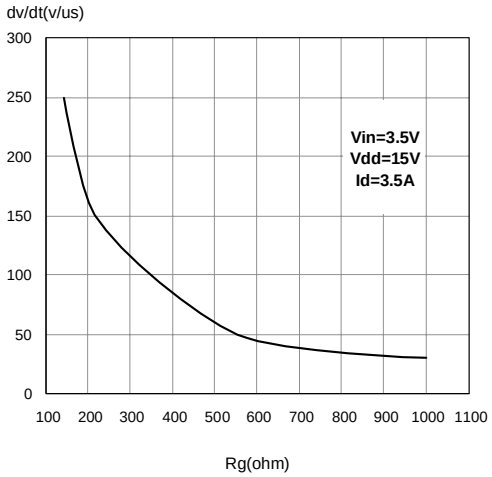


Figure 44. Current Limit Vs. Junction Temperature

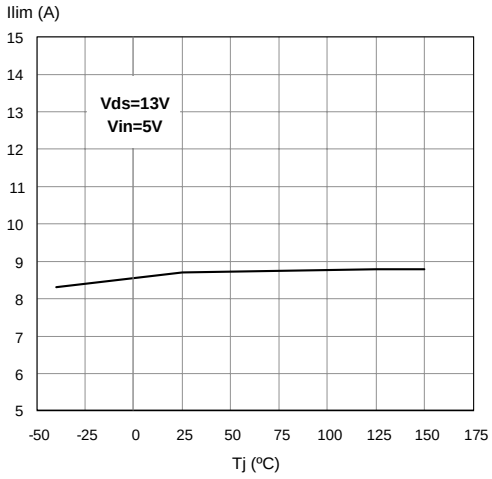


Figure 45. Turn off drain source voltage slope

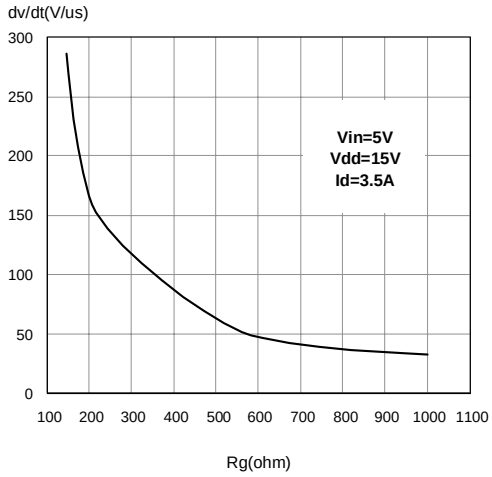


Table 20. SO-28 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A			2.65
a1	0.10		0.30
b	0.35		0.49
b1	0.23		0.32
C		0.50	
c1		45° (typ.)	
D	17.7		18.1
E	10.00		10.65
e		1.27	
e3		16.51	
F	7.40		7.60
L	0.40		1.27
S		8° (max.)	

Figure 46. SO-28 Package Dimensions

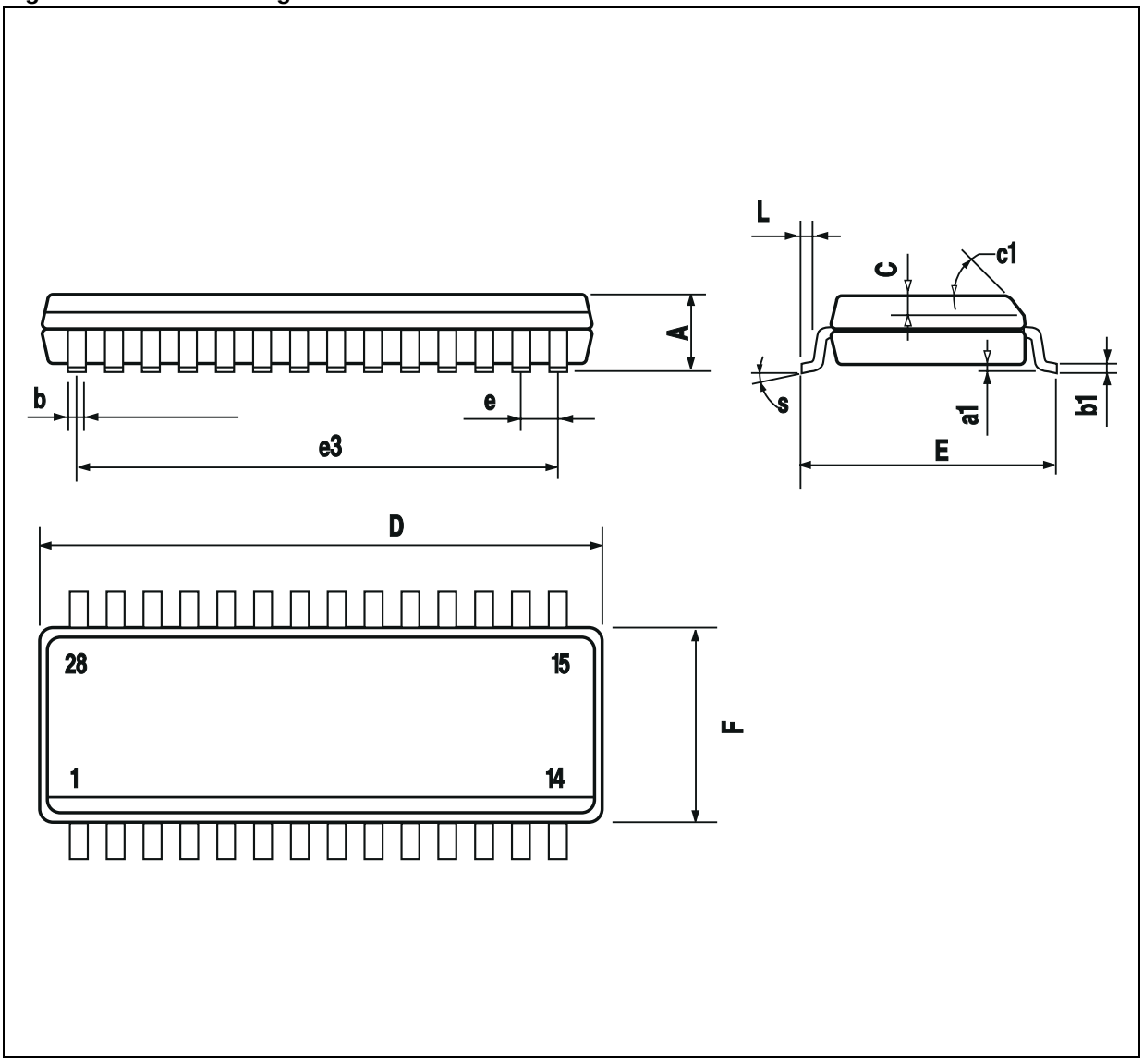
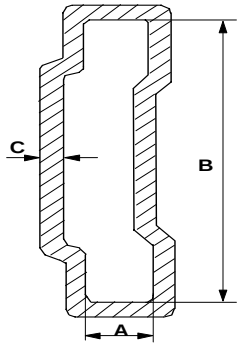


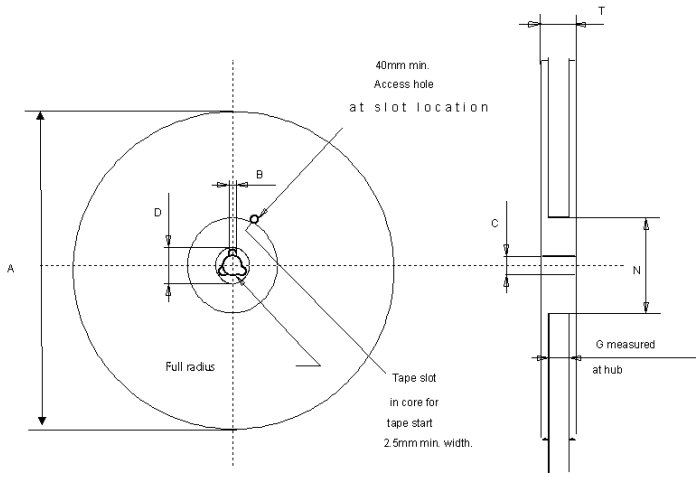
Figure 47. SO-28 Tube Shipment (No Suffix)



Base Q.ty	28
Bulk Q.ty	700
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 48. Tape And Reel Shipment (Suffix "TR")



REEL DIMENSIONS

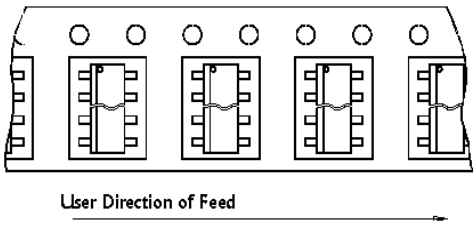
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

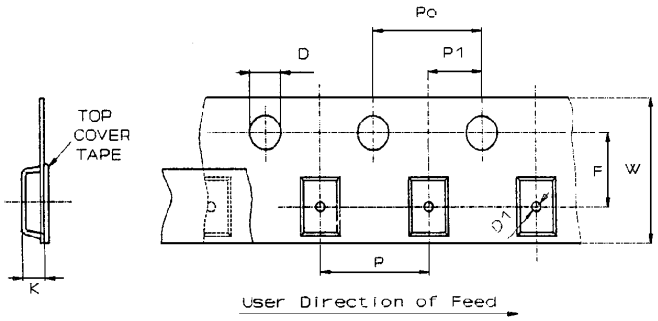
TAPE DIMENSIONS

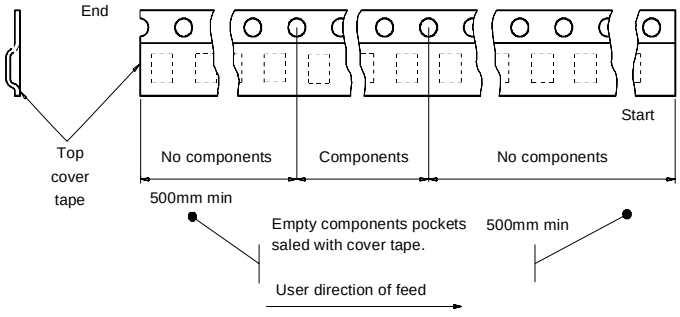
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	**W**	16
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	7.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







REVISION HISTORY

Date	Revision	Description of Changes
Sep. 2004	1	- First Issue.