Small Signal MOSFET

60 V, 310 mA, Single, N-Channel, SOT-23

Features

- Low R_{DS(on)}
- Small Footprint Surface Mount Package
- Trench Technology
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

MAXIMUM RATINGS ($T_J = 25^{\circ}C$ unless otherwise stated)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage		V _{DSS}	60	V
Gate-to-Source Voltage		V _{GS}	±20	V
Drain Current (Note 1) Steady State t < 5 s	$T_A = 25^{\circ}C$ $T_A = 85^{\circ}C$ $T_A = 25^{\circ}C$ $T_A = 85^{\circ}C$	I _D	260 190 310 220	mA
Power Dissipation (Note 1) Steady State t < 5 s		P _D	300 420	mW
Pulsed Drain Current (t _p = 10 μ	I _{DM}	1.2	Α	
Operating Junction and Storag Temperature Range	T _J , T _{STG}	-55 to +150	°C	
Source Current (Body Diode)	I _S	300	mA	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{ heta JA}$	417	°C/W
Junction-to-Ambient - t ≤ 5 s (Note 1)	$R_{\theta JA}$	300	

Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces)



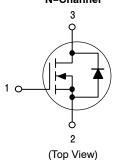
ON Semiconductor®

http://onsemi.com

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX (Note 1)		
60 V	3.0 Ω @ 4.5 V	310 mA		
	2.5 Ω @ 10 V			

Simplified Schematic

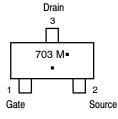
N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23 CASE 318 STYLE 21



703 = Device Code M = Date Code

■ = Pb-Free Package (Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]		
2N7002ET1G	SOT-23 (Pb-Free)	3000/Tape & Reel		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Units
OFF CHARACTERISTICS				•			•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				75		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V,	T _J = 25°C			1	μΑ
		V _{DS} = 60 V	T _J = 125°C			500	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V	/ _{GS} = ±20 V			±100	nA
ON CHARACTERISTICS (Note 2)				•			
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$	I _D = 250 μA	1.0		2.5	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J				4.4		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V,	I _D = 240 mA		0.86	2.5	Ω
		V _{GS} = 4.5 V	⁷ , I _D = 50 mA		1.1	3.0	1
Forward Transconductance	9FS	V _{DS} = 5 V, I _D = 200 mA			530		mS
CHARGES AND CAPACITANCES		•		•	•		•
Input Capacitance	C _{ISS}	$V_{GS} = 0 \text{ V, f} = 1 \text{ MHz,}$ $V_{DS} = 25 \text{ V}$			26.7	40	pF
Output Capacitance	C _{OSS}				4.6]
Reverse Transfer Capacitance	C _{RSS}				2.9		1
Total Gate Charge	Q _{G(TOT)}				0.81		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 5 V, V _{DS} = 10 V;			0.31		1
Gate-to-Source Charge	Q _{GS}		40 mA		0.48		
Gate-to-Drain Charge	Q_{GD}				0.08		
SWITCHING CHARACTERISTICS, V _{GS}	= V (Note 3)			•			
Turn-On Delay Time	t _{d(ON)}				1.7		ns
Rise Time	t _r	V_{GS} = 10 V, V_{DD} = 30 V, I_D = 200 mA, R_G = 10 Ω			1.2		
Turn-Off Delay Time	t _{d(OFF)}				4.8		
Fall Time	t _f				3.6		
DRAIN-SOURCE DIODE CHARACTER	STICS	•			-		-
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V,	T _J = 25°C		0.79	1.2	V
		I _S = 200 mA			0.7		1

Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%
 Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

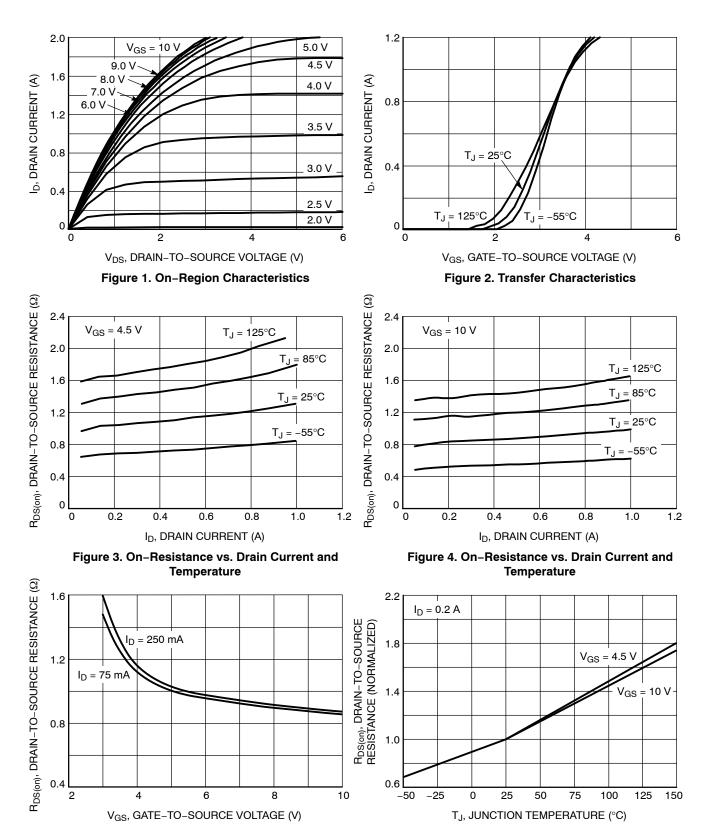


Figure 5. On-Resistance vs. Gate-to-Source Voltage

Figure 6. On–Resistance Variation with Temperature

TYPICAL CHARACTERISTICS

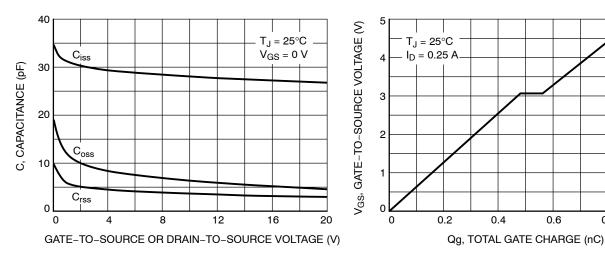


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

0.6

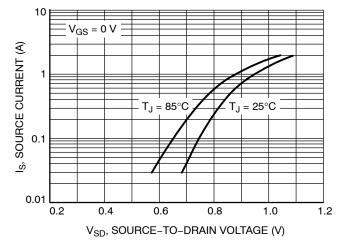
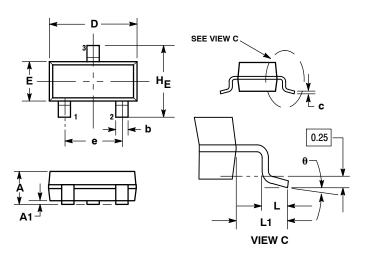


Figure 9. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 **ISSUE AP**



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH,
- PROTRUSIONS, OR GATE BURRS

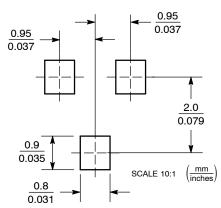
	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
Α	0.89	1.00	1.11	0.035	0.040	0.044	
A1	0.01	0.06	0.10	0.001	0.002	0.004	
b	0.37	0.44	0.50	0.015	0.018	0.020	
С	0.09	0.13	0.18	0.003	0.005	0.007	
D	2.80	2.90	3.04	0.110	0.114	0.120	
E	1.20	1.30	1.40	0.047	0.051	0.055	
е	1.78	1.90	2.04	0.070	0.075	0.081	
L	0.10	0.20	0.30	0.004	0.008	0.012	
L1	0.35	0.54	0.69	0.014	0.021	0.029	
HE	2.10	2.40	2.64	0.083	0.094	0.104	
θ	0°		10°	0°		10°	

STYLE 21:

PIN 1. GATE

- SOURCE 2.
- DRAIN

SOLDERING FOOTPRINT



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