

Description

The VN751S is a monolithic device developed using STMicroelectronics' VIPower technology, intended to drive any kind of load with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protect the device against overload. The device automatically turns off in case of ground pin disconnection. This device is especially suitable for industrial applications in conformity with IEC 61131-2 programmable controller international standard.

Features

- $R_{DS(on)}$: 60 m Ω
- I_{OUT} : 2.5 A
- V_{CC} : 36 V
- CMOS compatible input
- Thermal shutdown
- Shorted load protection
- Undervoltage and overvoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV
- Open drain status output
- Fast demagnetization of inductive loads

Table 1. Device summary

Order code	Package	Packing
VN751S	SO-8	Tube
VN751STR		Tape and reel

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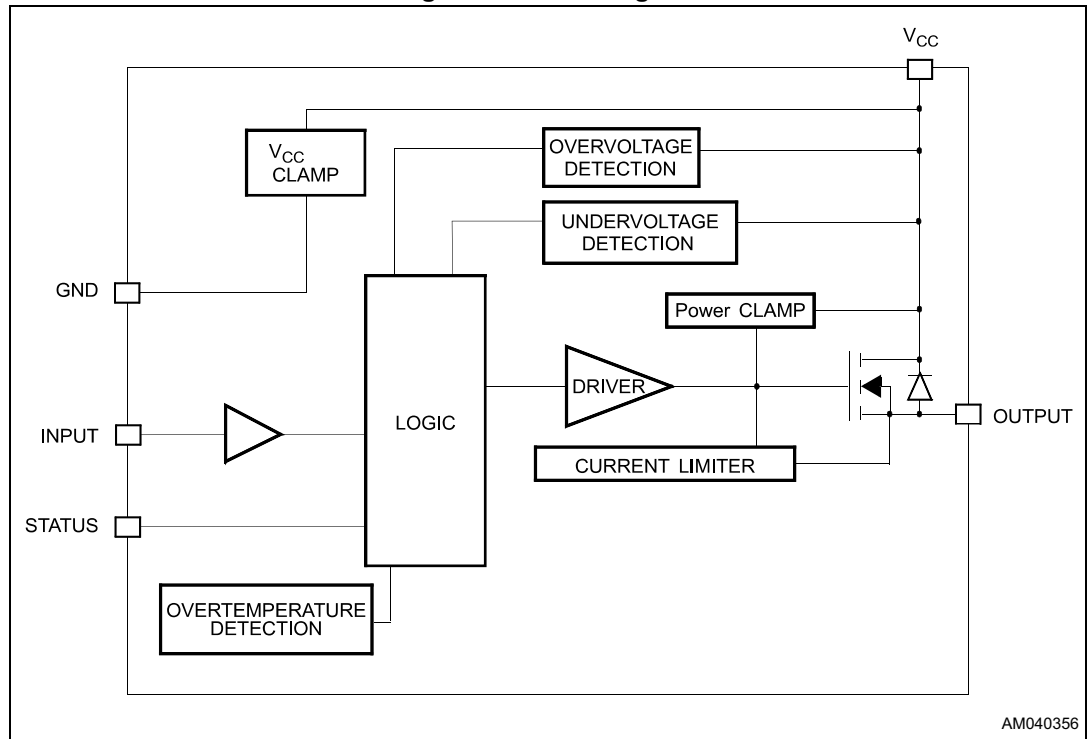
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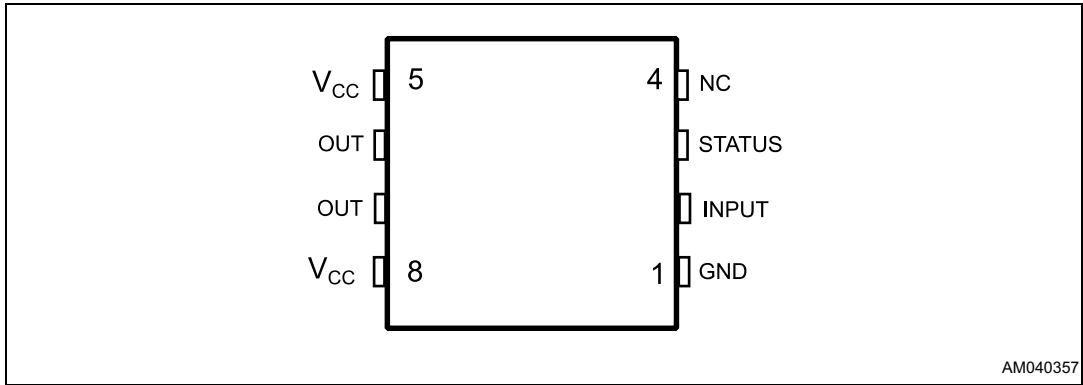
1 Block diagram

Figure 1. Block diagram



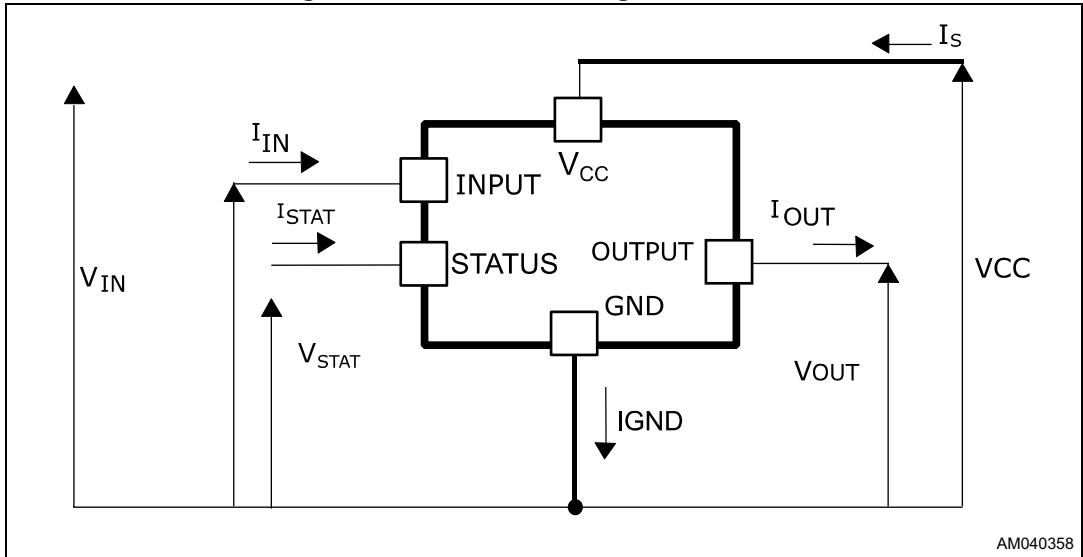
2 Pin connection

Figure 2. Connection diagram (top view)



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Figure 3. Current and voltage conventions



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3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	45	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-5	A
I_{IN}	DC input current	-1 to +10	mA
I_{STAT}	DC status current	-1 to +10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 k Ω ; C = 100 pF)	5000	V
E_{AS}	Single pulse avalanche energy ($T_{amb} = 125\text{ }^{\circ}\text{C}$, $V_{CC} = 24\text{ V}$, $I_{load} = 2.0\text{ A}$)	650	mJ
P_{TOT}	Power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	Internally limited	W
T_J	Junction operating temperature	Internally limited	$^{\circ}\text{C}$
T_C	Case operating temperature	-40 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature	-55 to 150	$^{\circ}\text{C}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	Max. 15	$^{\circ}\text{C}/\text{W}$
$R_{th(JA)}$	Thermal resistance junction-ambient	Max. 93 ⁽¹⁾	$^{\circ}\text{C}/\text{W}$
		82 ⁽²⁾	

1. When mounted on a standard single-sided FR-4 board with 0.5 cm² of Cu (at least 35 μm) thick connected to all VCC pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 2 cm² of Cu (at least 35 μm) thick connected to all VCC pins. Horizontal mounting and no artificial air flow.

4 Electrical characteristics

8 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Supply voltage	-	5.5	-	36	V
R _{DS(on)}	On-state resistance	I _{OUT} = 2 A at T _J = 25 °C	-	60	-	mΩ
		I _{OUT} = 2 A	-	-	180	
I _S ⁽¹⁾	Supply current	Off-state, V _{CC} = 24 V, T _J = 25 °C	-	10	20	μA
		On-state, V _{CC} = 24 V, T _J = 25 °C	-	3.5	-	mA
		On-state, V _{CC} = 24 V, T _J = 100 °C	-	-	3.8	mA
V _{USD}	Undervoltage shutdown	-	3	4	5.5	V
V _{OV}	Overvoltage shutdown	-	36	-	-	V
I _{L(off)}	Off-state output current	V _{IN} = V _{OUT} = 0 V	0	-	10	μA

1. Status: floating.

Table 5. Switching (V_{CC} = 24 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(ON)}	Turn-on delay time	R _L = 12 Ω from V _{IN} rising edge to V _{OUT} = 2.4 V	-	12	-	μs
t _{d(OFF)}	Turn-off delay time of output current	R _L = 12 Ω from V _{IN} falling edge to V _{OUT} = 21.6 V	-	35	-	μs
dV _{OUT} /dt _(on)	Turn -on voltage slope	R _L = 12 Ω from V _{OUT} = 2.4 V to V _{OUT} = 19.2 V	-	0.80	-	V/μs
dV _{OUT} /dt _(off)	Turn -off voltage slope	R _L = 12 Ω from V _{OUT} = 21.6 V to V _{OUT} = 2.4 V	-	0.30	-	

Table 6. Input pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{IL}	Input low level	-	-	-	1.25	V
I _{IL}	Low level input current	V _{IN} = 1.25 V	1	-	-	μA
V _{IH}	Input high level	-	3.25	-	-	V
I _{IH}	High level input current	V _{IN} = 3.25 V	-	-	10	μA
V _{hyst}	Input hysteresis voltage	-	0.5	-	-	V
I _{IN}	Input current	V _{IN} = V _{CC} = 5 V	-	-	10	μA
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	6	6.8	8	V
		I _{IN} = -1 mA	-	-0.7	-	

Table 7. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6 \text{ mA}$	-	-	0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5 \text{ V}$	-	-	10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5 \text{ V}$	-	-	100	fF
I_{IH}	High level input current	$V_{IN} = 3.25 \text{ V}$	-	-	10	μA
V_{SCL}	Status clamp voltage	$I_{STAT} = 1 \text{ mA}$	6	6.8	8	V
		$I_{STAT} = -1 \text{ mA}$	-	-0.7	-	

Table 8. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{demag}	Turn-off output clamp voltage	$R_L = 12 \Omega$; $L = 6 \text{ mH}$	$V_{CC} - 47$	$V_{CC} - 52$	$V_{CC} - 57$	V
T_{TSD}	Shutdown temperature	-	150	175	200	$^{\circ}\text{C}$
I_{lim}	Current limitation	$V_{CC} = 24 \text{ V}$; $R_{LOAD} = 10 \text{ m}\Omega$, $t = 0.4 \text{ ms}$	2.7	-	6.0	A
T_{hyst}	Thermal hysteresis	-	7	20	-	$^{\circ}\text{C}$
T_R	Reset temperature	-	135	-	-	$^{\circ}\text{C}$

5 Test circuits

Figure 4. Peak short-circuit current

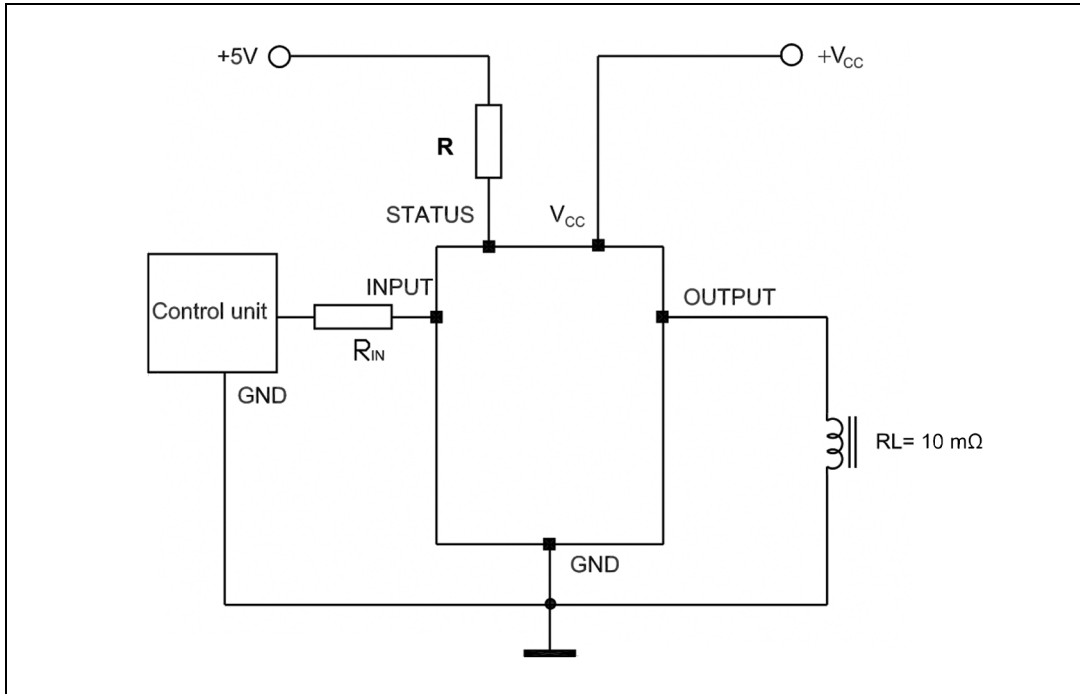
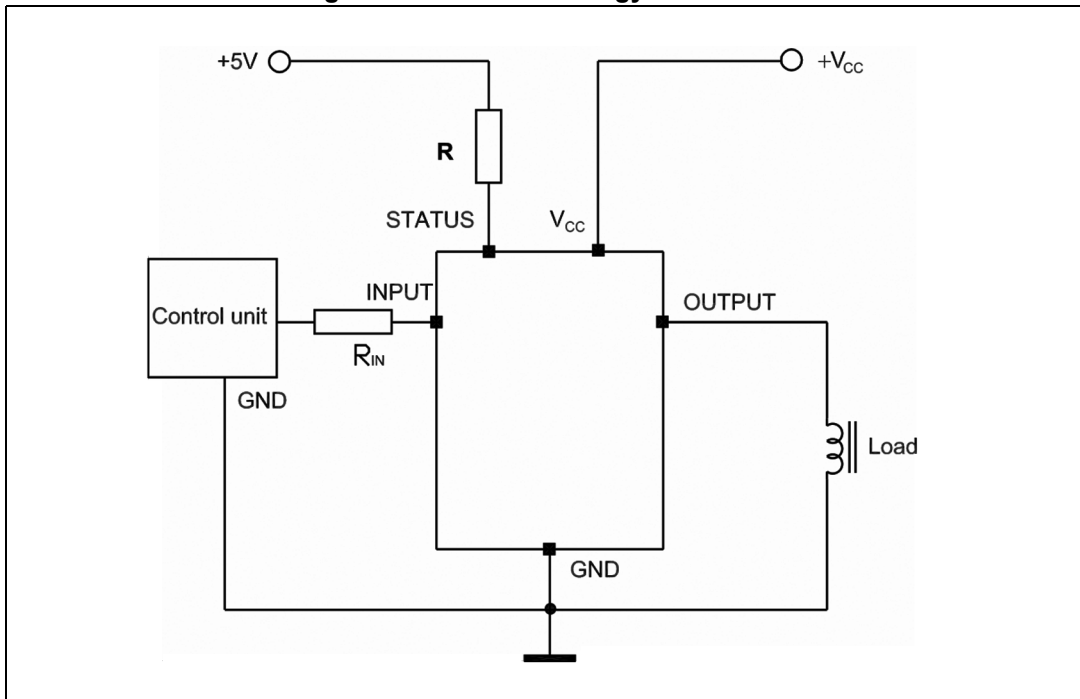


Figure 5. Avalanche energy test circuit



6 Switching time waveforms and truth table

Figure 6. Switching time waveforms

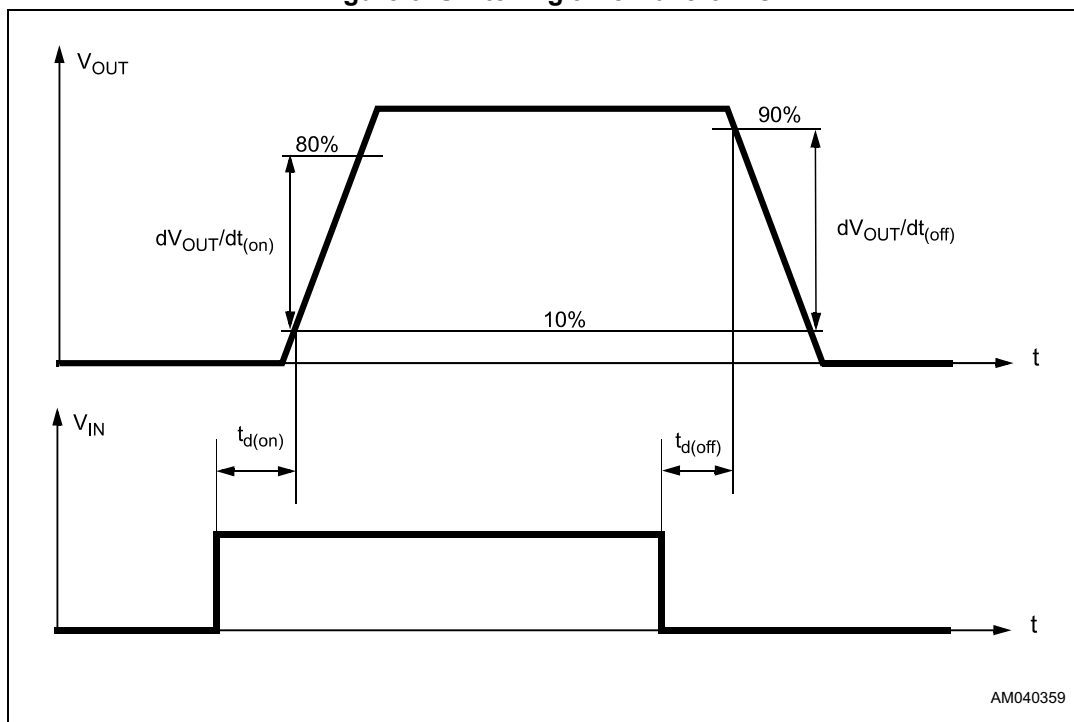
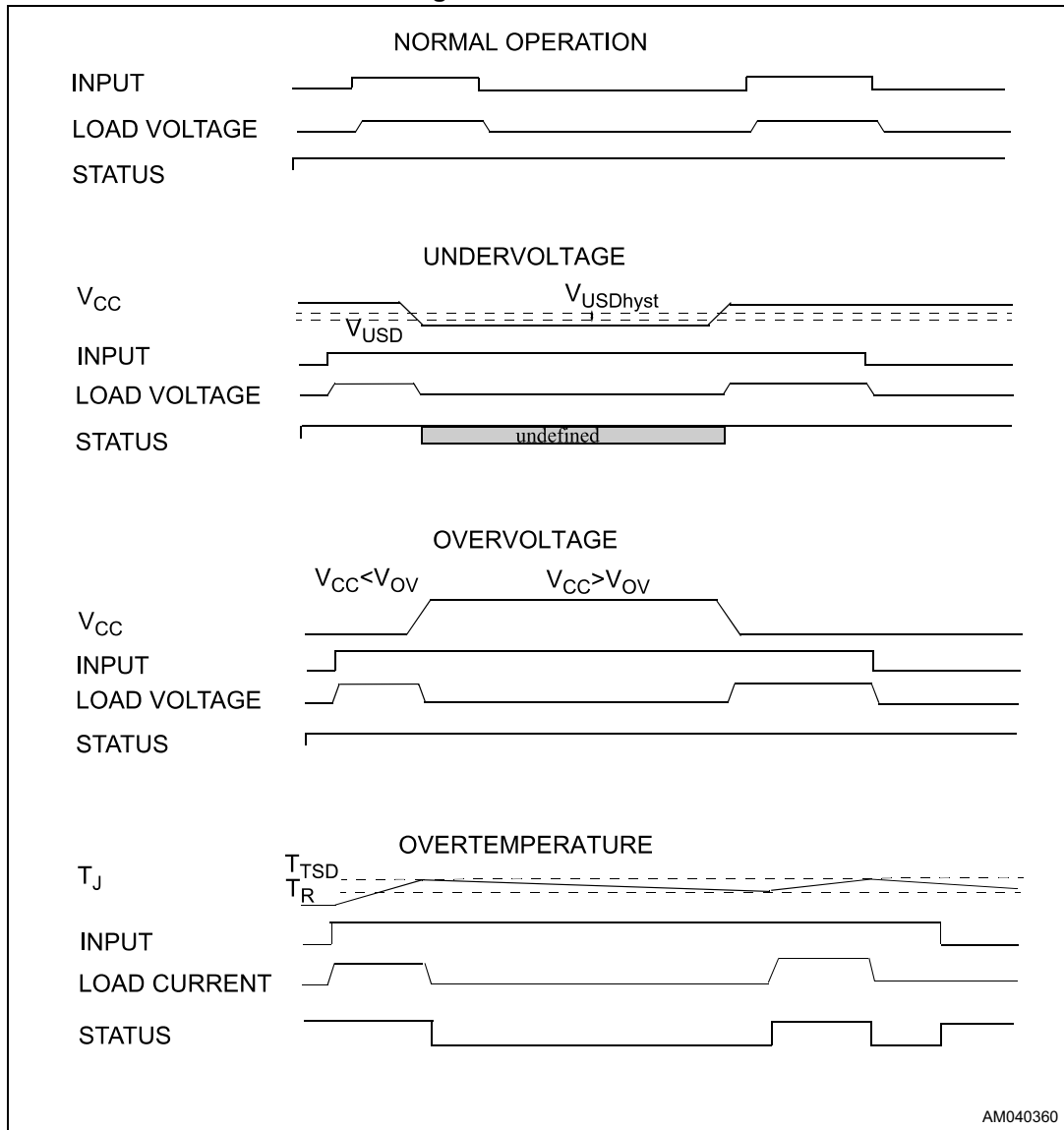


Table 9. Truth table

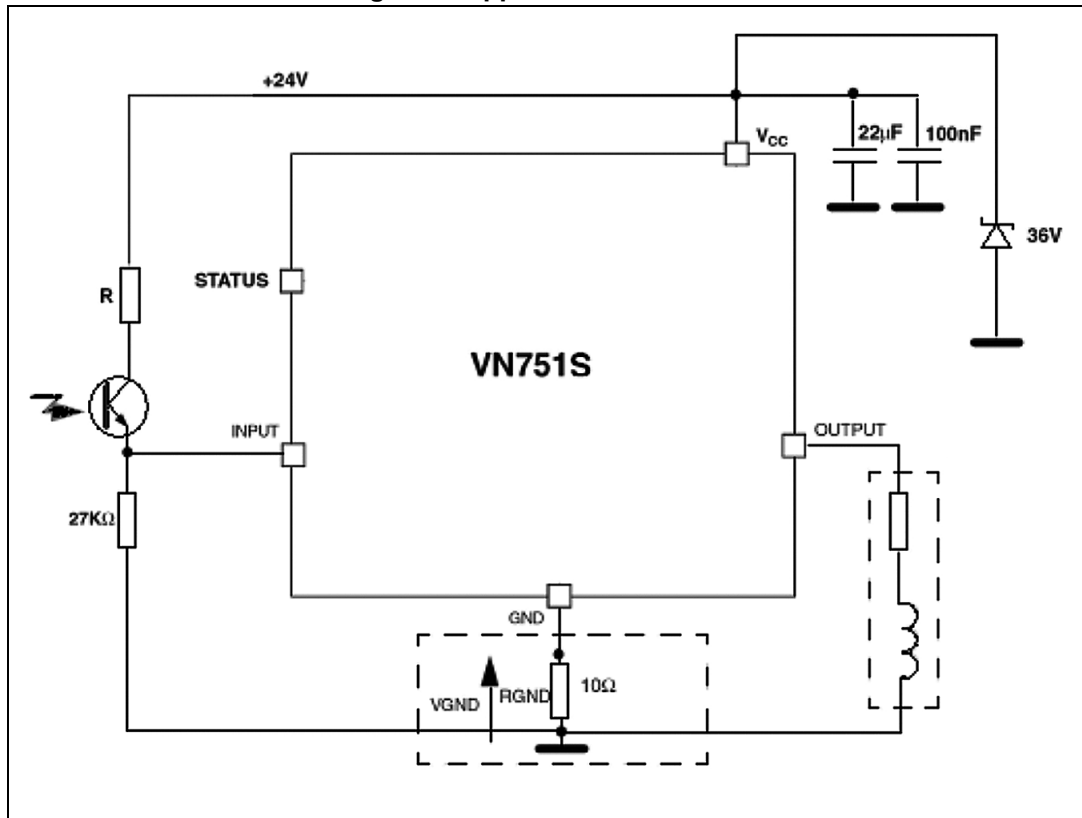
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	$(T_J < T_{TSD})$ H
	H	X	$(T_J > T_{TSD})$ L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H

Figure 7. Waveforms



7 Application schematic

Figure 8. Application schematic



8 Reverse polarity protection

A schematic solution to protect the IC against a reverse polarity condition is proposed.

This schematic is effective with any type of load connected to the outputs of the IC. The R_{GND} resistor value can be selected according to the following conditions:

Equation 1

$$R_{GND} \leq 600 \text{ mV} / (I_S \text{ in ON-state max.})$$

Equation 2

$$R_{GND} \geq (-V_{CC}) / (-I_{GND})$$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in [Section 3: Maximum ratings on page 7](#).

The power dissipation associated to R_{GND} during reverse polarity condition is:

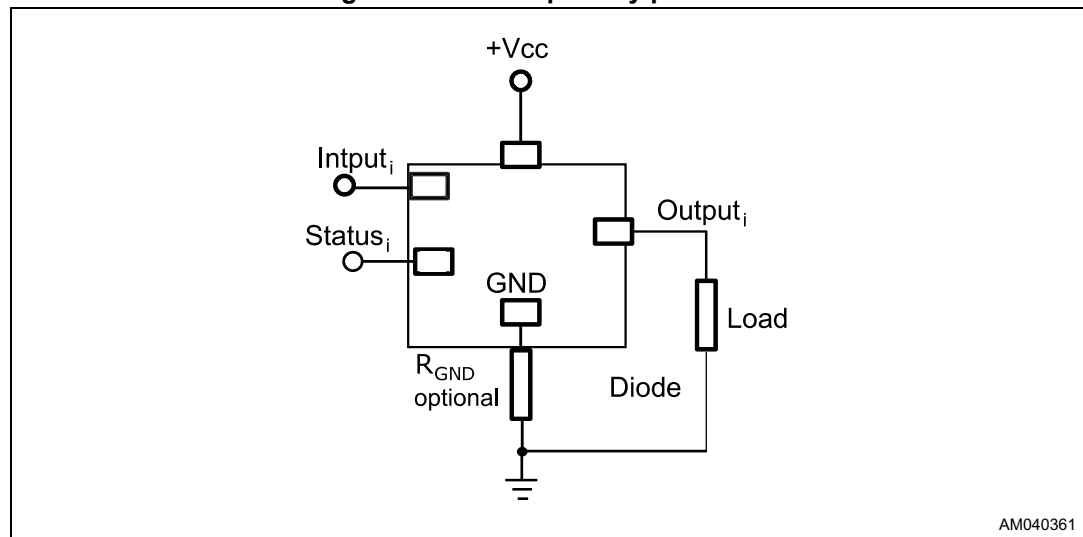
Equation 3

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared by several different ICs.

In such case I_S value in [Equation 1](#) is the sum of the maximum ON-state currents of the different devices. Please note that if the microprocessor ground and the device ground are separated, the voltage drop across the R_{GND} (given by $I_S \text{ in ON-state max.} * R_{GND}$) produces a difference between the generated input level and the IC input signal level. This voltage drop varies depending on how many devices are ON in case of several high-side switches sharing the same R_{GND} .

Figure 9. Reverse polarity protection



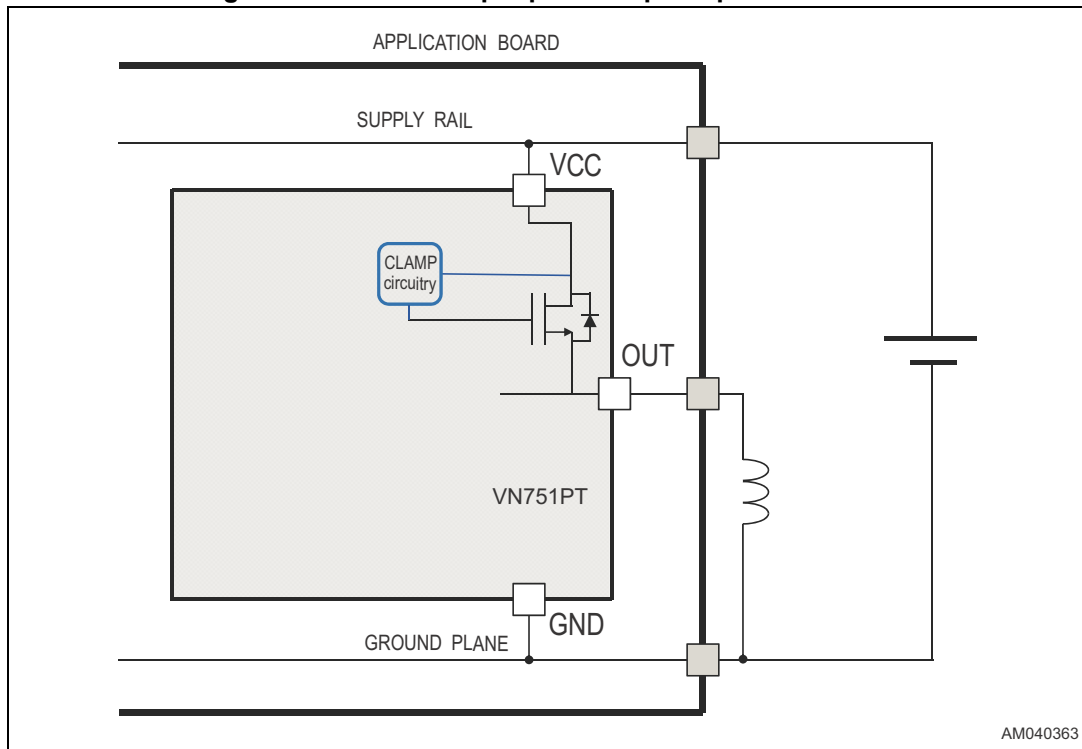
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9 Active VDS clamp

The active clamp is also known as the fast demagnetization of inductive loads or fast current decay. When a high-side driver turns off an inductance, an undervoltage is detected on the output.

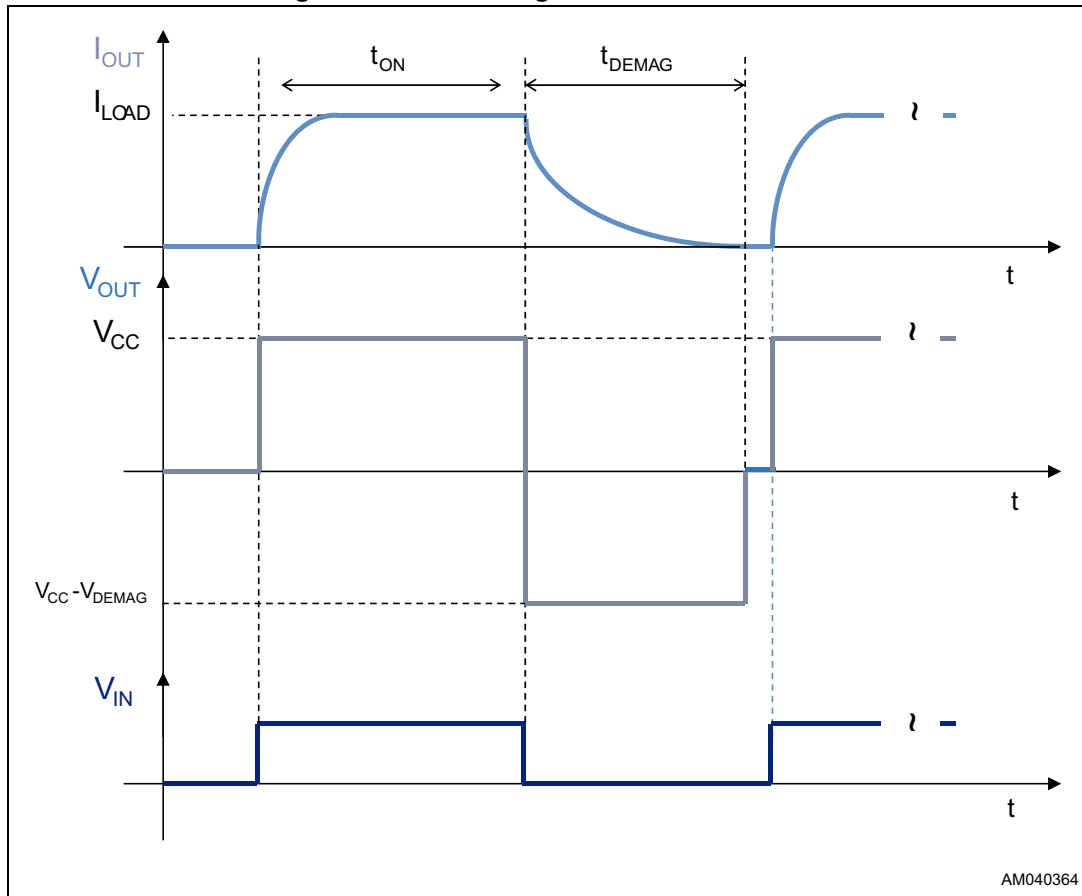
The OUT pin is pulled down to V_{demag} . The conduction state is modulated by internal circuitry in order to keep the OUT pin voltage at about V_{demag} until the load energy has been dissipated. The energy is dissipated both in the IC internal switch and in load resistance.

Figure 10. Active clamp equivalent principle schematic



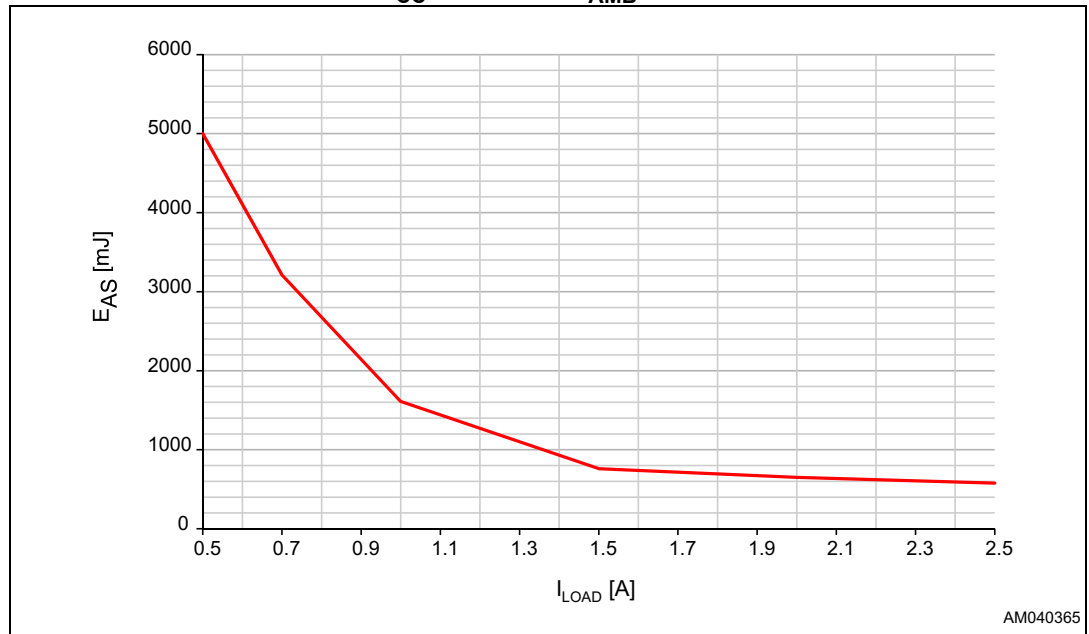
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Figure 11. Fast demagnetization waveforms



The demagnetization of the inductive load causes a huge electrical and thermal stress to the IC. The curve plotted in [Figure 12](#) shows the maximum demagnetization energy that the IC can support in a single demagnetization pulse with $V_{CC} = 24\text{ V}$ and $T_{AMB} = 125\text{ }^\circ\text{C}$. If higher demagnetization energy is required then an external free-wheeling Schottky diode has to be connected between OUT (cathode) and GND (anode) pins. Note that in this case the fast demagnetization is inhibited.

Figure 12. Typical demagnetization energy (single pulse)
at $V_{CC} = 24\text{ V}$ and $T_{AMB} = 125\text{ }^{\circ}\text{C}$



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

10.1 SO-8 package information

Figure 13. SO-8 package outline

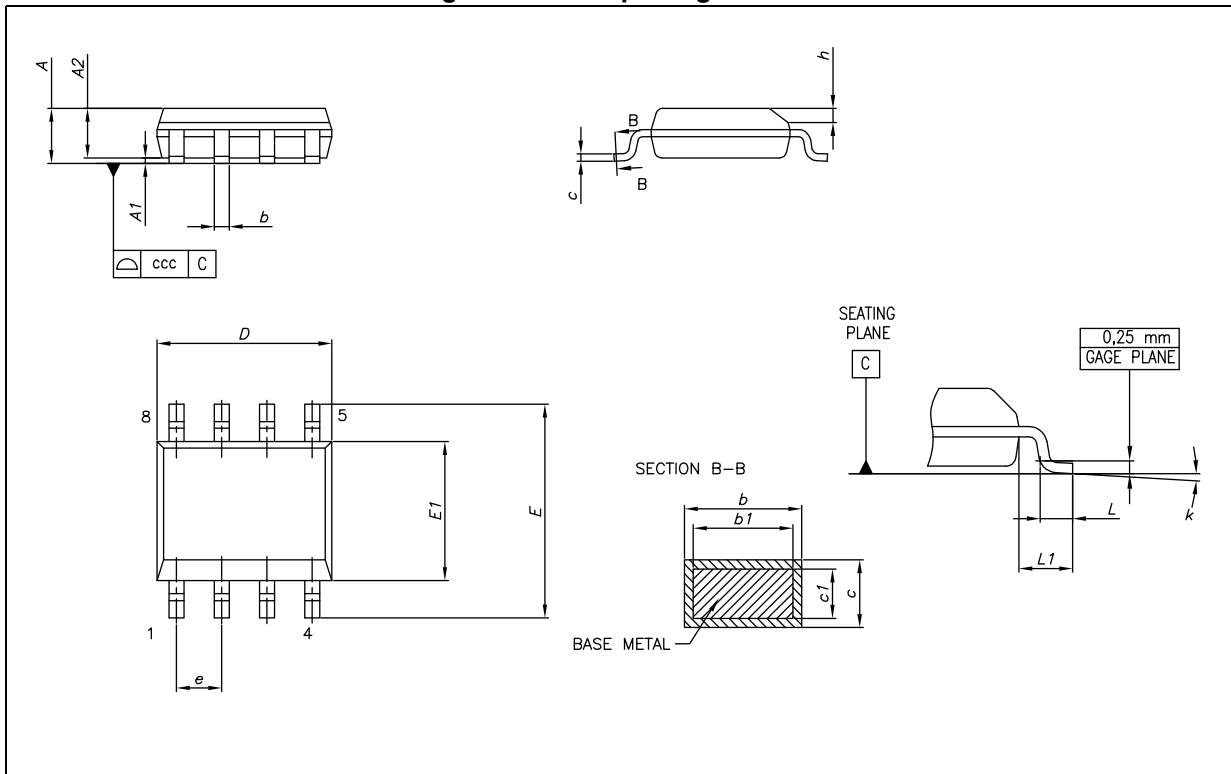
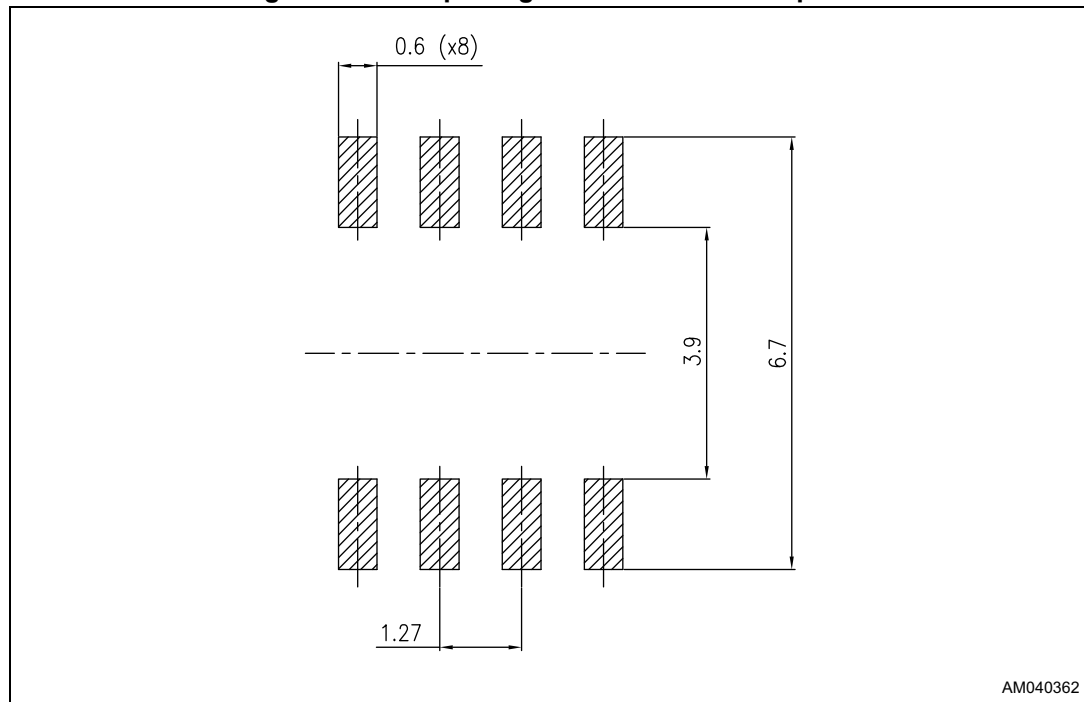


Table 10. SO-8 package mechanical data

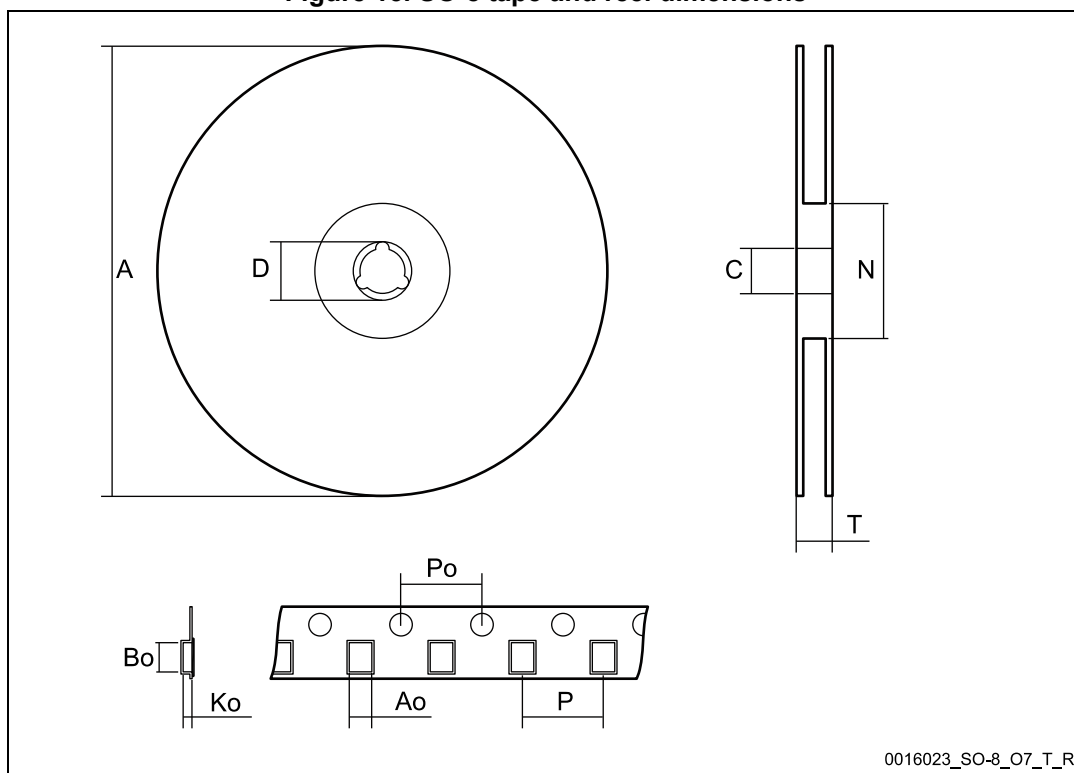
Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.28	-	0.48
c	0.17	-	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	-	1.27	-
h	0.25	-	0.50
L	0.40	-	1.27
L1	-	1.04	-
k	0°	-	8°
ccc	-	-	0.10

Figure 14. SO-8 package recommended footprint



10.2 SO-8 packing information

Figure 15. SO-8 tape and reel dimensions



0016023_SO-8_07_T_R

Table 11. SO-8 tape and reel mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-		330
C	12.8		13.2
D	20.2		-
N	60		-
T	-		22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

11 Revision history

Table 12. Document revision history

Date	Revision	Changes
18-Sep-2006	1	Initial release.
12-Mar-2007	2	Document reformatted, typo in table 3, updated P_{tot} value in table 2.
15-Mar-2007	3	Typo in table 1 V_{ESD} .
18-Sep-2007	4	Added I_{STAT} value in table 1.
11-Oct-2007	5	Updated table 2.
08-Jul-2008	6	Added section 7.
30-Nov-2009	7	Updated cover page and section 6.
12-Jul-2016	8	Updated Table 4: "Power section".
09-May-2018	9	Updated Section : Features on page 1 (added "Fast demagnetization of inductive loads"). Updated Table 2 on page 7 (Updated E_{AS} parameter and value). Updated Figure 8 on page 13 [removed "Nominal 2A LOAD and 270mH (SO8) 400mH (PPAK)"]. Added Section 9 on page 15 . Minor modifications throughout document.

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