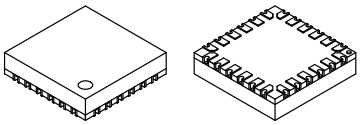
LC709301F

Switching Charge/Discharge Controller for 1-Cell Li-Ion Battery

ON Semiconductor®

www.onsemi.com



VCT24 3.5x3.5, 0.5P
CASE 601AD

Features

- 10 x / 20 x Amplifier
- 8/10−bit High−speed PWM (150 kHz)
- Reference Voltage Generator Circuit (2 V / 4 V) for an AD Converter
- Temperature Sensor
- Internal Reset Circuit
- 8−Channel AD Converter with 12−/8−bit Resolution Selector
- Internal Oscillation Circuits (30 kHz / 1 MHz / 8 MHz)

Performance

- 83.3 ns (12.0 MHz) V_{DD} = 2.7 V to 5.5 V Ta = −40°C to + 85°C
- 125 ns (8.0 MHz) V_{DD} = 2.0 V to 5.5 V Ta = −40°C to + 85°C
- 250 ns (4.0 MHz) V_{DD} = 1.8 V to 5.5 V Ta = −40°C to + 85°C

Function Descriptions

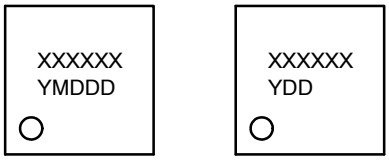
- Ports
  - I/O Ports :18
  - Reference Voltage Outputs: 1 (VREF)
  - Power Supply Pin : 3 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$)
- Timers (3ch)
  - Timer 0 : 16−bit Timer/Counter with a Capture Register
  - Timer 1 : 16−bit Timer/Counter that Supports PWM/Toggle Outputs
  - Base Timer Serving as a Realtime Clock
- SIO (1ch)
  - SIO1: 8−bit Asynchronous/Synchronous Serial Interface
- Comparator
- Watchdog Timer
- Frequency Tunable 12−bit PWM x 2ch
- System Clock Divider Function
- 15 sources, 10 Vectors Interrupts
- On−chip Debugger Function

Application

- Battery Charge/Discharge Control (E−cigarette)

*This product is licensed from Silicon Storage Technology, Inc. (USA).

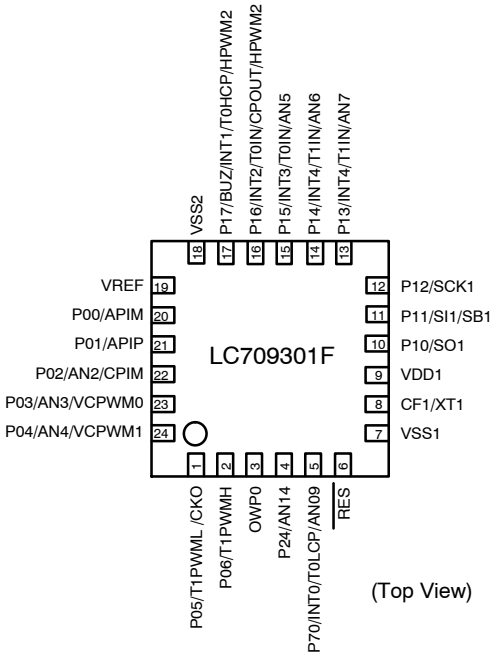
MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DD / DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 23 of this data sheet.

Function Details

Flash ROM

- Capable of on−board programming with a wide range of supply voltages: 2.2 to 5.5 V
- Block−erasable in 128 byte units
- Writes data in 2−byte units
- 8192 x 8 bits

RAM

- 256 x 9 bits

Bus Cycle Time

- 83.3 ns (12 MHz, V_{DD} = 2.7 V to 5.5 V, Ta = −40°C to 85°C)
- 125 ns (8 MHz, V_{DD} = 2.0 V to 5.5 V, Ta = −40°C to 85°C)
- 250 ns (4 MHz, V_{DD} = 1.8 V to 5.5 V, Ta = −40°C to 85°C)

NOTE: The bus cycle time here refers to the ROM read speed.

Minimum Instruction Cycle Time (tCYC)

- 250 ns (12 MHz, V_{DD} = 2.7 V to 5.5 V, Ta = −40°C to 85°C)
- 375 ns (8 MHz, V_{DD} = 2.0 V to 5.5 V, Ta = −40°C to 85°C)
- 750 ns (4 MHz, V_{DD} = 1.8 V to 5.5 V, Ta = −40°C to 85°C)

Potrs

- Normal withstand voltage I/O ports whose I/O direction can be designated in 1−bit units 18 (P0n, P1n, P24, P70, CF1)
- Reset pins 1 ($\overline{RES}$)
- Power supply pins 3 ($V_{SS}1$, $V_{SS}2$, $V_{DD}1$)
- Reference voltage outputs 1 (VREF)
- Dedicated debugger port 1 (OWP0)

Timers

- Timer 0: 16−bit timer/counter with 2 capture registers.
  - Mode 0: 8−bit timer with an 8−bit programmable prescaler (with two 8−bit capture registers) x 2 channels
  - Mode 1: 8−bit timer with an 8−bit programmable prescaler (with two 8−bit capture registers) + 8−bit counter (with two 8−bit capture registers)
  - Mode 2: 16−bit timer with an 8−bit programmable prescaler (with two 16−bit capture registers)
  - Mode 3: 16−bit counter (with two 16−bit capture registers)
- Timer 1: 16−bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8−bit timer with an 8−bit prescaler (with toggle outputs) + 8−bit timer/counter with an 8−bit prescaler (with toggle outputs)
  - Mode 1: 8−bit PWM with an 8−bit prescaler x 2 channels
  - Mode 2: 16−bit timer/counter with an 8−bit prescaler (with toggle outputs) (toggle outputs also possible from lower−order 8 bits)
  - Mode 3: 16−bit timer with an 8−bit prescaler (with toggle outputs) (lower−order 8 bits may be used as a PWM output)
- Base timer
  1. The clock is selectable from the low speed RC, system clock, and timer 0 prescaler output.
  2. with an 8−bit programmable prescaler
  3. Interrupts programmable in 5 different time schemes

SIO

- SIO1: 8−bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8−bit serial I/O (2− or 3−wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half−duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

AD Converter

- AD converter input port with 10 x /20 x amplifier (1 channel)
- AD converter input port (8 channel) 12−/8−bit resolution selectable AD converter
- Selectable reference voltage source for an AD converter (Selectable from V_{DD}, Internal Reference Voltage Generator Circuit (VREF))

Internal Reference Voltage Generator Circuit (VREF)

- Generates 2.0 V/4.0 V for AD converter.

Comparator

Comparator input pin (1 channel)
Comparator output pin (1 channel)
Comparator output set high when (comparator input level) <1.22 V
Comparator output set low when (comparator input level) >1.22 V

Clock Output Function

- Generates clocks with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillation clock that is selected as the system clock.

Watchdog Timer

- Generates an internal reset on an overflow occurring in the timer running on the low−speed RC oscillator clock (approx. 30 kHz).
- Operating mode at standby is selectable from 3 modes (continue counting/suspend operation/suspend counting with the count value retained)

Interrupts

- 15 sources, 10 vectors
  1. Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2. When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/BT
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	HPWM2
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	P0/VCPWM

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

Subroutine Stack Levels

Up to 128levels (the stack is allocated in RAM.)

High−speed Multiplication/Division Instructions

- 16 bits x 8 bits (5 tCYC execution time)
- 24 bits x 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

Oscillation Circuits

- Internal oscillation circuits
  1. Low−speed RC oscillation circuit: For system clock (approx.30 kHz)
  2. Medium−speed RC oscillation circuit: For system clock (1 MHz)
  3. Hi−speed RC oscillation circuit1: For system clock (8 MHz)
  4. Hi−speed RC oscillation circuit2: For High speed PWM (40 MHz)

System Clock Divider Function

- Can run on low consumption current
- Minimum instruction cycle selectable from 375 ns, 750 ns, 1.5 μs, 3.0 μs, 6.0 μs, 12.0 μs, 24.0 μs, 48.0 μs, and 96.0 μs (at 8 MHz main clock)

Internal Reset Circuit

- Power−on reset (POR) function
  1. POR reset is generated only at power−on time.
  2. The POR release level is 1.67 V.
- Low−voltage detection reset (LVD) function
  1. LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2. The use/disuse of the LVD function and the low voltage threshold level can be selected from 7 levels (1.91 V, 2.01 V, 2.31 V, 2.51 V, 2.81 V, 3.79 V and 4.28 V), through option configuration.

Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1. Oscillation is not halted automatically.
  2. There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) Having the watchdog timer or LVD function generate a reset
     (3) Having an interrupt generated
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1. The low−speed, medium−speed, and high−speed RC oscillators automatically stop operation.

     NOTE: The low−speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
  2. There are four ways of resetting the HOLD mode:
     (1) Setting the reset pin to the lower level
     (2) Having the watchdog timer or LVD function generate a reset
     (3) Having an interrupt source established at one of the INT0, INT1, INT2 and INT4 pins
     * INT0 and INT1 can be used in the level sense mode only.
     (4) Having an interrupt source established at port 0.

- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer (when low−speed RC oscillation is selected).
  1. The low−speed, medium−speed, and high−speed RC oscillators automatically stop operation.

     NOTE: The low−speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.

     NOTE: If the base timer is run with low−speed RC oscillation selected as the base timer input clock source and the X'tal HOLD mode is entered, the low−speed RC oscillator retains the state that is established when the X'tal HOLD mode is entered.
  2. There are five ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Having the watchdog timer or LVD function generate a reset
     (3) Having an interrupt source established at one of the INT0, INT1, INT2, and INT4 pins
     * INT0 and INT1 can be used in the level sense mode only.
     (4) Having an interrupt source established at port 0
     (5) Having an interrupt source established in the base timer circuit

VCPWM

Frequency tunable 12−bit PWM x 2ch

High Speed PWM (HPWM2)

8−/10− bits PWM x1ch

1. The PWM clock is selectable from system clock and Hi−speed RC2 (40 MHz)
2. The PWM type is selectable from 8 bits (Normal mode) and 10 bits (additive pulse mode).

Temperature Sensor

- Sensor voltage can be compared by the AD converter.

On−chip Debugger Function

- Supports software debugging with the IC mounted on the target board.
- Provides 1 channel of on−chip debugger pin.
  OWP0

Data Security Function

- Protects the program data stored in flash memory from unauthorized read or copy.

NOTE: This data security function does not necessarily provide absolute data security.

Package Form

- VCT24 (3.5 x 3.5): Lead−free and halogen−free type

Development Tools

- On−chip debugger: TCB87 Type C (1−wire interface cable) + LC709301F

Programming Boards

Package	Programming Boards
VCT24 (3.5 x 3.5)	W709301V−GMDT

FLASH PROGRAMMER

Maker		Model	Supported Version	Device
Flash Support Group Company (FSG)	Single Programmer	AF9711	Rev 03.28 or later	87F008SU
Flash Support Group Company (FSG) + ON Semiconductor (Note 1)	Onboard Single/Gang Programmer	AF9101/AF9103 (Main unit) (FSG models)	(Note 2)	−
		SIB87 Type C (Inter Face Driver) (Our company model)		
ON Semiconductor	Single/Gang Programmer	SKK Type B / SKK Type C	Application Version 1.08A or later Chip Data Version 2.52 or later	LC709301F
	Onboard Single/Gang Programmer	SKK−DBG Type C		

For information about AF−Series:
Flash Support Group Company (TOA ELECTRONICS, Inc.)
TEL: +81−53−459−1050
E−mail: sales@j−fsg.co.jp

1. On−board−programmer from FSG (AF9101/AF9103) and serial interface driver from ON Semiconductor. (SIB87 Type C) together can give a PC−less, standalone on−board−programming capabilities.
2. It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or our company for the information.

Pin Assignment

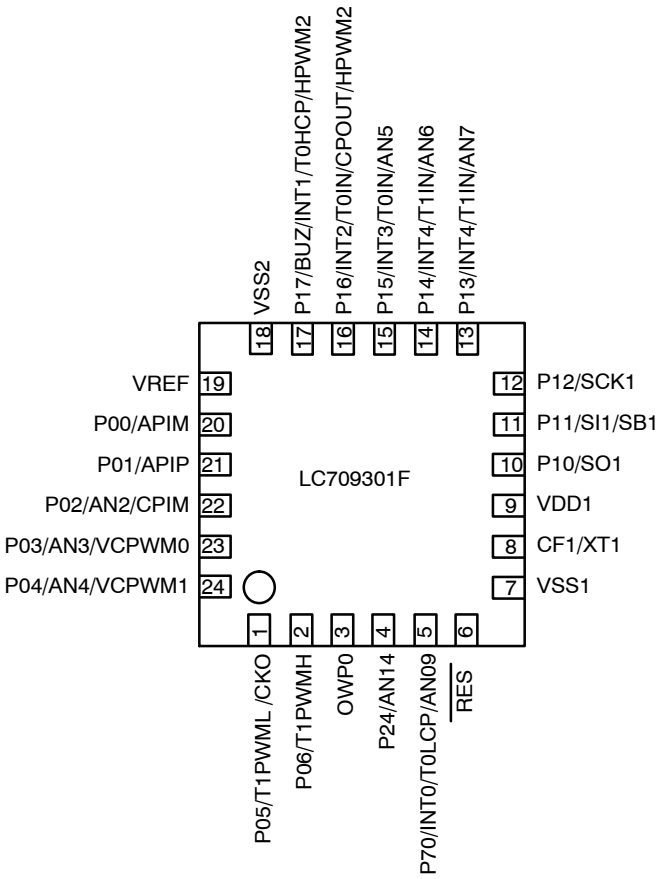


Figure 1. Top View
VCT24 (3.5 x 3.5) "Pb−Free / Halogen Free Type"

VCT24	NAME
1	P05/T1PWML /CKO
2	P06/T1PWMH
3	OWP0
4	P24/AN14
5	P70/INT0/T0LCP/AN09
6	$\overline{\text{RES}}$
7	VSS1
8	CF1/XT1
9	VDD1
10	P10/SO1
11	P11/SI1/SB1
12	P12/SCK1

VCT24	NAME
13	P13/INT4/T1IN/AN7
14	P14/INT4/T1IN/AN6
15	P15/INT3/T0IN/AN5
16	P16/INT2/T0IN/CPOUT/HPWM2
17	P17/BUZ/INT1/T0HCP/HPWM2
18	VSS2
19	VREF
20	P00/APIM
21	P01/APIP
22	P02/AN2/CPIM
23	P03/AN3/VCPWM0
24	P04/AN4/VCPWM1

System Block Diagram

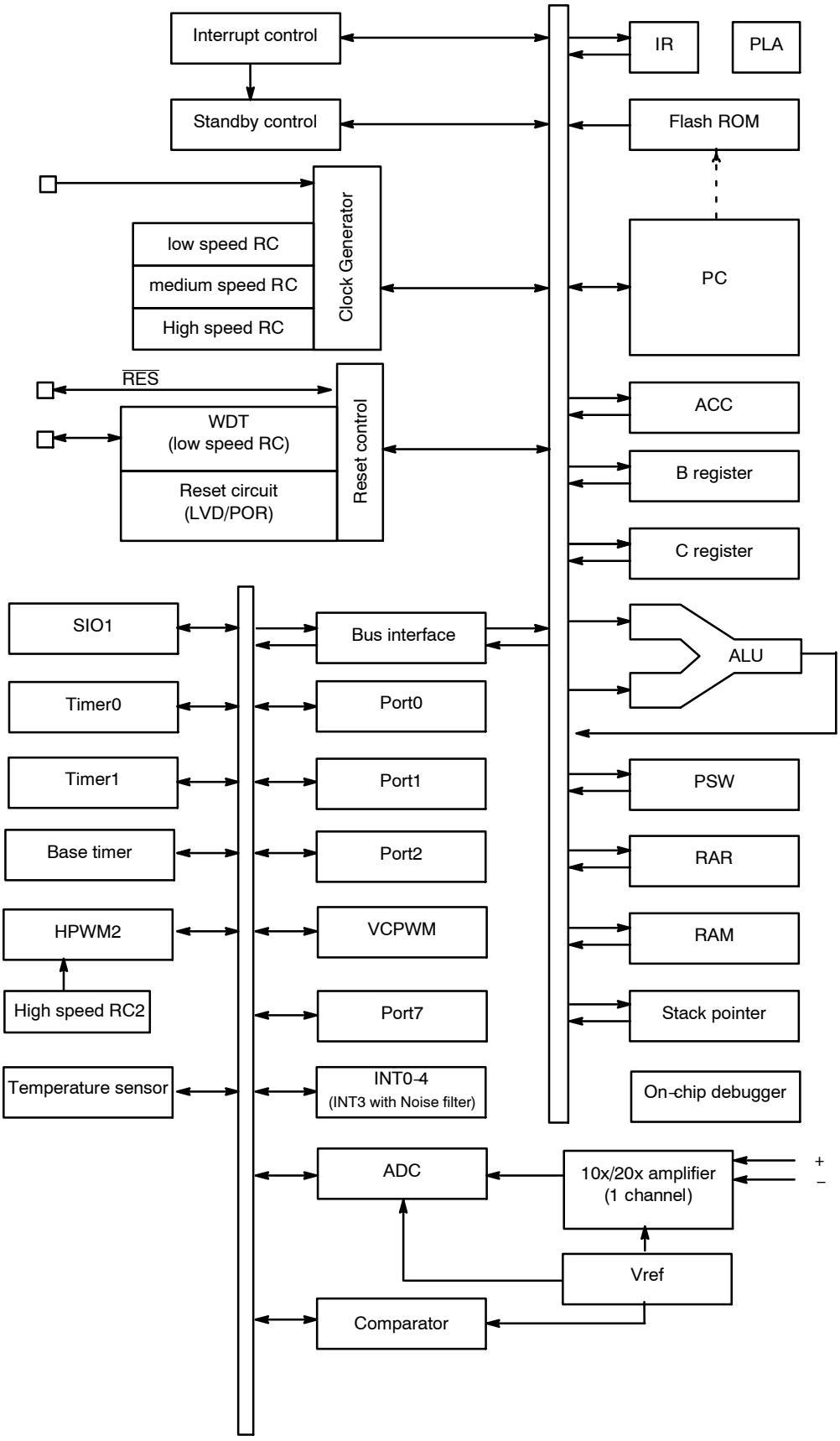


Figure 2. System Block Diagram

PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>–</td><td>– power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>–</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>$V_{SS}2$</td><td>–</td><td>– power supply pin</td><td>No</td></tr>
<tr><td>VREF</td><td>I/O</td><td>Reference voltage output (2.0 V / 4.0 V) or External input</td><td>No</td></tr>
<tr><td>Port 0

P00 to P06</td><td>I/O</td><td>•7−bit I/O port
• I/O specifiable in 1−bit units.
• Pull−up resistors can be turned on and off in 1−bit units.

• Pin functions
P00, P01: AD converter input port with 10x/20x operational amplifier
P02: AD converter input port (AN2) / Comparator input (CPIM)
P03: AD converter input port (AN3) / VCPWM0 output
P04: AD converter input port (AN4) / VCPWM1 output
P05: Timer 1 PWML output / System clock output
P06: Timer 1 PWMH output
P07: On−chip debugger pin (OWP0)</td><td>Yes</td></tr>
<tr><td>Port 1

Port10 to P15</td><td>I/O</td><td>• 8−bit I/O port
• I/O specifiable in 1−bit units.
• Pull−up resistors can be turned on and off in 1−bit units.

• Pin functions
P10: SIO1 data output
P11: SIO1 data input/bus input/output
P12: SIO1 clock input/output
P13: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/timer 0H capture input/AD converter input port (AN7)
P14: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/timer 0H capture input/AD converter input port (AN6)
P15: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/AD converter input port (AN5)
P16: INT2 input/HOLD release input/timer 0 event input/timer 0L capture input/HPWM2 output
P17: beeper output/INT1 input/HOLD release input/timer 0H capture input/HPWM2 output

Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 2

P24</td><td>I/O</td><td>• 1−bit I/O port
• I/O specifiable
• Pull−up resistors can be turned on and off.

• Pin functions
P24: AD converter input port (AN14)</td><td>Yes</td></tr>
<tr><td>Port 7

P70</td><td>I/O</td><td>• 1−bit I/O port
• I/O specifiable
• Pull−up resistors can be turned on and off.

• Pin functions
P70: INT0 input/HOLD release input/timer 0L capture input/AD converter input port (AN9)

Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table></td><td>No</td></tr>
</table>

PIN DESCRIPTION (continued)

Pin Name	I/O	Description	Option
$\overline{\text{RES}}$	I	External reset input/internal reset output pin	Yes Internal pullup ON/OFF
CF1/XT1	I/O	• External system clock input Port • Pin functions • 1−bit I/O port • I/O specifiable (only Nch−open drain)	No
OWP0	I/O	On−chip debugger pin	No

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull−up resistor.

Data can be read into any input port even if it is in the output mode.

PORT OUTPUT TYPES

Port Name	Option Selected in Units of	Option Type	Output Type	Pull−up Resistor
P00 to P06	1 bit	1	CMOS	Programmable
		2	Nch−open drain	Programmable
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch−open drain	Programmable
P24	1 bit	1	CMOS	Programmable
		2	Nch−open drain	Programmable
CF1/XT1	−	No	Nch−open drain when general I/O port is selected.	No
P70	−	No	Nch−open drain	Programmable

USER OPTION TABLE

Option Name	Option Type	Flash Version	Option Selected in Units of	Option Selection
Port output form	P00 to P06	enable	1 bit	CMOS
				Nch−open drain
	P10 to P17	enable	1 bit	CMOS
				Nch−open drain
	P24	enable	1 bit	CMOS
				Nch−open drain
Program start address	−	enable	−	00000h or 01E00h When protected area 1) is selected
				00000h When either of protected area 2), 3) or 4) is selected
Protected area (Note 3)	−	enable	−	1) 1800h−1FFFh
				2) 0000h−1DFFh, 1F00h−1FFFh
				3) 0000h−1CFFh, 1F00h−1FFFh
				4) 0000h−1AFFh, 1F00h−1FFFh
Reset pin	Internal pullup ON/OFF	enable	−	ON
				OFF
Low−voltage detection reset function	Detect function	enable	−	Enable: Use
				Disable: Not Used
	Detect level	enable	−	7−level
Power−on reset function	Power−On reset level	enable	−	1−level

3. Onboard programming inhibited address

RECOMMENDED UNUSED PIN CONNECTIONS

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P06	Open	Output low
P10 to P17	Open	Output low
P24	Open	Output low
P70	Open	Output low
CF1/XT1	Open	General I/O port output low
OWP0	Pulled low with a 100 kΩ resistor	−

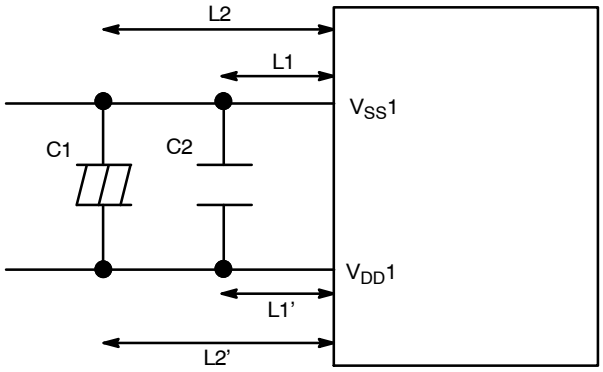
On−chip Debugger Pin Connection Requirements

For the treatment of the on−chip debugger pins, refer to the separately available documents entitled “Rd87 On−chip Debugger Installation Manual”

Power Pin Treatment Recommendations ($V_{DD}1$, $V_{SS}1$)

Connect bypass capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins:

- Connect among the $V_{DD}1$ and $V_{SS}1$ pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as equal as possible (L1 = L1’, L2 = L2’).
- Connect a large−capacity capacitor C1 and a small−capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1 μF.



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD} [V]	Min	Typ	Max	Unit
Maximum supply voltage		V_{DD}MAX	$V_{DD}1$		−	−0.3	to	+6.5	V
Input/output voltage		VIO	Port0, 1, 2 Port7 CF1, RES		−	−0.3	to	V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Port0 Port1 Port2	• When CMOS output type is selected • Per 1 applicable pin	−	−10	−	−	mA
	Average output current (Note 4)	IOMH(1)	Port0 Port1 Port2	• When CMOS output type is selected • Per 1 applicable pin	−	−7.5	−	−	
	Total output current	ΣIOAH(1)	Port0, 1 Port2	Total current of all applicable pins	−	−30	−	−	
Low level output current	Peak output current	IOPL(1)	Port0	• Per 1 applicable pin	−	−	−	20	
		IOPL(2)	Port1	• Per 1 applicable pin	−	−	−	20	
		IOPL(3)	Port2	• Per 1 applicable pin	−	−	−	20	
		IOPL(4)	Port7, CF1	• Per 1 applicable pin	−	−	−	10	
	Average output current (Note 4)	IOML(1)	Port0	• Per 1 applicable pin	−	−	−	15	
		IOML(2)	Port1	• Per 1 applicable pin	−	−	−	15	
		IOML(3)	Port2	• Per 1 applicable pin	−	−	−	15	
		IOML(4)	Port7, CF1	• Per 1 applicable pin	−	−	−	7.5	
	Total output current	ΣIOAL(1)	Port0, 1, 2, 7, CF1	Total current of all applicable pins	−	−	−	80	
Allowable power Dissipation		Pdmax(1)	VCT24 (3.5 x 3.5)	Ta = −40 to + 85°C Package with thermal resistance board (Note 5)	−	−	−	280	mW
Operating ambient Temperature		Topr			−	−40	−	+85	°C
Storage ambient Temperature		Tstg			−	−55	−	+125	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. The average output current is an average of current values measured over 100 ms intervals.
5. Thermal resistance board (size 40x50x0.85 mm, glass epoxy) is used.

ALLOWABLE OPERATING CONDITIONS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			
					Min	Typ	Max	Unit
Operating supply voltage (Note 6)	$V_{DD}(1)$	$V_{DD}1$	0.245 μs ≤ tCYC ≤ 200 μs	–	2.7	–	5.5	V
	$V_{DD}(2)$		0.367 μs ≤ tCYC ≤ 200 μs	–	2.0	–	5.5	
	$V_{DD}(3)$		0.735 μs ≤ tCYC ≤ 200 μs	–	1.8	–	5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1$	RAM and register contents sustained in HOLD mode.	–	1.6	–	–	
High level input voltage	VIH(1)	Port0, 1, 2 P70		1.8 to 5.5	$0.3V_{DD}$ +0.7	–	V_{DD}	
	VIH(4)	CF1, $\overline{RES}$		1.8 to 5.5	$0.75V_{DD}$	–	V_{DD}	
Low level input voltage	VIL(1)	Port0, 1, 2 P70		4.0 to 5.5	V_{SS}	–	$0.1V_{DD}$+0.4	
				1.8 to 4.0	V_{SS}	–	$0.2V_{DD}$	
	VIL(4)	CF1, $\overline{RES}$		1.8 to 5.5	V_{SS}	–	$0.25V_{DD}$	
Instruction cycle time (Note 7)	tCYC (Note 7)			2.7 to 5.5	0.245	–	200	μs
				2.0 to 5.5	0.367	–	200	
				1.8 to 5.5	0.735	–	200	
External system clock frequency	FEXCF	CF1	• System clock frequency division ratio=1/1 • External system clock duty = 50 ±5%	2.7 to 5.5	0.1	–	12	MHz
				2.2 to 5.5	0.1	–	8	
Oscillation frequency range	FmFRC(1)		Internal high−speed RC oscillation Ta = −10°C to +85°C (Note 8)	1.8 to 5.5	7.76	8.0	8.24	MHz
	FmFRC(2)		Internal high−speed RC oscillation Ta = −40°C to +85°C (Note 8)	1.8 to 5.5	7.60	8.0	8.40	
	FmRC		Internal medium−speed RC oscillation	1.8 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low−speed RC oscillation (Note 9)	1.8 to 5.5	27	30	33	kHz
	FmPWMRC		Internal high−speed RC oscillation for HPWM2	2.7 to 5.5	38	40	42	MHz
Oscillation Stabilization Time	TmsFRC (Note 8)		• When oscillation circuit is switched from “oscillation stopped” to “oscillation enabled” . • See Fig. 4.	1.8 to 5.5	–	–	100	μs
	tmsPWMRC			1.8 to 5.5	–	–	100	
	tmsRC			1.8 to 5.5	–	0	–	
	TmsSRC (Note 9)			1.8 to 5.5	–	–	1	ms

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. V_{DD} must be held greater than or equal to 2.7 V in the flash ROM onboard programming mode.
7. Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.
8. An oscillation stabilization time of 100 μs or longer must be provided before switching the system clock source after the state of the high−speed RC oscillation circuit is switched from “oscillation stopped” to “oscillation enabled” .
9. An oscillation stabilization time of 1ms or longer must be provided before switching the system clock source after the state of the low−speed RC oscillation circuit is switched from “oscillation stopped” to “oscillation enabled” .

ELECTRICAL CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			
					Min	Typ	Max	Unit
High level input current	$I_{IH}(1)$	Port0, 1, 2, Port7, $\overline{RES}$	Output disabled Pull−up resistor off $V_{IN} = V_{DD}$ (Including output Tr's off leakage current)	1.8 to 5.5	−	−	1	μA
	$I_{IH}(2)$	CF1	$V_{IN} = V_{DD}$	1.8 to 5.5	−	−	15	
Low level input current	$I_{IL}(1)$	Port0, 1, 2, Port7, $\overline{RES}$	Output disabled Pull−up resistor off $V_{IN} = V_{SS}$ (Including output Tr's off leakage current)	1.8 to 5.5	−1	−	−	
	$I_{IL}(2)$	CF1	$V_{IN} = V_{SS}$	1.8 to 5.5	−15	−	−	
High level output voltage	$V_{OH}(1)$	Port0, 1, 2	I_{OH} = −1 mA	4.5 to 5.5	V_{DD}−1	−	−	V
	$V_{OH}(2)$		I_{OH} = −0.2 mA	1.8 to 5.5	V_{DD}−0.4	−	−	
Low level output voltage	$V_{OL}(1)$	Port0, 1, 2, P70, CF1	I_{OL} = 10 mA	4.5 to 5.5	−	−	1.5	
	$V_{OL}(2)$		I_{OL} = 1.0 mA	1.8 to 5.5	−	−	0.4	
Pull−up resistance	Rpu(1)	Port0, 1, 2, P70	$V_{OH} = 0.9\ V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			1.8 to 4.5	18	50	230	
	Rpu(3)	$\overline{RES}$		1.8 to 5.5	300	400	500	
Hysteresis voltage	VHYS(1)	Port0, 1, 2, P70 $\overline{RES}$		2.7 to 5.5	−	$0.1V_{DD}$	−	V
				1.8 to 5.5	−	$0.07V_{DD}$	−	
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN} = V_{SS}$, f = 1 MHz, Ta = 25°C	1.8 to 5.5	−	10	−	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SIO1 SERIAL I/O CHARACTERISTICS (Note 10)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			
							Min	Typ	Max	Unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK1 (P12)	• See Fig. 6.	1.8 to 5.5	2	–	–	tCYC
		Low level pulse width	tSCKL(1)				1	–	–	
		High level pulse width	tSCKH(1)				1	–	–	
	Output clock	Frequency	tSCK(2)	SCK1 (P12)	• CMOS output type selected • See Fig. 6.	1.8 to 5.5	2	–	–	
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
Serial input	Data setup time		tsDI(1)	SI1 (P11), SB1 (P11)	• Specified with respect to rising edge of SIOCLK. • See Fig. 6.	1.8 to 5.5	0.05	–	–	µs
	Data hold time		thDI(1)				0.05	–	–	
Serial output	Output delay time		tdDO(1)	SO1 (P10), SB1 (P11)	• Specified with respect to falling edge of SIOCLK • Specified as the time up to the beginning of output change in open drain output mode. • See Fig. 6.	1.8 to 5.5	–	–	(1/3)tCYC +0.08	

10. These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

PULSE INPUT CONDITIONS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification			
					Min	Typ	Max	Unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0 (P70), INT1 (P17), INT2 (P16), INT4 (P13, P14)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	1.8 to 5.5	1	–	–	tCYC
	tPIH(2) tPIL(2)	INT3 (P15) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	2	–	–	
	tPIH(3) tPIL(3)	INT3 (P15) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	64	–	–	
	tPIH(4) tPIL(4)	INT3 (P15) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	1.8 to 5.5	256	–	–	
	tPIL(5)	$\overline{RES}$	• Resetting is enabled.	1.8 to 5.5	200	–	–	µs

AD CONVERTER CHARACTERISTICS ($V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	Typ	Max	Unit
12 BITS AD CONVERTER MODE (Ta = −40°C to +85°C)								
Resolution	N	AN2 (P02) AN3 (P03) AN4 (P04) AN5 (P15) AN6 (P14) AN7 (P13) AN9 (P70) AN14 (P24) (Note 13)		1.8 to 5.5	–	12	–	bit
Absolute accuracy	ET		(Note 11)	1.8 to 5.5	–	–	±16	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 12)	2.7 to 5.5	32	–	115	μs
				2.2 to 5.5	134	–	215	
				1.8 to 5.5	400	–	430	
Analog input voltage range	VAIN(1)		When V_{DD} is selected	1.8 to 5.5	V_{SS}	–	V_{DD}	V
	VAIN(2)		When internal VREF = 4 V is selected. VREF ≤ V_{DD}	4.3 to 5.5	V_{SS}	–	VREF	
			When internal VREF = 2 V is selected VREF ≤ V_{DD}	2.3 to 3.6	V_{SS}	–	VREF	
Analog port input current	IAINH		VAIN = V_{DD}	1.8 to 5.5	–	–	1	μA
	IAINL		VAIN = V_{SS}	1.8 to 5.5	−1	–	–	
8 BITS AD CONVERTER MODE (Ta = −40°C to +85°C)								
Resolution	N	AN2 (P02) AN3 (P03) AN4 (P04) AN5 (P15) AN6 (P14) AN7 (P13) AN9 (P70) AN14 (P24) (Note 13)		1.8 to 5.5	–	8	–	bit
Absolute accuracy	ET		(Note 11)	1.8 to 5.5	–	–	±1.5	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 12)	2.7 to 5.5	20	–	90	μs
				2.2 to 5.5	80	–	135	
				1.8 to 5.5	245	–	265	
Analog input voltage range	VAIN(1)		When V_{DD} is selected	1.8 to 5.5	V_{SS}	–	V_{DD}	V
	VAIN(2)		When internal VREF = 4 V is selected. VREF ≤ V_{DD}	4.3 to 5.5	V_{SS}	–	VREF	
			When internal VREF = 2 V is selected. VREF ≤ V_{DD}	2.3 to 3.6	V_{SS}	–	VREF	
Analog port input current	IAINH		VAIN = V_{DD}	1.8 to 5.5	–	–	1	μA
	IAINL		VAIN = V_{SS}	1.8 to 5.5	−1	–	–	

11. The quantization error (±1/2LSB) is excluded from the absolute accuracy. The absolute accuracy is measured when no change occurs in the I/O state of the pins that are adjacent to the analog input channel during AD conversion processing.
12. The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.
    The conversion time is twice the normal value when one of the following conditions occurs:
    • The first AD conversion executed in the 12−bit AD conversion mode after a system reset
    • The first AD conversion executed after the AD conversion mode is switched from 8−bit to 12−bit AD conversion mode
13. See page 16, "10x/20x amplifier characteristics", for analog channel 0 (10x/20z amplifier output).

Conversion Time Calculation Method

12bits AD Converter Mode: TCAD (Conversion time) = ((52 / (AD division ratio)) + 2) x (1 / 3) x tCYC

8bits AD Converter Mode: TCAD (Conversion time) = ((32 / (AD division ratio)) + 2) x (1 / 3) x tCYC

RECOMMENDED OPERATING CONDITIONS

External Oscillation (FmCF)	Operating Supply Voltage Range (V_{DD})	System Division Ratio (SYSDIV)	Cycle Time (tCYC)	AD Division Ratio (ADDIV)	AD Conversion Time (TCAD)	
					12bit AD	8bit AD
CF−8 MHz	2.7 V to 5.5 V	1/1	375 ns	1/8	52.25 μs	32.25 μs
	2.2 V to 5.5 V	1/1	375 ns	1/32	208.25 μs	128.25 μs
CF−4 MHz	2.7 V to 5.5 V	1/1	750 ns	1/8	104.5 μs	64.5 μs
	2.2 V to 5.5 V	1/1	750 ns	1/16	208.5 μs	128.5 μs
	1.8 V to 5.5 V	1/1	750 ns	1/32	416.5 μs	256.5 μs

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

REFERENCE VOLTAGE GENERATOR CIRCUIT (VREF) CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD} [V]	Min	Typ	Max	Unit
VREF = 2 V voltage accuracy	VREF2VO	VREF (Note 15)		1.8 to 2.0	V_{DD}−0.1	−	V_{DD}	V
				2.0 to 5.5	1.90	−	2.02	
				2.3 to 5.5	1.98	−	2.02	
VREF = 4 V voltage accuracy	VREF4VO			1.8 to 4.0	V_{DD}−0.1	−	V_{DD}	
				4.0 to 5.5	3.90	−	4.04	
				4.3 to 5.5	3.96	−	4.04	
VREF output current	VREFIO			1.8 to 5.5	V_{SS}	−	0.5	mA
Operation stabilization time (Note 14)	tVREFW			1.8 to 5.5	−	−	5	ms

14. Refers to the interval between the time VR12ON and VR24ON are set to 1 and the time operation gets stabilized.
15. An external 4.7 μF capacitor must be connected to the VREF pin to stabilize the VREF voltage.

10x/20x AMPLIFIER CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions		V_{DD} [V]	Specification Min	Typ	Max	Unit
20x Amplifier gain	APGAIN20 See Fig. 8	P00/APIM P01/APIP	1) APDIR = 0 & GAIN20 = 1. • P00 = 0 V, P01 ≥ 0 V 2) APDIR = 1 & GAIN20 = 1. • P01 = 0 V, P00 ≥ 0 V		4.3 to 5.0	–	20.5	–	
			1) APDIR = 0 & GAIN20 = 1. • P01 = 0 V, P00 ≤ 0 V 2) APDIR = 1 & GAIN20 = 1. • P00 = 0 V, P01 ≤ 0 V			–	−19.9	–	
20x Amplifier offset	VAPIO20		1) APDIR = 0 & GAIN20 = 1. • P01 = 0 V, P00 ≤ 0 V or P00 = 0 V, P01 ≥ 0 V 2) APDIR = 1 & GAIN20 = 1. • P01 = 0 V, P00 ≥ 0 V or P00 = 0 V,P01 ≤ 0 V			200	–	600	mV
20x Amplifier input voltage range	VAPIM20−1	P00/APIM	1)	P01/APIP = 0 V		−0.17	–	0	V
	VAPIP20−1	P01/APIP		P00/APIM = 0 V		0	–	0.17	
	VAPIM20−2	P00/APIM	2)	P01/APIP = 0 V		0	–	0.17	V
	VAPIP20−2	P01/APIP		P00/APIM = 0 V		−0.17	–	0	
10x Amplifier gain	APGAIN10 See Fig. 8	P00/APIM P01/APIP	3) APDIR = 0 & GAIN20 = 0. • P00 = 0 V, P01 ≥ 0 V 4) APDIR = 1 & GAIN20 = 0. • P01 = 0 V, P00 ≥ 0 V			–	10.8	–	
			3) APDIR = 0 & GAIN20 = 0. • P01 = 0 V, P00 ≤ 0 V 4) APDIR = 1 & GAIN20 = 0. • P00 = 0 V, P01 ≤ 0 V			–	−9.95	–	
10x Amplifier offset	VAPIO10		3) APDIR = 0 & GAIN20 = 0. • P01 = 0 V, P00 ≤ 0 V or P00 = 0 V, P01 ≥ 0 V 4) APDIR = 1 & GAIN20 = 0. • P01 = 0 V, P00 ≥ 0 V or P00 = 0 V, P01 ≤ 0 V			100	–	300	mV
10x Amplifier input voltage range	VAPIM10−3	P00/APIM	3)	P01/APIP = 0 V		−0.24	–	0	V
	VAPIP10−3	P01/APIP		P00/APIM = 0 V		0	–	0.24	
	VAPIM10−4	P00/APIM	4)	P01/APIP = 0 V		0	–	0.24	V
	VAPIP10−4	P01/APIP		P00/APIM = 0 V		−0.24	–	0	
Amplifier input port input current	IAPINL	P00/APIM	P00/APIM = V_{SS}−0.2 V			−1	–	–	μA
	IAPINH	P01/APIP	P01/APIP = V_{DD}			–	–	1	
Operation stabilization time (Note 16)	tAPW					–	–	20	μs

16. Refers to the interval between the time APON is set to 1 and the time operation gets stabilized.

Amplifier Input Voltage Calculation Method: See Fig. 8

VAPFUL = (VREFAD − VAPIO) / APGAIN (VREFAD can be selected from internal − VREF4V, internal − VREF2V and V_{DD}.)

Note: VAPFUL must not exceed VAPIP or VAPIM.

COMPARATOR CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	Min	Typ	Max	Unit
Comparator threshold voltage (Note 17)	VCMVT	P02/CPIM		2.5 to 5.5	1.12	1.22	1.32	V
Input voltage range	VCMIN			2.5 to 5.5	V_{SS}	–	V_{DD}	V
Offset voltage	VOFF		• Within input voltage range	2.5 to 5.5	–	±10	±30	mV
Response time	tRT		• Within input voltage range • Input amplitude = 100 mV • Overdrive = 50 mV	2.5 to 5.5	–	200	600	ns
Operation stabilization time (Note 18)	tCMW			2.5 to 5.5	–	–	1.0	μs

17. Comparator output=High level when (P02/CPIM voltage) < VCMVT
    Comparator output=Low level when (P02/CPIM voltage) > (VCMVT + VOFF)
18. Refers to the interval between the time CPON is set to 1 and the time operation gets stabilized.

TEMPERATURE SENSOR CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD} [V]	Min	Typ	Max	Unit
4−DIODE MODE								
Output voltage	VOTMP4(1)		Ta = −40°C	5.0	3.23	3.25	3.27	V
	VOTMP4(2)		Ta = +25°C	5.0	2.75	2.77	2.80	
	VOTMP4(3)		Ta = +85°C	5.0	2.28	2.31	2.34	
Sensitivity	Vsen4		Ta = −40 to +85°C	3.5 to 5.5	−7.63	−7.54	−7.45	mV/°C
Absolute accuracy (Note 19, 20)	ETTMP4	Vref = 4 [V]	Ta = (60 ±10) °C (Note 21)	3.5 to 5.5	–	±2.5	±5	°C
			Ta = −40 to +85°C	3.5 to 5.5	–	±5	±10	
2−DIODE MODE								
Output voltage	VOTMP2(1)		Ta = −40°C	3.3	1.61	1.63	1.64	V
	VOTMP2(2)		Ta = +25°C	3.3	1.37	1.39	1.40	
	VOTMP2(3)		Ta = +85°C	3.3	1.14	1.16	1.17	
Sensitivity	Vsen2		Ta = −40 to +85°C	2.0 to 5.5	−3.81	−3.77	−3.72	mV/°C
Absolute accuracy (Note 19, 20)	ETTMP2	Vref = 2 [V]	Ta = (60 ±10) °C (Note 22)	2.0 to 5.5	–	±2.5	±5	°C
			Ta = −40 to +85°C	2.0 to 5.5	–	±5	±10	

19. There are cases when the absolute accuracy specification value is exceeded when a large current flows through the ports.
20. Including error of AD Converter.
21. When using the Temperature sensor 60°C 2−diodes reference register D2TL / D2TH.
22. When using the Temperature sensor 60°C 4−diodes reference register D4TL / D4TH.

POWER−ON RESET (POR) CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				Option Selected Voltage	Min	Typ	Max	Unit
POR release voltage	PORRL		Option selected (Note 23)	1.67 V	1.10	–	1.79	V
Detection voltage unpredictable area	POUKS		See Fig. 9. (Note 24)	–	–	0.7	0.95	
Power supply rise time	PORIS		Power startup time from V_{DD} = 0 V to 1.6 V	–	–	–	100	ms

23. The POR release voltage can be selected when the low−voltage detection feature is deselected.
24. There is an unpredictable area before the transistor starts to turn on.

LOW VOLTAGE RESET (LVD) CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	Option Selected Voltage	Specification Min	Typ	Max	Unit
LVD reset voltage (Note 26)	LVDET		Option selected See Fig. 10. (Note 25, 27)	1.91 V	1.81	1.91	2.01	V
				2.01 V	1.91	2.01	2.11	
				2.31 V	2.21	2.31	2.41	
				2.51 V	2.41	2.51	2.61	
				2.81 V	2.71	2.81	2.93	
				3.79 V	3.69	3.79	3.92	
				4.28 V	4.18	4.28	4.41	
LVD voltage hysteresis	LVHYS			1.91 V	–	55	–	mV
				2.01 V	–	55	–	
				2.31 V	–	55	–	
				2.51 V	–	55	–	
				2.81 V	–	60	–	
				3.79 V	–	65	–	
				4.28 V	–	65	–	
Detection voltage unpredictable area	LVUKS		See Fig. 10. (Note 28)	–	–	0.7	0.95	V
Minimum low voltage detection width (response sensitivity)	TLVDW		LVDET−0.5 V See Fig. 11.	–	0.2	–	–	ms

25. The LVD reset voltage can be selected from 7 levels when the low−voltage detection feature is selected.
26. The hysteresis voltage is not included in the LVD reset voltage specification value.
27. There are cases when the LVD reset voltage specification value is exceeded when a greater change in the output level or large current is applied to the port.
28. There is an unpredictable area before the transistor starts to turn on.

CONSUMPTION CURRENT CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	Typ	Max	Unit
Normal mode consumption current (Note 29, 30)	IDDOP(1)	$V_{DD}1$	• External clock = 8 MHz • System clock set to 8 MHz mode • Internal low−/medium−speed RC oscillation stopped • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/1	2.2 to 5.5	–	3.8	5.2	mA
				2.2 to 3.6	–	2.2	2.9	
	IDDOP(2)		• External clock = 4 MHz • System clock set to 4 MHz mode • Internal low−/medium−speed RC oscillation stopped • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5	–	2.1	3.5	
				1.8 to 3.6	–	1.1	1.7	
	IDDOP(3)		• Internal low−speed RC oscillation stopped • System clock set to internal medium−speed RC oscillation mode • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5	–	0.23	0.39	
				1.8 to 3.6	–	0.13	0.19	
	IDDOP(4)		• Internal low−/medium−speed RC oscillation stopped • System clock set to internal high−speed RC oscillation mode • Frequency division ratio set to 1/1	1.8 to 5.5	–	2.7	3.6	
				1.8 to 3.6	–	1.7	2.3	
	IDDOP(5)		• System clock set to internal low−speed RC oscillation mode • Internal medium−speed RC oscillation stopped • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5	–	10	42	μA
				1.8 to 3.6	–	6	21	

CONSUMPTION CURRENT CHARACTERISTICS (Ta = −40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0$ V) (continued)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	Typ	Max	Unit
HALT mode consumption current (Note 29, 30)	IDDHALT(1)	$V_{DD}1$	HALT mode • External clock=8Mhz • System clock set to 8MHz mode • Internal low−/medium−speed RC oscillation stopped • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/1	2.2 to 5.5	−	2.0	3.2	mA
				2.2 to 3.6	−	1.0	1.6	
	IDDHALT(2)		HALT mode • External clock = 4 MHz • System clock set to 4 MHz mode • Internal low−/medium−speed RC oscillation stopped • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5	−	1.2	2.4	
				1.8 to 3.6	−	0.5	1.0	
	IDDHALT(3)		HALT mode • Internal low−speed RC oscillation stopped • System clock set to internal medium−speed RC oscillation mode • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/2	1.8 to 5.5	−	0.12	0.25	
				1.8 to 3.6	−	0.06	0.11	
	IDDHALT(4)		HALT mode • Internal low−/medium−speed RC oscillation stopped • System clock set to internal high−speed RC oscillation mode • Frequency division ratio set to 1/1	1.8 to 5.5	−	1.1	1.7	
				1.8 to 3.6	−	0.7	1.0	
	IDDHALT(5)		HALT mode • System clock set to internal low−speed RC oscillation mode • Internal medium−speed RC oscillation stopped • Internal high−speed RC oscillation stopped • Frequency division ratio set to 1/1	1.8 to 5.5	−	3.8	37	μA
				1.8 to 3.6	−	2.4	17	
HOLD mode consumption current (Note 29, 30)	IDDHOLD(1)	$V_{DD}1$	HOLD mode	1.8 to 5.5	−	0.023	33.2	μA
				1.8 to 3.6	−	0.012	14.2	
	IDDHOLD(2)		HOLD mode • LVD option selected	1.8 to 5.5	−	1.09	26.9	
				1.8 to 3.6	−	0.86	11.8	
Timer HOLD mode consumption current (Note 29, 30)	IDDHOLD(3)		Timer HOLD mode • FmSRC = 30 kHz internal low−speed RC oscillation mode	1.8 to 5.5	−	0.63	34	
				1.8 to 3.6	−	0.53	15	

29. The consumption current value includes none of the currents that flow into the output transistors and internal pull−up resistors.
30. Unless otherwise specified, the consumption current for the LVD circuit is not included.

F−ROM PROGRAMMING CHARACTERISTICS (Ta = 10°C to +55°C, $V_{SS}1 = V_{SS}2 = 0$ V)

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD} [V]	Specification Min	Typ	Max	Unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	2.2 to 5.5	−	5	10	mA
Programming time	tFW(1)		• Erasing time	2.2 to 5.5	−	20	30	ms
	tFW(2)		• Programming time		−	40	60	μs

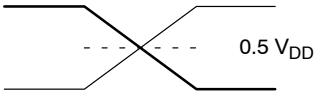
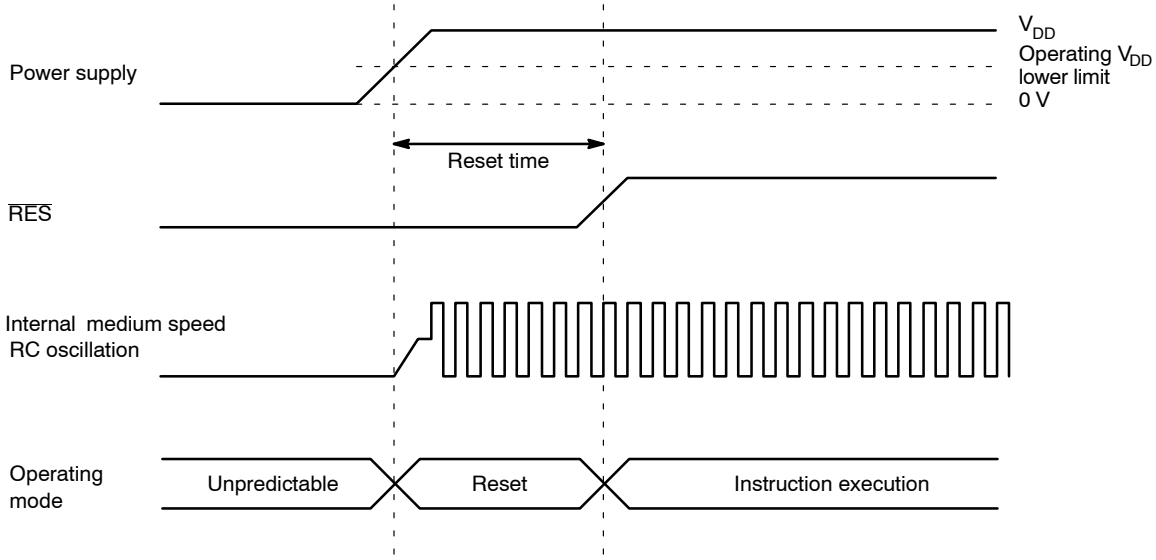
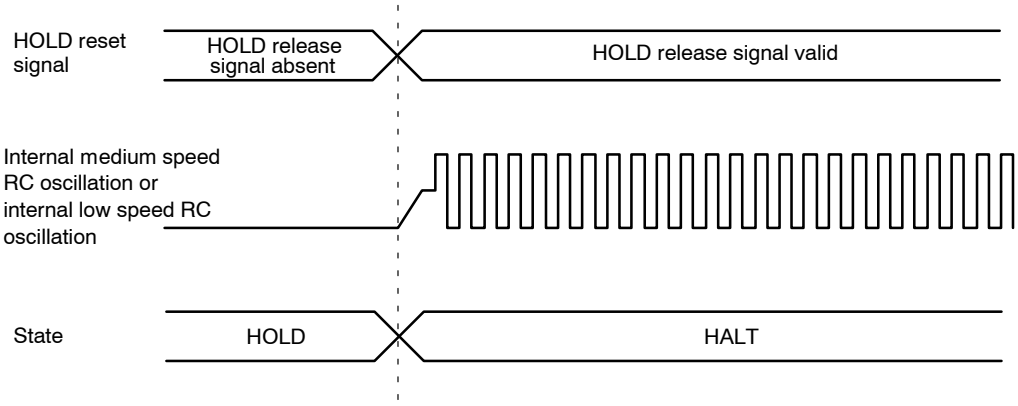


Figure 3. AC Timing Measurement Point



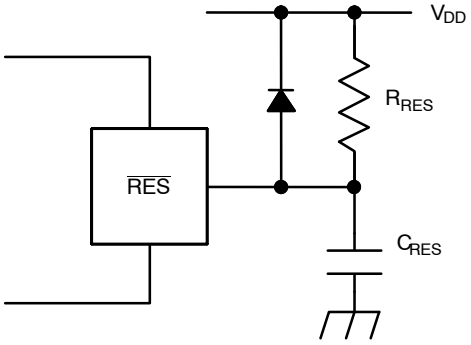
Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

NOTE: When an external oscillation circuit is selected.

Figure 4. Oscillation Stabilization Time



NOTE: The external circuit for reset may vary depending on the usage of POR and LVD. See “Reset Function” in the user’s manual.

Figure 5. Sample Reset Circuit

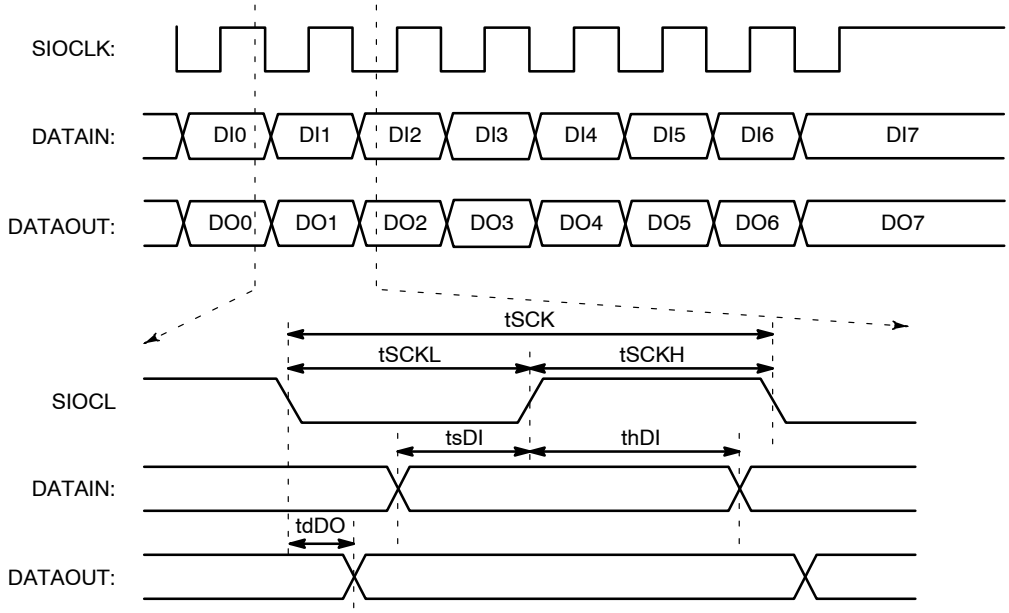


Figure 6. Serial I/O Waveform

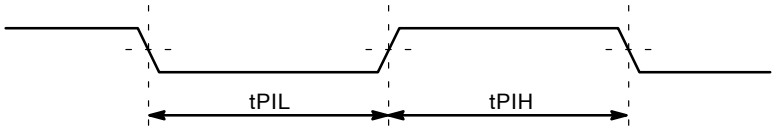


Figure 7. Pulse Input Timing Signal Waveform

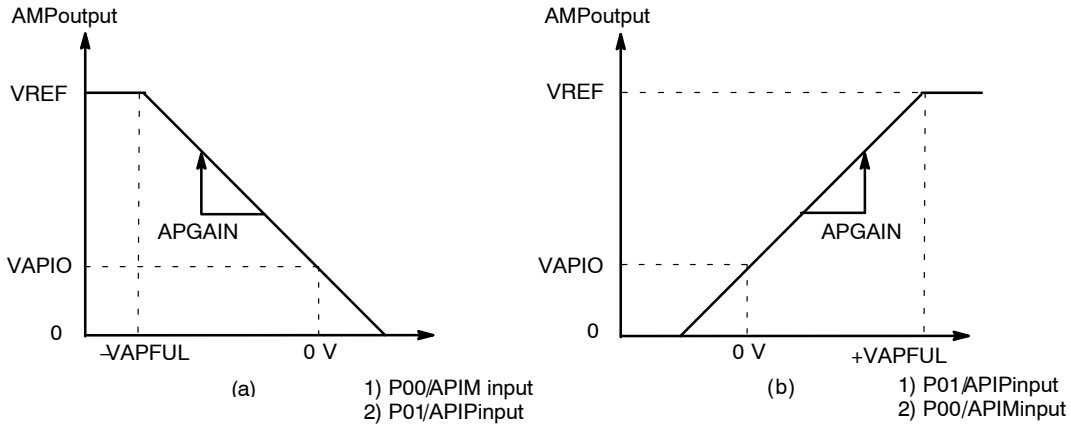


Figure 8. 10x / 20x Amplifier Characteristics

a) 1) When P01/APIP is 0 V, P00/APIM ≤ 0 V.
2) When P00/APIM is 0 V, P01/APIP ≤ 0 V.

b) 1) When P00/APIM is 0 V, P01/APIP ≥ 0 V.
2) When P01/APIP is 0 V, P00/APIM ≥ 0 V.

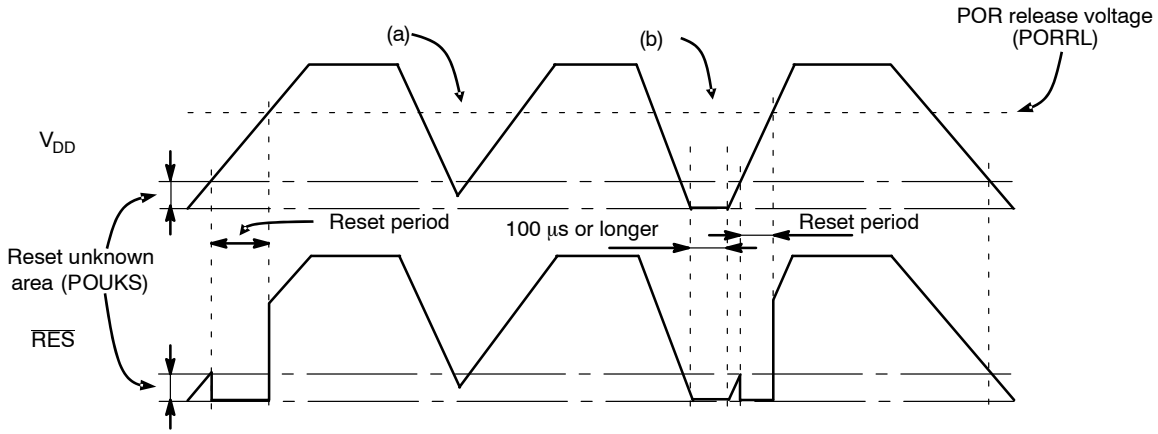


Figure 9. Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with R_{RES} Pull−up Resistor Only)

- The POR function generates a reset only when the power voltage goes up from the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit as shown below.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100 μs or longer.

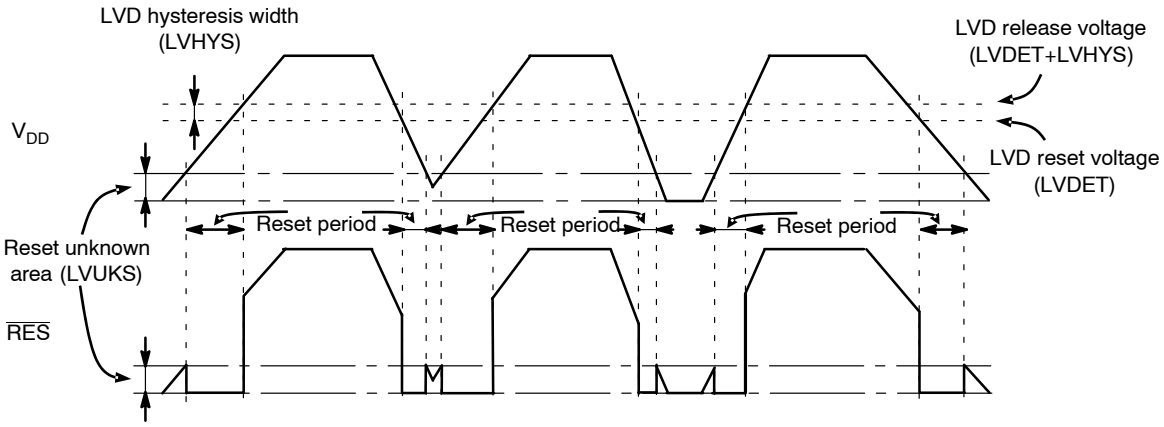


Figure 10. Example of POR + LVD Mode Waveforms (at Reset Pin with R_{RES} Pull−up Resistor Only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

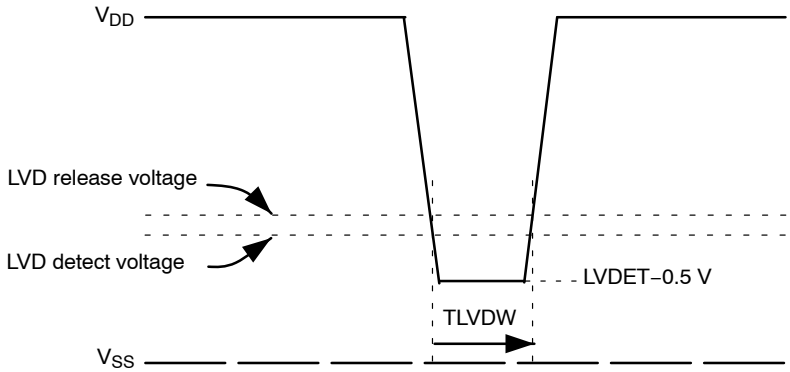


Figure 11. Minimum Low Voltage Detection Width (Example of Voltage Sag/Fluctuation Waveform)

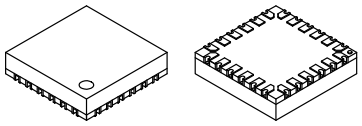
ORDERING INFORMATION

Device Order Number	Package Type	Shipping†
LC709301FRF−AUNH	VCT24 3.5x3.5, 0.5P (Pb−Free / Halogen Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

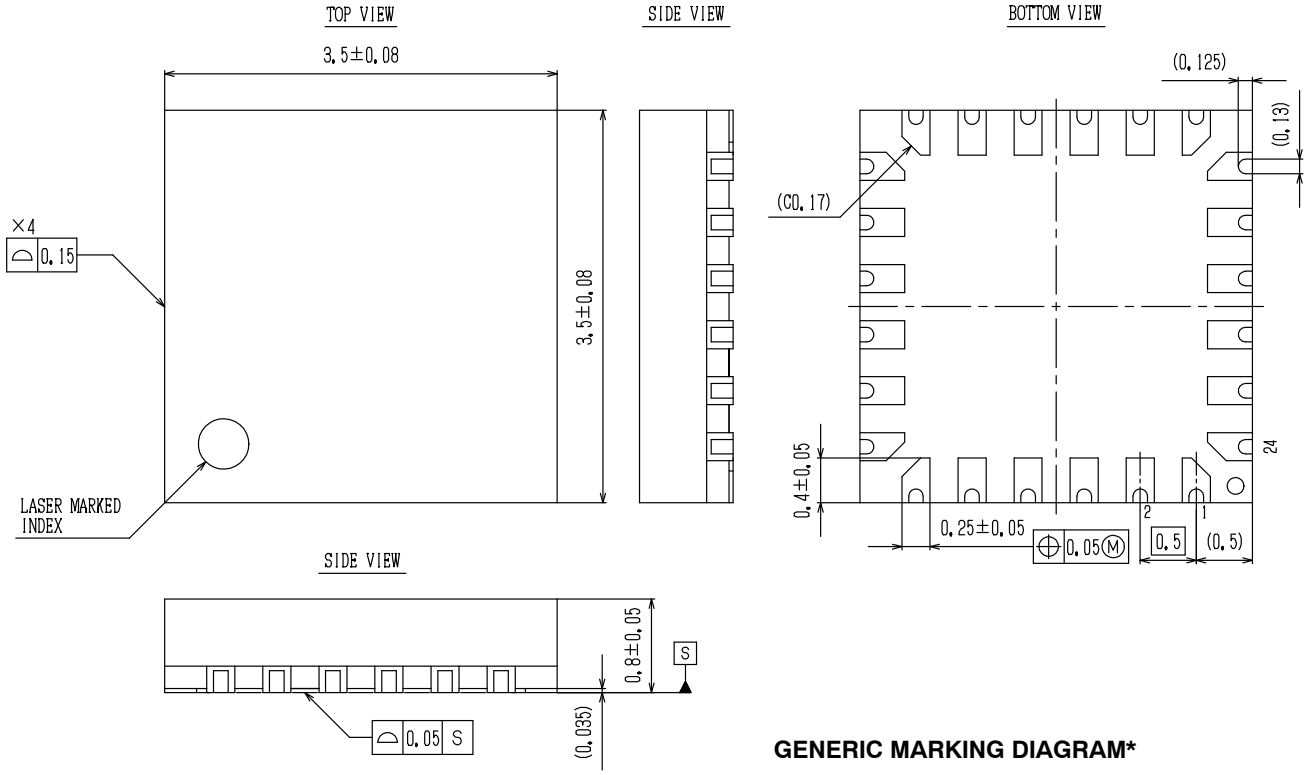
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

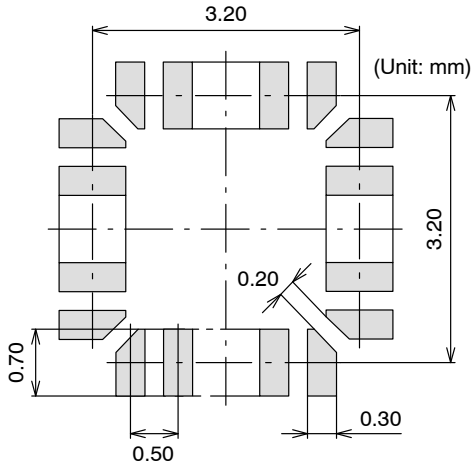


VCT24 3.5x3.5, 0.5P
CASE 601AD
ISSUE A

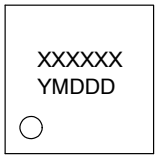
DATE 15 NOV 2013



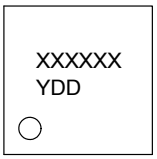
SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data



XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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