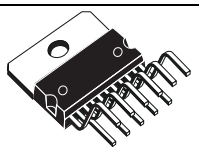
STA7360

20 W bridge/stereo audio amplifier with clipping detector

Features

- Very few external components
- No boucherot cells
- No bootstrap capacitors
- High output power
- No switch-on/off noise
- Very low standby current
- Fixed gain (20 db stereo)
- Programmable turn-on delay
- Clipping detector
- Standby function
- Protections
  - Output AC-DC short-circuit to ground and to supply voltage
  - Highly inductive loads
  - Loudspeaker protection
  - Overrating chip temperature
  - ESD protection



MULTIWATT11V

Description

The STA7360 is a class-AB audio power amplifier in the Multiwatt® package.Thanks to the fully complementary PNP/NPN output configuration, the high-power performance of the STA7360 is obtained without bootstrap capacitors.

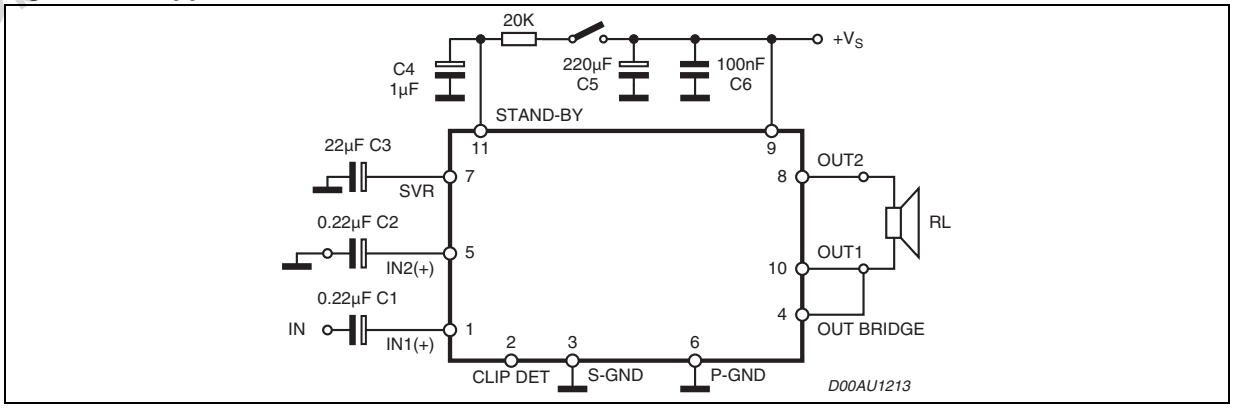
A delayed turn-on mute circuit eliminates audible on/off noise, and a short-circuit protection system prevents spurious intervention with highly inductive loads.

The device provides a circuit for the detection of clipping in the output stages. The output, an open collector, is able to drive systems with automatic volume control.

Table 1. Device summary

Order code	Package	Packing
STA7360	Multiwatt11V	Tube

Figure 1. Application circuit



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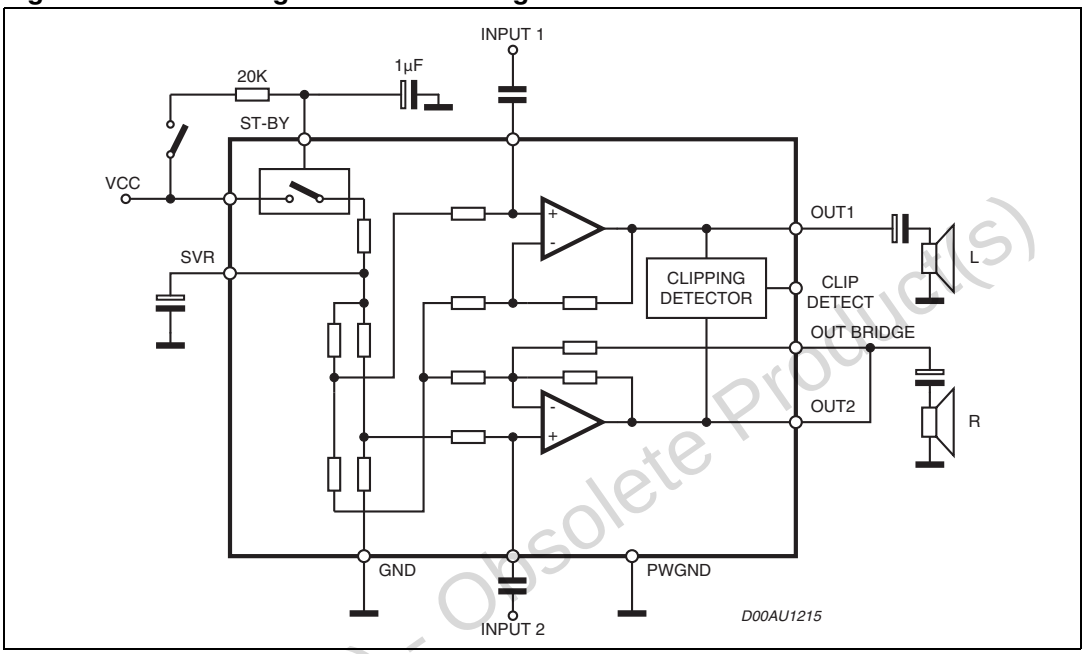
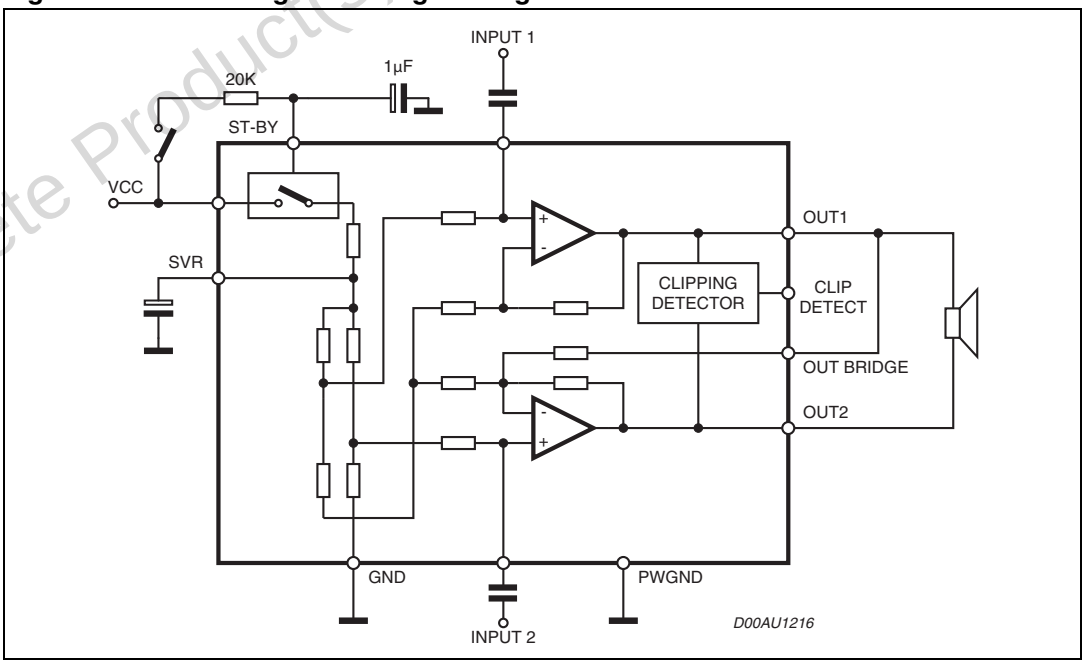
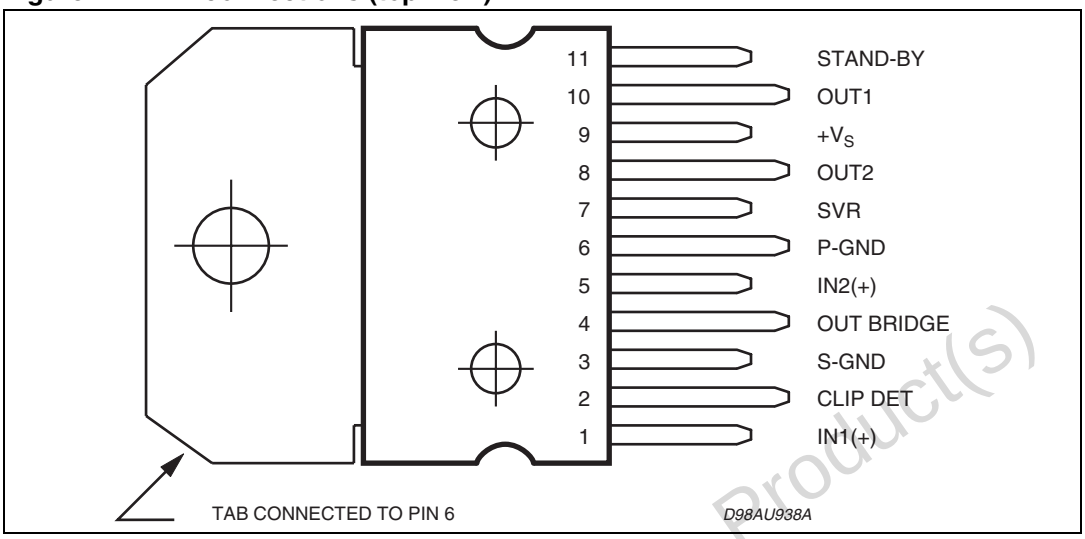


Figure 3. Block diagram - bridge configuration



1.2 Pin connections

Figure 4. Pin connections (top view)



2 Electrical specifications

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	22	V
I_O	Output peak current (non rep. for t = 100 µs)	5	A
I_O	Output peak current (rep. freq. > 10 Hz)	4	A
P_{tot}	Power dissipation at T_{case} = 85 °C	36	W
T_{stg}, T_J	Storage and junction temperature	-40 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-case (max)	1.8	°C/W

2.3 Electrical characteristics

Refer to the test circuits, T_{amb} = 25 °C, VS = 14.4 V, f = 1 kHz, unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage range		8		18	V
I_d	Total quiescent drain current	stereo configuration		65	120	mA
A_{SB}	Standby attenuation		60	80		dB
I_{SB}	Standby current				100	µA
V_{st_on}	Standby on threshold				1	V
V_{st_off}	Standby off threshold		3.5			V
I_{CO}	Clip detector prog. current	pin 2 pull-up to 5 V d = 1% with 10 kΩ d = 5 %		70 130		µA µA
Stereo						
P_O	Output power (each channel) THD = 10%	R_L = 2 Ω R_L = 3.2 Ω R_L = 4 Ω, 12 V R_L = 4 Ω	7	11 8 4.5 6.5		W W W W
d	Distortion	P_O = 0.1 to 2.5 W; R_L = 4 Ω P_O = 0.1 to 4 W; R_L = 3.2 Ω		0.05 0.05	0.5 0.5	% %
SVR	Supply voltage rejection	R_g = 10 kΩ C3 = 22 µF f = 100 Hz C3 = 100 µF	45	 62		dB dB
CT	Crosstalk	f = 1 kHz f = 10 kHz	45	 55		dB dB
R_I	Input resistance			50		kΩ
G_V	Voltage gain		19	20	21	dB
G_V	Voltage gain match				1	dB
E_{IN}	Input noise voltage	22 Hz to 22 kHz R_g = 50 Ω R_g = 10 kΩ R_g = ∞		2.5 3 3.5	5 7	µV µV µV
Bridge						
V_{OS}	Output offset voltage				250	mV
P_O	Output power THD = 10%	R_L = 4 Ω, 12 V R_L = 4 Ω, 14.4 V	16	15 20		W W
d	Distortion	P_O = 0.1 to 7 W; R_L = 4 Ω		0.05	0.5	%
SVR	Supply voltage rejection	R_g = 10 kΩ C3 = 22 µF f = 100 Hz C3 = 100 µF	45	 62		dB dB
R_I	Input resistance			50		kΩ
G_V	Voltage gain			26		dB
EIN	Input noise voltage	22 Hz to 22 kHz R_g = 50 Ω R_g = 10 kΩ		3.5 4		µV µV

2.4 Test and application circuits

Figure 5. Stereo test and application circuit

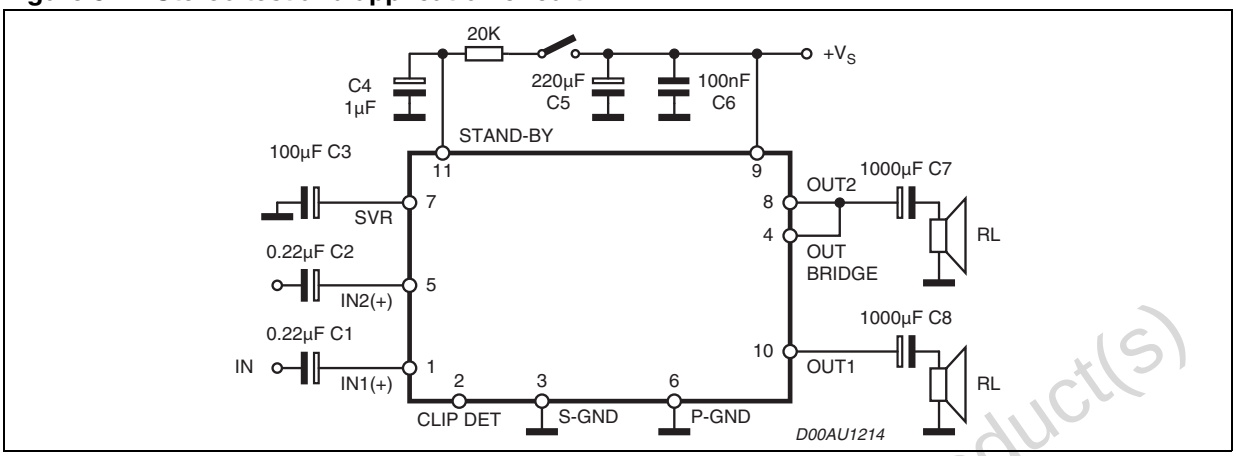


Figure 6. Board and layout of the stereo test and application circuit (1:1 scale)

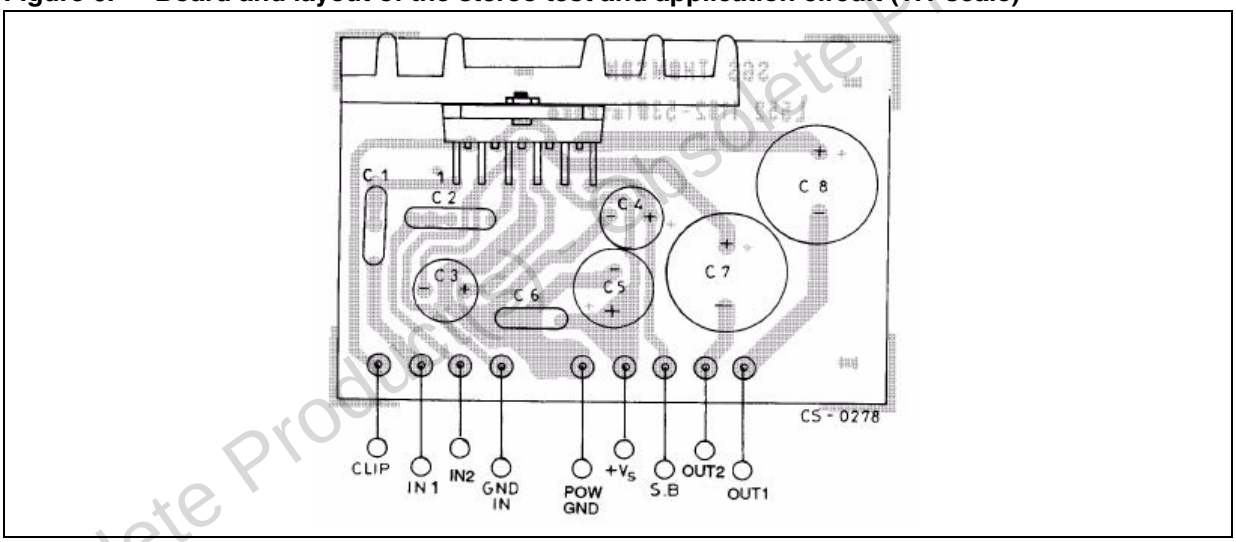


Table 5. Recommended values of the external components (stereo test and application circuit)

Comp.	Recommended value	Purpose	Larger than the recommended value	Smaller than the recommended value
C1	0.22 µF	Input decoupling (CH1)	-	-
C2	0.22 µF	Input decoupling (CH2)	-	-
C3	100 µF	Supply voltage rejection filtering capacitor	Longer turn-on delay	-Worse supply voltage rejection -Shorter turn-on delay -Danger of noise (pop)
C4	1 µF	Standby ON/OFF delay	Delayed turn-off with standby switch	Danger of noise (pop)

Table 5. Recommended values of the external components (stereo test and application circuit)

Comp.	Recommended value	Purpose	Larger than the recommended value	Smaller than the recommended value
C5	220 µF (min)	Supply bypass		Danger of oscillation
C6	100 nF (min)	Supply bypass		Danger of oscillation
C7	2200 µF	Output decoupling (CH2)	-Decrease of low-frequency cutoff -Longer turn-on delay	-Increase of low-frequency cutoff -Shorter turn-on delay
C8	2200 µF	Output decoupling (CH1)	-Decrease of low-frequency cutoff -Longer turn-on delay	-Increase of low-frequency cutoff -Shorter turn-on delay

Figure 7. Bridge test and application circuit

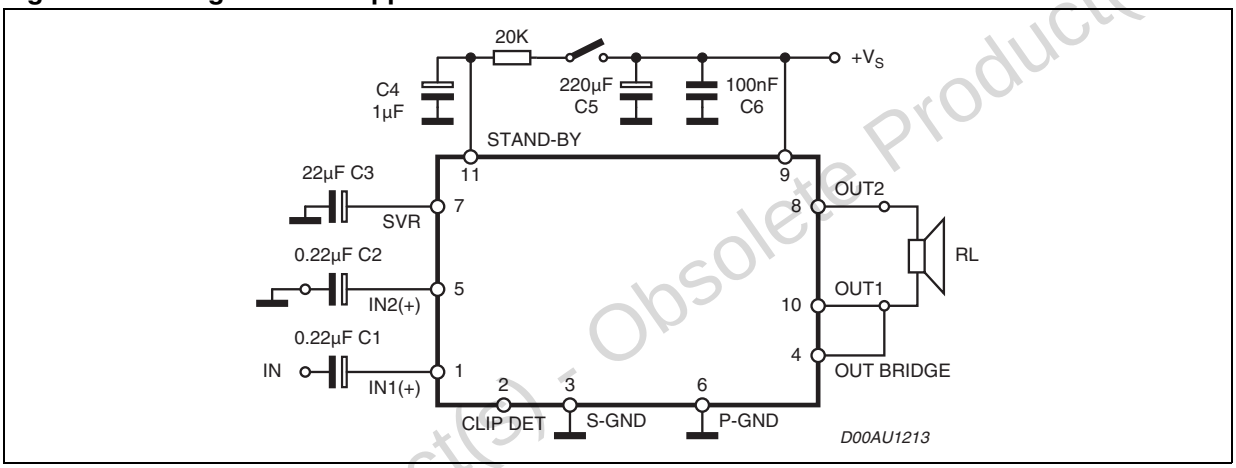
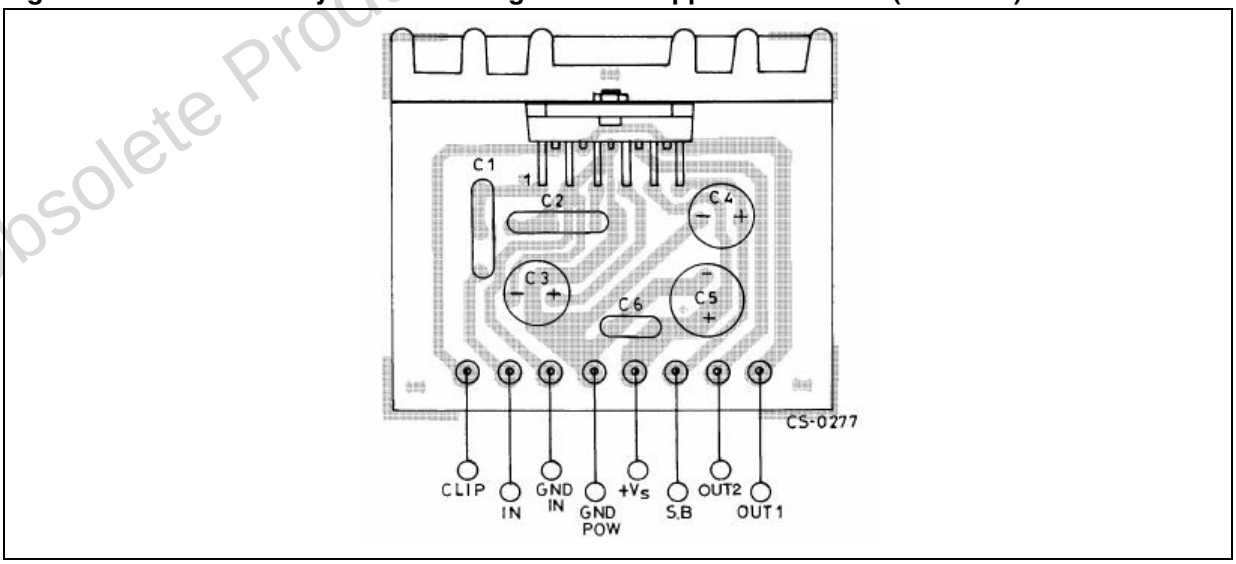


Figure 8. Board and layout of the bridge test and application circuit (1:1 scale)



3 Typical operating characteristics

Figure 9. Output power vs. supply voltage (stereo)

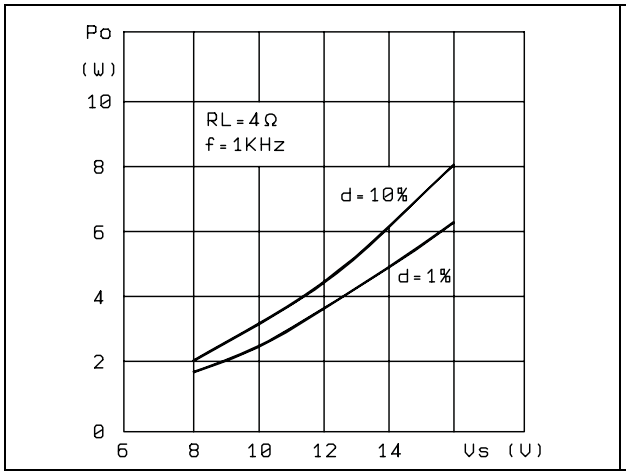


Figure 10. Output power vs. supply voltage (stereo)

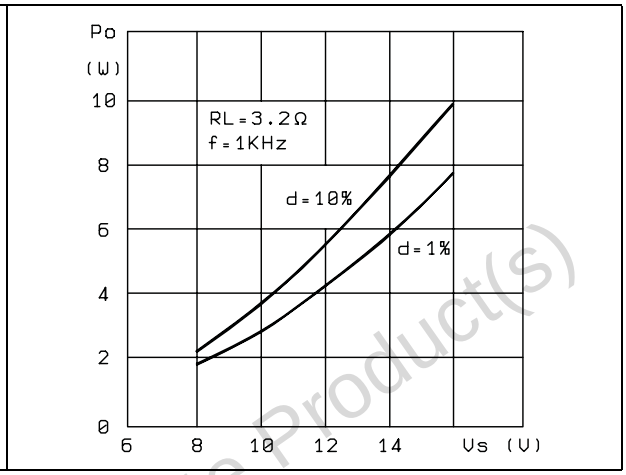


Figure 11. Output power vs. supply voltage (stereo)

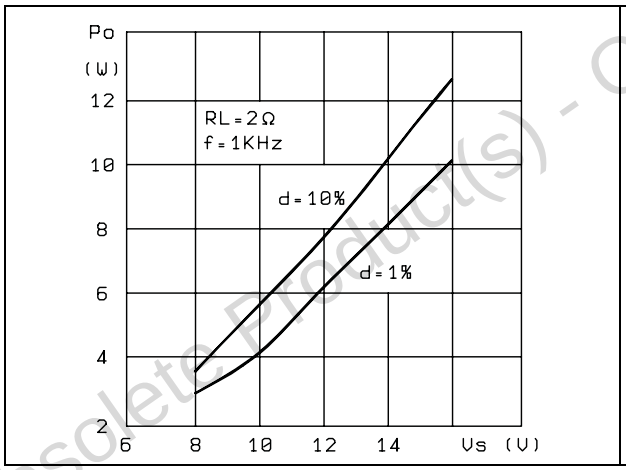


Figure 12. Output power vs. supply voltage (stereo)

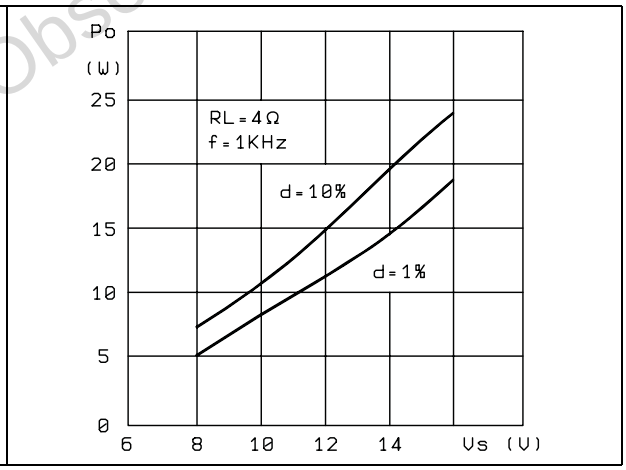


Figure 13. Drain current vs. supply voltage (stereo)

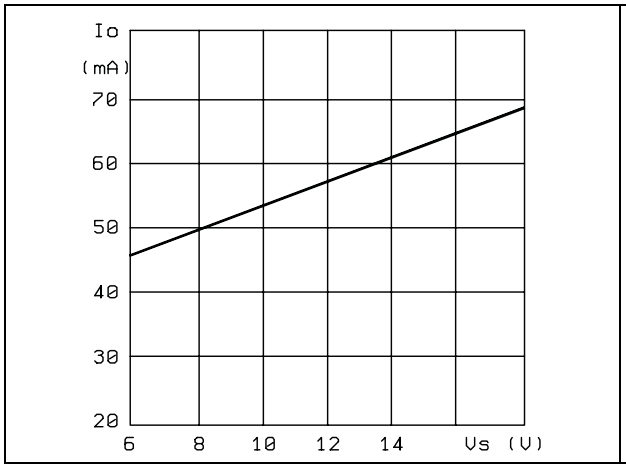


Figure 14. Distortion vs. output power (stereo)

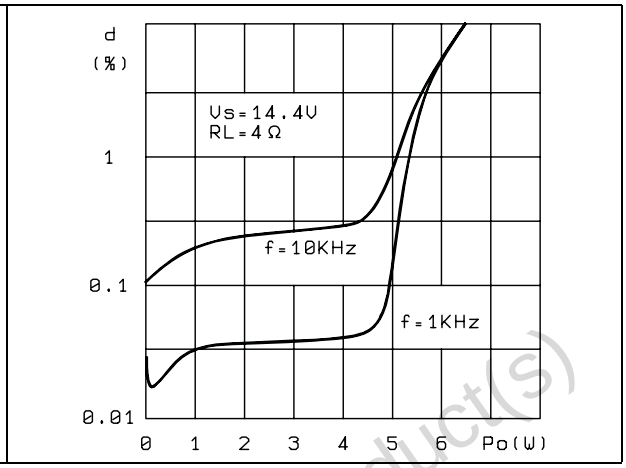


Figure 15. Distortion vs. output power (stereo)

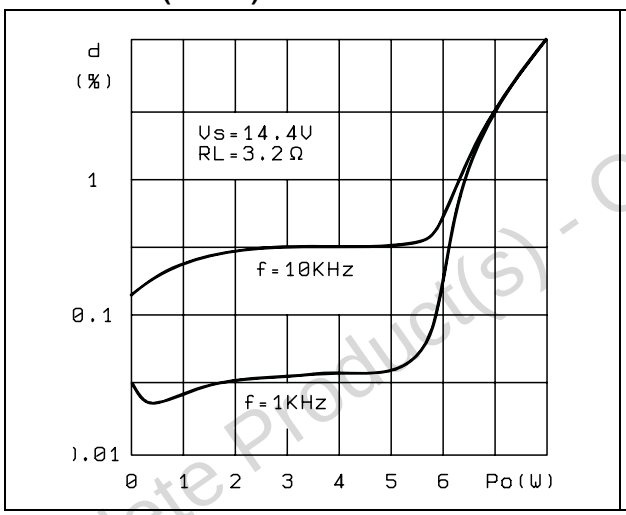


Figure 16. Distortion vs. output power (stereo)

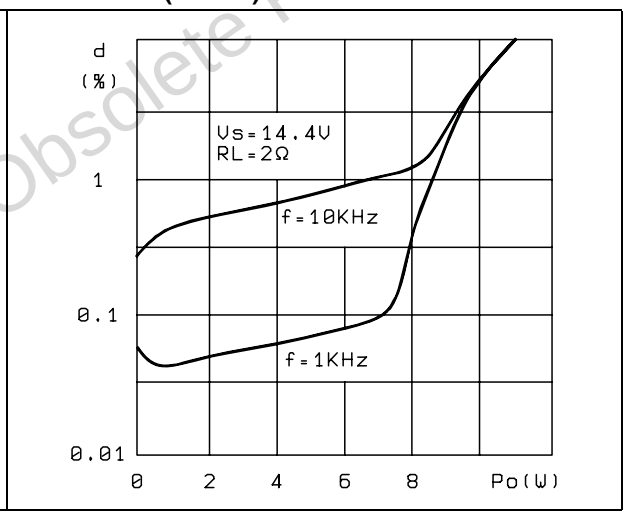


Figure 17. Distortion vs. output power (bridge)

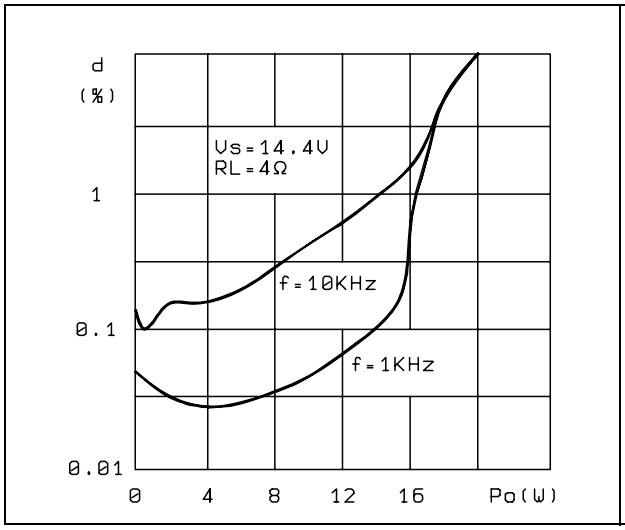


Figure 18. SVR vs. frequency & C3 (stereo)

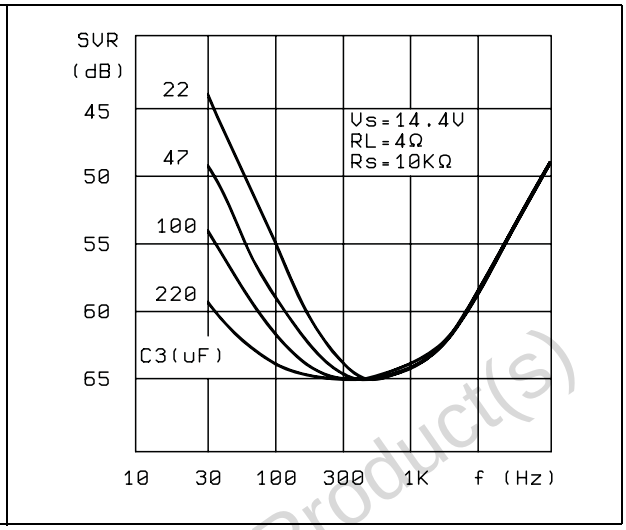


Figure 19. SVR vs. frequency & C3 (bridge)

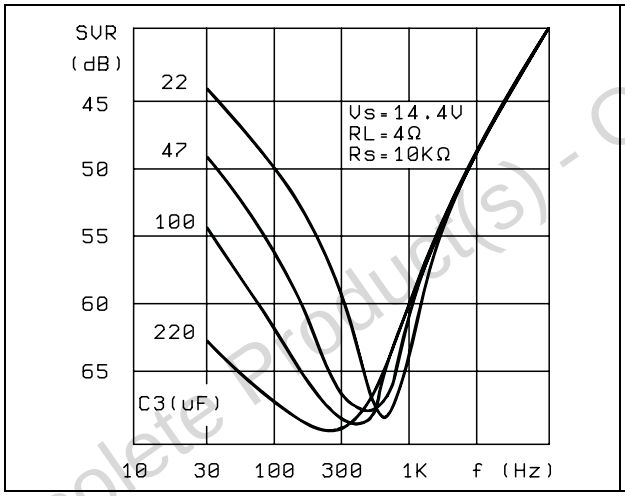


Figure 20. Crosstalk vs. frequency (stereo)

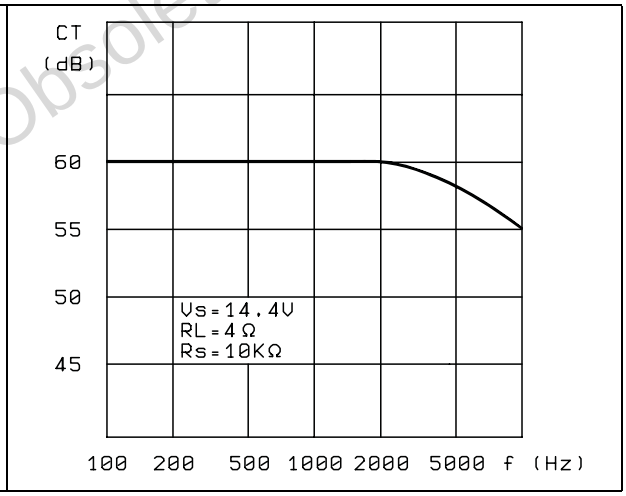


Figure 21. Power dissipation & efficiency vs. output power (stereo)

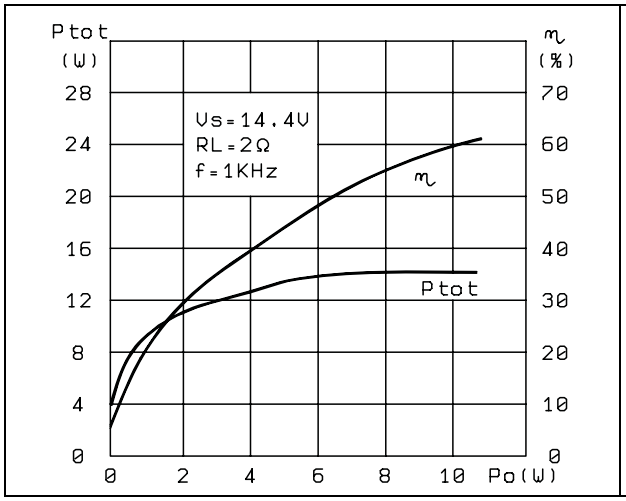


Figure 22. Power dissipation & efficiency vs. output power (stereo)

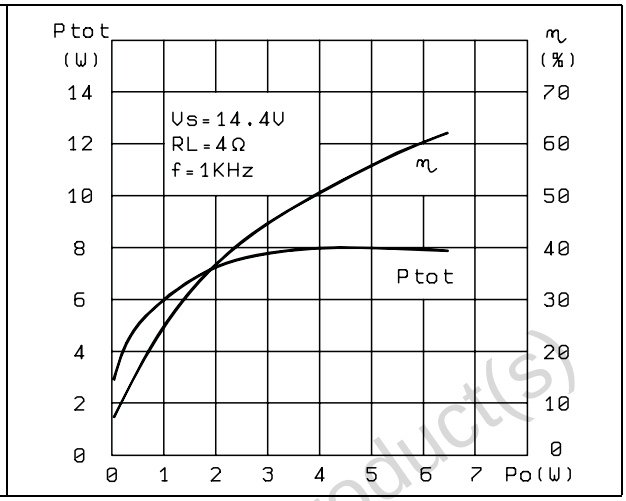
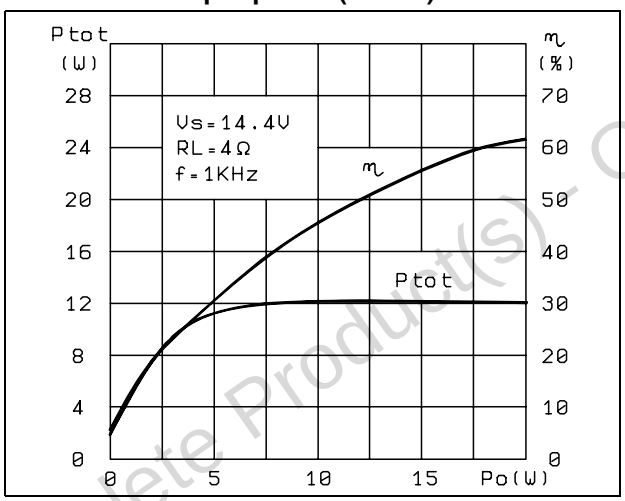


Figure 23. Power dissipation & efficiency vs. output power (stereo)



4 Block description

4.1 Polarization

The device is organized with the gain resistors directly connected to the signal ground pin i.e. without gain capacitors (*Figure 2*).

The non-inverting inputs of the amplifiers are connected to the SVR pin by means of resistor dividers, equal to the feedback networks. This allows the outputs to track the SVR pin which is sufficiently slow to avoid audible turn-on and turn-off transients.

4.2 SVR

The voltage ripple on the outputs is equal to the one on the SVR pin: with appropriate selection of CSVR, more than 60 dB of ripple rejection can be obtained.

4.3 Delayed turn-on (muting)

The CSVR sets a signal turn-on delay too. A circuit is included which mutes the device until the voltage on the SVR pin reaches ~2.5 V typ. (*Figure 25*). The mute function is obtained by duplicating the input differential pair (*Figure 24*); it can be switched to the signal source or to an internal mute input. This feature is necessary to prevent transients at the inputs reaching the loudspeaker(s) immediately after power-on).

Figure 25 represents the detailed turn-on transient with reference to the stereo configuration. At power-on the output decoupling capacitors are charged through an internal path but the device itself remains switched off (phase 1 of the represented diagram).

When the outputs reach the voltage level of about 1 V (this means that there are no short-circuits) the device switches on, the SVR capacitor starts charging itself and the output tracks exactly the SVR pin. During this phase the device is muted until the SVR reaches the "Play" threshold (~2.5 V typ.), after which the music signal starts being played.

4.4 Stereo/bridge switching

There is also no need for external components for changing from stereo to bridge configuration (*Figure 2*, *3*). A simple short-circuit between two pins allows phase reversal at one output, yet maintaining the quiescent output voltage.

4.5 Standby

The device is also equipped with a standby function, so that a low current, and hence a low cost switch, can be used for turn-on/off.

4.6 Stability

The device is provided with an internal compensation which allows reaching low values of closed loop gain. In this way better performances of the S/N ratio and SVR can be obtained.

Figure 24. Mute function diagram

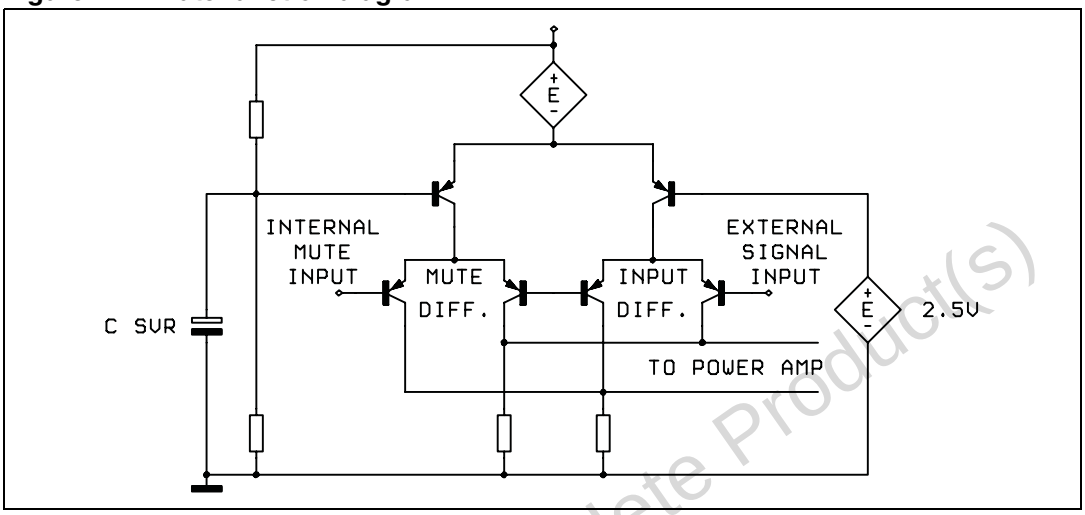


Figure 25. Turn-on delay circuit

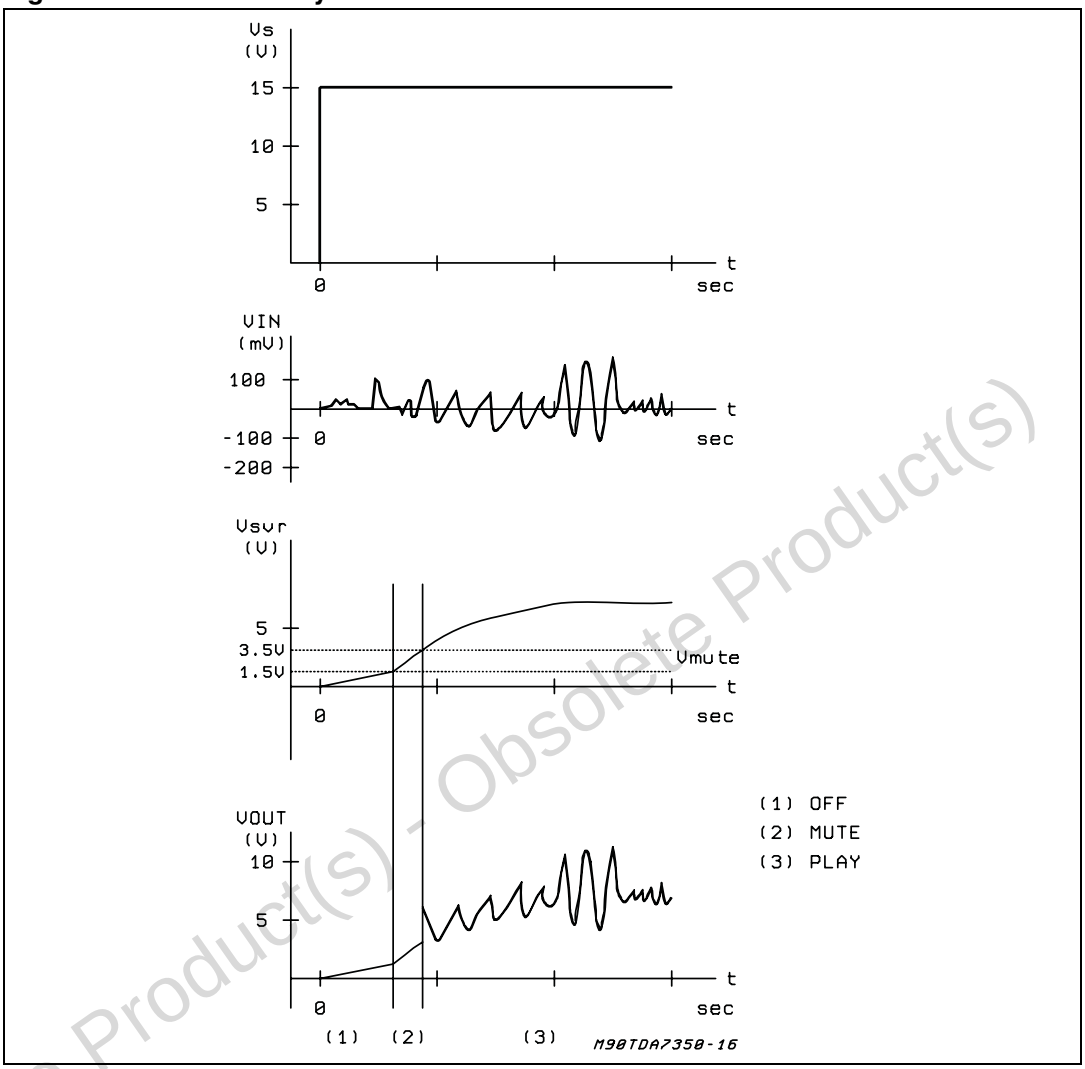
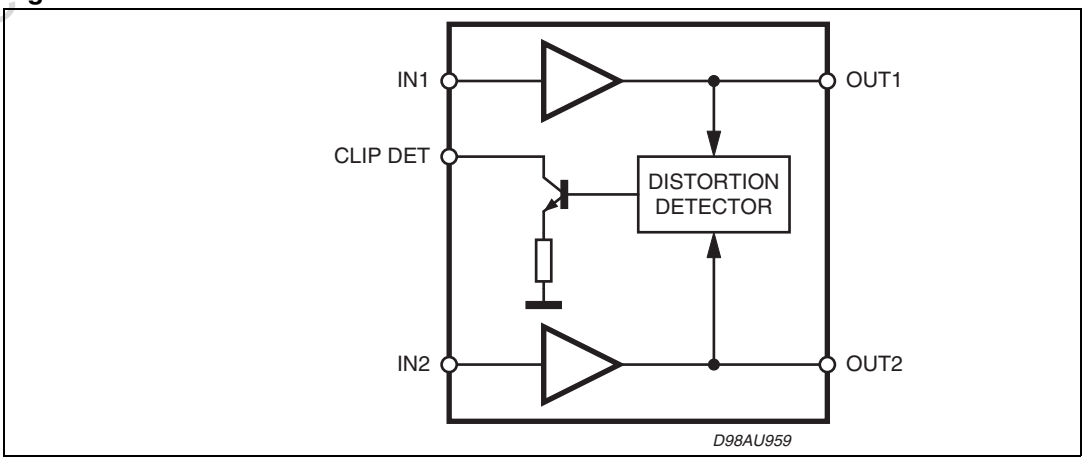


Figure 26. Dual-channel distortion detector



4.7 Output stage

Poor current capability and low cutoff frequency are well-known limits of the standard lateral PNP. Composite PNP-NPN power output stages have been widely used, regardless of their high saturation drop. This drop can be overcome only at the expense of external components, namely, the bootstrap capacitors. The availability of 4 A isolated collector PNP (ICV PNP) adds versatility to the design. The performance of this component, in terms of gain, VCEsat and cutoff frequency, is shown in *Figure 27*, *28*, and *29* respectively. It is realized in a new bipolar technology, characterized by top-bottom isolation techniques, allowing the implementation of low leakage diodes, too. It guarantees BVCEO > 20 V and BVCBO > 50 V both for NPN and PNP transistors. Basically, the connection shown in *Figure 30* has been chosen. First of all because its voltage swing is rail-to-rail, limited only by the VCEsat of the output transistors, which are in the range of 0.3 W each. Then, the gain VOUT/VIN is greater than unity, approximately 1+R2/R1. (VCC/2 is fixed by an auxiliary amplifier common to both channel). It is possible, controlling the amount of this local feedback, to force the loop gain (A * b) to less than unity at frequencies for which the phase shift is 180°. This means that the output buffer is intrinsically stable and not prone to oscillation.

Figure 27. ICV - PNP gain vs. I_C

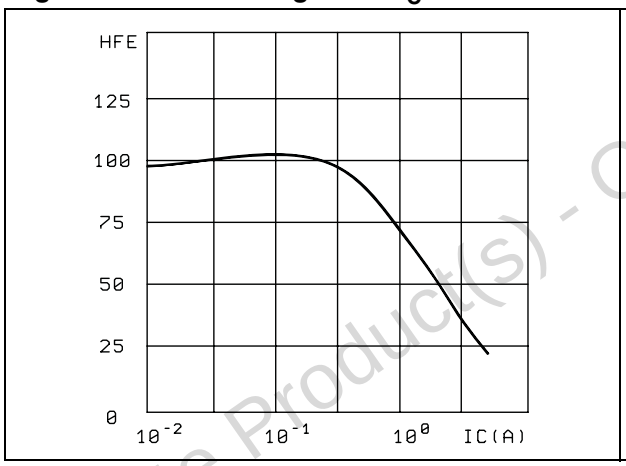


Figure 28. ICV - PNP VCE (sat) vs. I_C

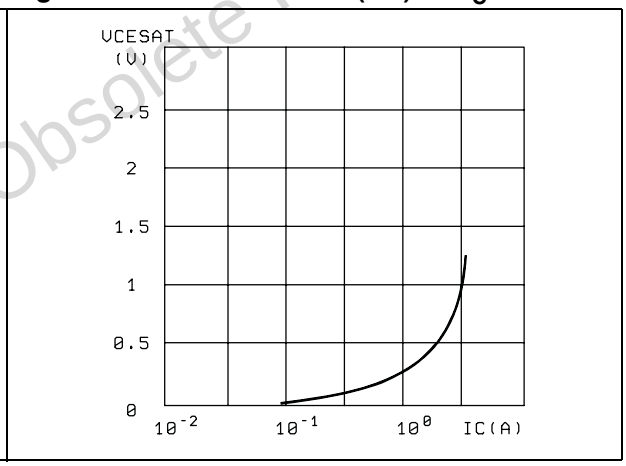


Figure 29. ICV - PNP cutoff frequency vs. I_C

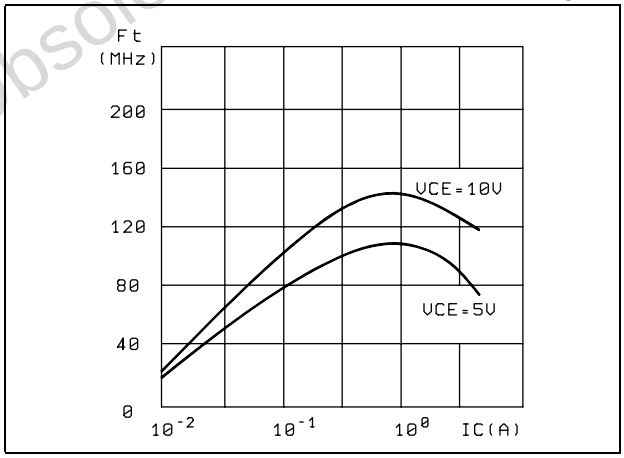
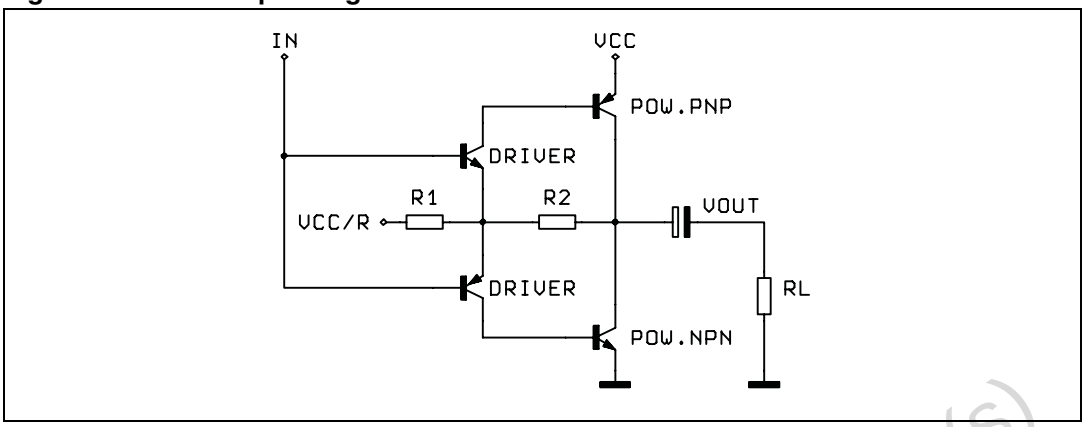


Figure 30. New output stage



In contrast, with the circuit of *Figure 31*, the solution adopted to reduce the gain at high frequencies is the use of an external RC network.

4.8 Amplifier block diagram

The block diagram of each voltage amplifier is shown in *Figure 32*. Regardless of production spread, the current in each final stage is kept low, with enough margin on the minimum, below which crossover distortion would appear.

Figure 31. Classical output stage

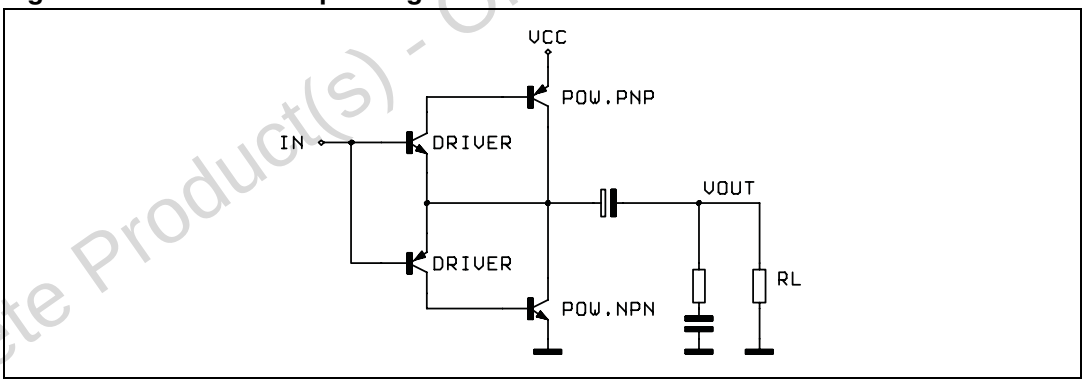
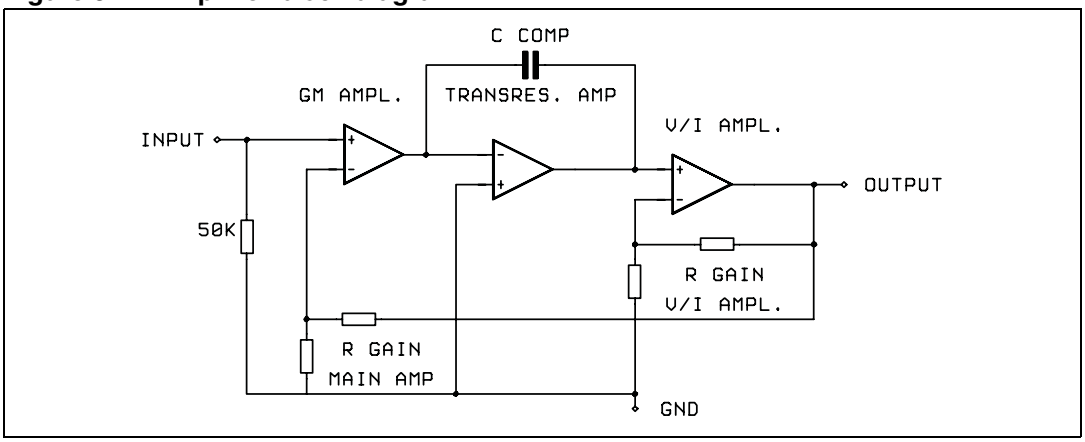


Figure 32. Amplifier block diagram



5 Built-in protection systems

5.1 Short-circuit protection

The maximum current the device can deliver can be calculated by considering the voltage that may be present at the terminals of a car radio amplifier and the minimum load impedance.

Apart from consideration concerning the area of the power transistors, it is not difficult to achieve peak currents of this magnitude (5 A peak).However, it becomes more complicated if AC and DC short-circuit protection is also required. In particular, with a protection circuit which limits the output current following the SOA curve of the output transistors, it is possible that in some conditions (highly reactive loads, for example) the protection circuit may intervene during normal operation. For this reason each amplifier has been equipped with a protection circuit that intervenes when the output current exceeds 4 A.

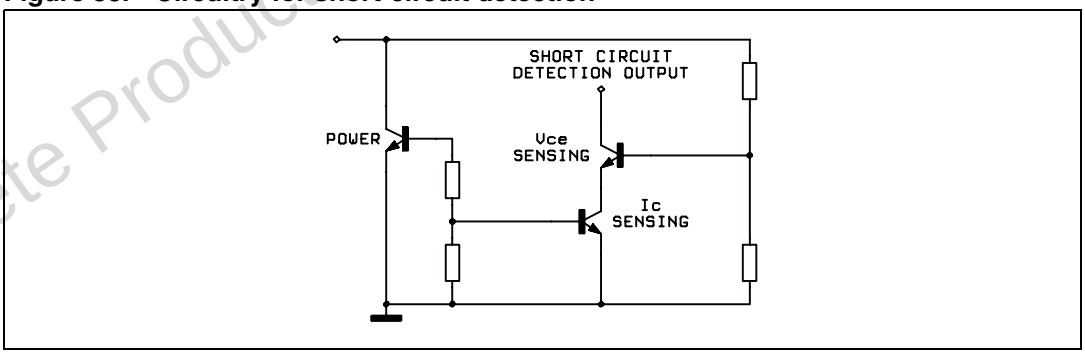
Figure 33 shows the protection circuit for an NPN power transistor (a symmetrical circuit applies to PNP). The VBE of the power is monitored and gives out a signal, available through a cascode.

This cascode is used to avoid the intervention of the short-circuit protection when the saturation is below a given limit.

The signal sets a flip-flop which forces the amplifier outputs into a high impedance state.

In case of DC short-circuit when the short-circuit is removed, the flip-flop is reset and restarts the circuit (*Figure 35*). In case of AC short-circuit or load shorted in bridge configuration, the device is continuously switched in ON/OFF conditions and the current is limited.

Figure 33. Circuitry for short-circuit detection



5.2 Polarity inversion

High current (up to 10 A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2 A fuse (normally connected in series with the supply). This features is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

5.3 DC voltage

The maximum operating DC voltage for the STA7360 is 18 V.

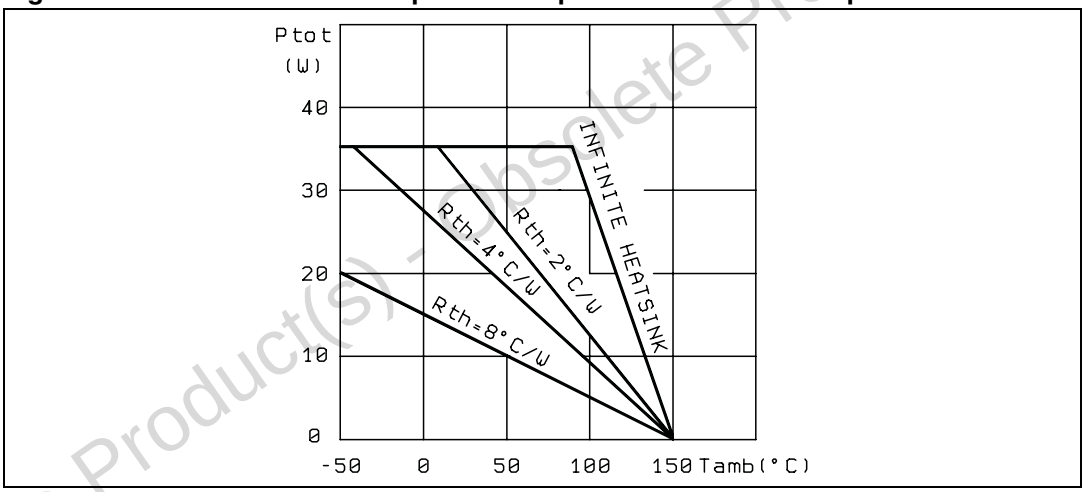
5.4 Thermal shutdown

The presence of a thermal limiting circuit offers the following advantages:

1. an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2. the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that Po (and therefore Ptot) and Id are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance). *Figure 34* shows the dissipable power as a function of ambient temperature for different thermal resistance.

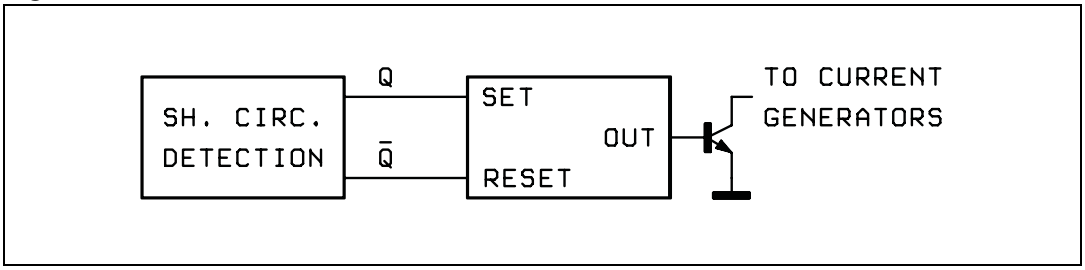
Figure 34. Maximum allowable power dissipation vs. ambient temperature



5.5 Loudspeaker protection

The STA7360 guarantees safe operations even for the loudspeaker in case of accidental short-circuit. Whenever a single OUT to GND, OUT to VS short-circuit occurs, both the outputs are switched OFF, thus limiting dangerous DC current flowing through the loudspeaker.

Figure 35. Restart circuit



6 Application hints

This section explains briefly how to get the best from the STA7360 and presents some application circuits with suggestions for the value of the components. These values can change depending on the characteristics that the designer of the car radio wants to obtain, or other parts of the car radio that are connected to the audio block.

To optimize the performance of the audio part it is useful (or indispensable) to analyze also the parts outside this block that can have an interconnection with the amplifier.

This method can provide components and system cost savings.

6.1 Reducing turn-on/off pop

The STA7360 has been designed in a way that the turn-on (off) transients are controlled through the charge (discharge) of the C_{svr} capacitor.

As a result of it, the turn-on (off) transient spectrum contents is limited only to the subsonic range. The following section gives some brief notes to get the best from this design feature (it will refer mainly to the stereo application which appears to be in most cases the more critical from the pop viewpoint. The bridge connection in fact, due to the common-mode waveform at the outputs, does not give a pop effect).

6.2 Turn-on

Figure 36 shows the output waveform (before and after the "A" weighting filter) compared to the value of C_{svr}.

Better pop-on performance is obtained with higher C_{svr} values (the recommended range is from 22 µF to 220 µF).

The turn-on delay (during which the amplifier is in mute condition) is essentially a function of C_{out}, C_{svr}.

$$T1 \approx 120 \bullet C_{out}$$

$$T2 \approx 1200 \bullet C_{svr}$$

The turn-on delay is given by:

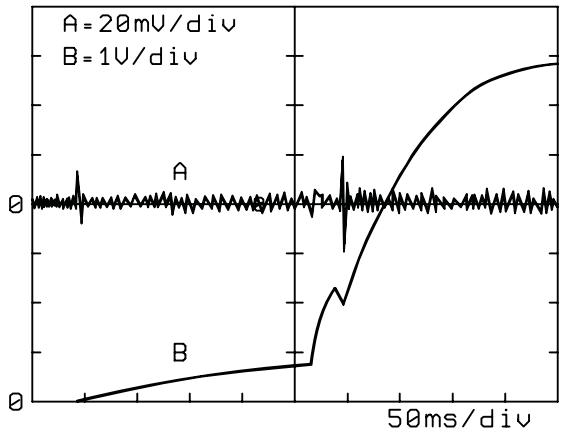
$$T1+T2 \text{ STEREO}$$

$$T2 \text{ BRIDGE}$$

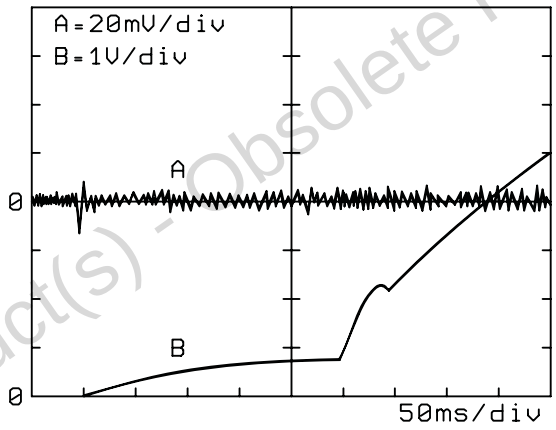
The best performance is obtained by driving the st-by pin with a ramp having a slope slower than 2 V/ms.

Figure 36. Turn-on output waveforms compared to the values of C_{svr}

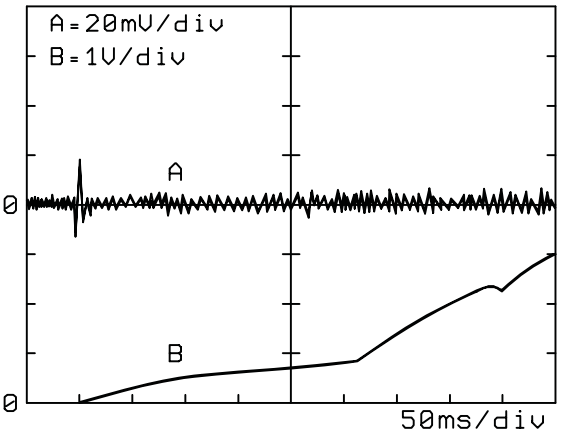
a) C_{svr} = 22 µF



b) C_{svr} = 47 µF



c) C_{svr} = 100 µF



6.3 Turn-off

A turn-off pop can occur if the st-by pin goes low with a short time constant. This pop is due to the fast switch-off of the internal current generator of the amplifier.

If the voltage present across the load becomes rapidly zero (due to the fast switchoff) a small pop occurs, depending also on C_{out}, R_{load}.

The parameters that set the switchoff time constant of the st-by pin are:

- the st-by capacitor (C4)
- the SVR capacitor (C_{svr})
- resistors connected from the st-by pin to the logical input (R_{ext})

6.4 Balanced input in bridge configuration

A helpful characteristic of the STA7360 is that, in bridge configuration, a signal present on both the input capacitors is amplified by the same amount and it is present in phase at the outputs, so this signal does not produce effects on the load. The typical value of CMRR is 46 dB.

Looking at *Figure 37*, we can see that a noise signal from the ground of the power amplifier to the ground of the hypothetical preamplifier is amplified of a factor equal to the gain of the amplifier (2 * Gv).

Using a configuration of *Figure 38* the same ground noise is present at the output multiplied by the factor 2 * Gv/200.

This means less distortion, less noise (e.g. motor cassette noise) and/or a simplification of the layout of PC board.

The only limitation of this balanced input is the maximum amplitude of common-mode signals (few tens of millivolt) to avoid a loss of output power due to the common-mode signal on the output, but in a large number of cases this signal is within this range.

Figure 37. Balanced input in bridge configuration, example 1

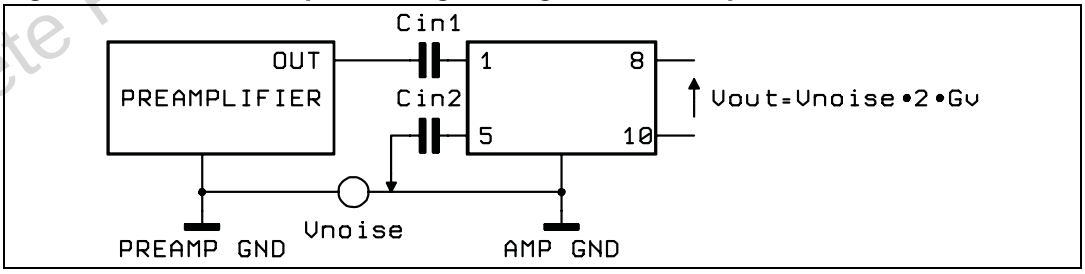
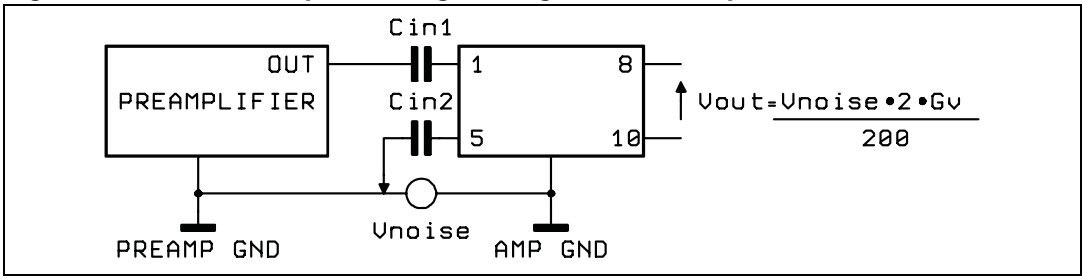


Figure 38. Balanced input in bridge configuration, example 2



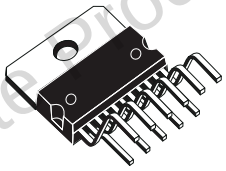
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

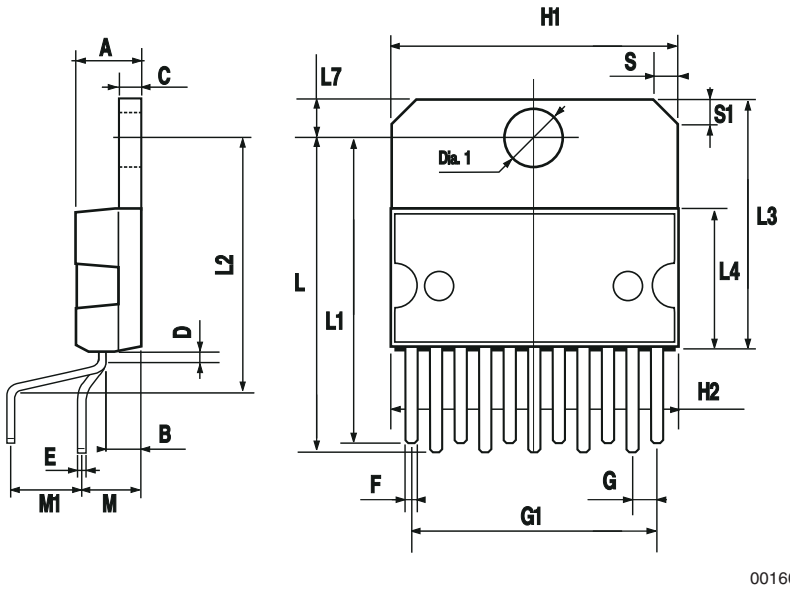
Figure 39. Multiwatt11V package mechanical data and dimensions.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.88		0.95	0.035		0.037
G	1.45	1.7	1.95	0.057	0.067	0.077
G1	16.75	17	17.25	0.659	0.669	0.679
H1	19.6			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.87	0.886
L2	17.4		18.1	0.685		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.73	5.08	5.43	0.186	0.200	0.214
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



Multiwatt11 (Vertical)



8 Revision history

Table 6. Document revision history

Date	Revision	Changes
Sep-2003	1	Initial release.
Nov-2005	2	Add V_{st_on} and V_{st_off} in electrical characteristics.
Jan-2006	3	Modified V_{st_on} max value in *Table 4*.
12-Dec-2011	4	Added *Table 1: Device summary* Updated ECOPACK® text in *Section 7: Package information* Revised document presentation, layout; minor textual updates

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