NCP590

Dual Output, High Accuracy, Ultra Low Dropout CMOS LDO

The NCP590 is a family of very high precision dual−output CMOS LDOs offered in a 2x2 DFN8 package. Each output is capable of delivering up to 300 mA and is available in voltages from 0.8 V to 5 V.

The set point output voltage is accurate to within ±0.9% with an operating voltage input up to 5.5 V. With its ultra low dropout characteristics and low quiescent and ground current consumption, the NCP590 is ideal for all battery operated consumer and microprocessor applications. The NCP590 is protected against short circuit and thermal overload conditions.

Features

- Dual Outputs, Each Supporting up to 300 mA Current
- Available in Output Combinations Ranging from 0.8 V to 5.0 V
- 2.1 V to 5.5 V V_{CC} Operating Supply Range
- Ultra−High Accuracy (0.9% max at 100 mA load & 25°C)
- Each Output has a Dedicated Enable Control Pin
- Enable Threshold Supports sub−1 V Systems
- Very Low Drop Out Voltage (50 mV typ @ 100 mA load)
- Low Noise (~20 μV_{rms}) without Bypass Capacitor
- Ultra Low Shutdown Current (0.2 μA)
- Low Quiescent and Ground Current (80 − 100 μA typ.)
- Thermal Shutdown and Current Limit Protection
- Active Output Discharge when Disabled
- No Minimum Output Current Required for Stability
- Requires C_{out} of only 1.0 μF (any ESR) for Stability
- Stable with Any Type of Capacitor (including MLCC) and Zero Load
- Input Under Voltage Lock Out (UVLO)
- Internally Compensated Regulator for Quick Transient Response
- Space−Efficient 2x2 DFN8 Package
- This is a Pb−Free Device

Applications

- Cellular Phones
- Cameras
- MP3/CD Players, PDA's, Camcorders
- DSP Supplies
- Portable Info−tronics
- PCMCIA Cards
- Networking Systems, DSL/Cable Modems

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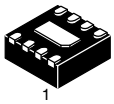
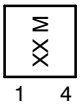


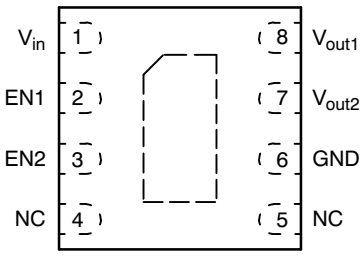
DFN8, 2x2
MN SUFFIX
CASE 506AA

MARKING DIAGRAM



XX = Specific Device Code
M = Date Code

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

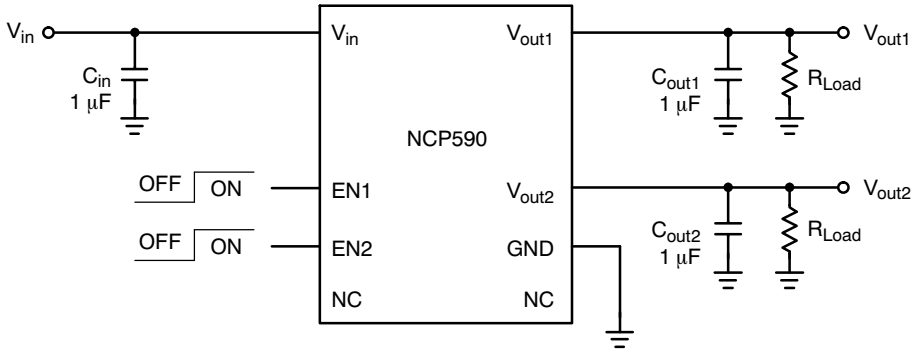


Figure 1. Typical Application

PIN FUNCTION

Pin No.	Symbol	Function
1	V_{in}	Input; Bypass directly at the IC with a 1 μF ceramic capacitor to Ground
2	EN1	Enable for output regulator 1; raise above 0.95 V to enable V_{out1}
3	EN2	Enable for output regulator 2; raise above 0.95 V to enable V_{out2}
4, 5	NC	NC; Do not make connection to these pins
6	GND	Ground
PAD	GND	The thermal pad should be connected to ground for best thermal performance. Float if necessary
7	V_{out2}	Output 2; Bypass to GND with a capacitor, 4.7 μF ≥ C ≥ 0.7 μF, any ESR
8	V_{out1}	Output 1; Bypass to GND with a capacitor, 4.7 μF ≥ C ≥ 0.7 μF, any ESR

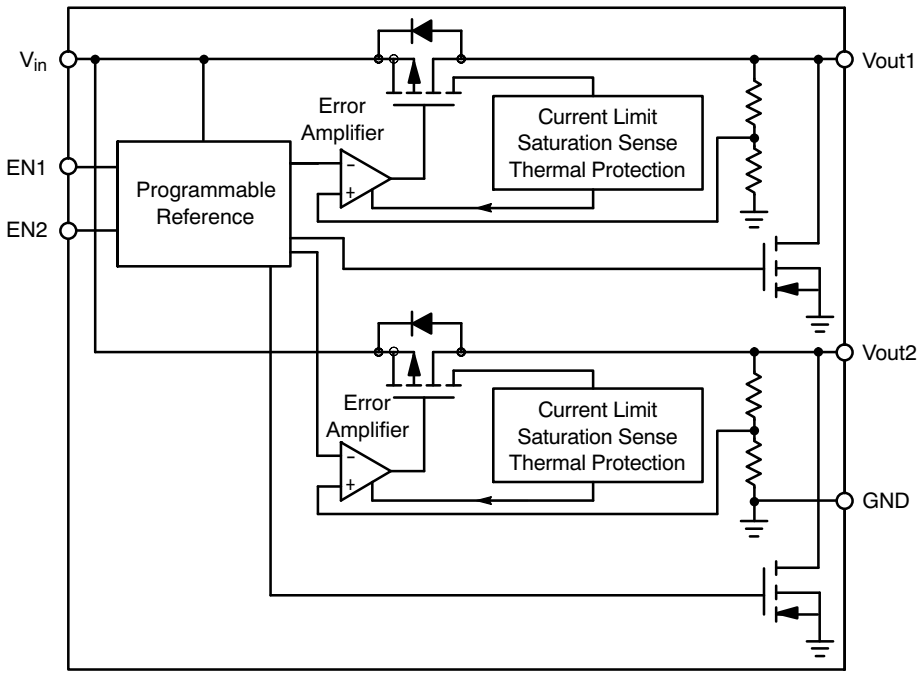


Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS T_J = −40°C to 125°C

Pin Symbol, Parameter		Symbol	Condition	Min	Max	Unit
V_{IN}, Input to regulator	Voltage	V_{IN}		−0.3	6.0	V
	Current	I_{IN}		−	Internally Limited	
V_{IN}, Input peak Transient Voltage to regulator wrt GND		V_{IN}			7.0	V
V_{OUT1}, V_{OUT2}, Regulated Output	Voltage	V_{OUT}		−0.3	V_{IN} + 0.3 or 6.0 (Note 1)	V
	Current	I_{OUT}		−	Internally Limited	
EN1, EN2, Enable Input		V_{EN}		−0.3	V_{IN} + 0.3 or 6.0 (Note 1)	V
Junction Temperature Storage Temperature		T_J T_{stg}		− −50	125 150	°C
ESD Capability, Human body model (Note 3)		ESD_{HB}		−2	2	kV
ESD Capability, Machine model (Note 3)		ESD_{MM}		−200	200	V
V_{outx}−V_{in} (Note 2)		V_{RB}		−	0.3	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Which ever limit is lower
2. Exceeding this value will turn on the body diode of the PMOS driver (reference Figure 2).

THERMAL RESISTANCE

Parameter		Symbol	Condition	Value	Unit
Junction−to−Ambient	2X2 DFN 1 oz Cu	θ_{JA}	207.0 sq mm 1 oz Cu 54.2 sq mm 1 oz Cu 20.2 sq mm 1 oz Cu	158 210 375	°C/W
Junction−to−Ambient	2X2 DFN 2 oz Cu	θ_{JA}	207.0 sq mm 2 oz Cu 54.2 sq mm 2 oz Cu 20.2 sq mm 2 oz Cu	133 184 330	°C/W
Junction−to−Board	2X2 DFN	Psi_{JB}		36.4	°C/W
Lead Temperature Soldering, (Note 4) Reflow (SMD styles only), lead free		T_{sld}	60 −150 sec above 217 40 sec max at peak	265 pk	°C
Moisture Sensitivity Level		MSL		1	

3. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
4. Per IPC/JEDEC J−STD−020C

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$ (Note 5); $V_{IN} = V_{OUT}$ +0.5 V or 2.1 V, whichever is greater (Note 6). $V_{EN1,2}$ = 0.95 V, $C_{IN} = C_{OUT1,2}$ = 1.0 μF, unless noted otherwise

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Regulators						
Input Voltage	V_{IN}	** which ever limit is greater	$V_{out(max)}$ + 0.5 or 2.1 V**	–	5.5	V
Enable Input Voltage	V_{EN}	* which ever limit is lower	0.0	–	V_{IN}+ 0.3 or 5.5*	V
Voltage Accuracy	V_{OUT}	I_{OUT} = 100 mA, T_A = 25°C (Note 11)	−0.9	–	+0.9	%
Voltage Accuracy	V_{OUT}	I_{OUT} = 1 mA to 200 mA $-40\ °C \le T_A \le 85°C$ (Notes 9, 11, 12)	−1.9	–	+1.9	%
Overall Voltage Accuracy	V_{OUT}	I_{OUT} = 1 mA to 200 mA, V_{IN} = (V_{OUT} +0.5 V) to 5.5 V, 2.1 V_{INmin} $0°C \le T_A \le 85°C$, (Notes 12, 13)	−2.4	–	+2.4	%
Line Regulation (Note 7)	ΔV_{OUT}	I_{OUT} = 1.0 mA V_{IN} = (V_{out} + 0.5 V) to 5.5 V, V_{INmin} = 2.1 V	–	±0.05	–	%/V
Load Regulation (Note 7)	ΔV_{OUT}	I_{OUT} = 1 mA to 200 mA	−0.012	−0.005	0.012	%/mA
Drop−out Voltage, (Note 8)	V_{DO}	I_{OUT} = 50 mA	–	23	40	mV
Drop−out Voltage, (Note 8)	V_{DO}	I_{OUT} = 100 mA	–	52	85	mV
Drop−out Voltage, (Note 8)	V_{DO}	I_{OUT} = 150 mA	–	80	125	mV
Drop−out Voltage, (Note 8)	V_{DO}	I_{OUT} = 200 mA	–	110	170	mV
Drop−out Voltage, (Note 8)	V_{DO}	I_{OUT} = 300 mA	–	165	225	mV
Quiescent Current; $I_q = I_{IN} - I_{OUT}$	I_q	V_{EN1} = 0.95 V, I_{OUT1} = 0 mA; V_{EN2} = 0.4 V, I_{OUT2} = 0 mA OR V_{EN2} = 0.95 V, I_{OUT2} = 0 mA; V_{EN1} = 0.4 V, I_{OUT1} = 0 mA One Regulator ON; One Regulator OFF	–	80	125	μA
Quiescent Current; $I_q = I_{IN} - I_{OUT}$	I_q	$I_{OUT1} = I_{OUT2}$ = 0 mA Both Regulators ON	–	115	195	μA

5. Performance guaranteed over specified operating range by design, guard banded test limits, and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. V_{OUT} based on the greater of the two outputs.
7. Overall accuracy specified over specified operating conditions of line, load, and temperature.
8. Drop out voltage $V_{DO} = V_{IN} - V_{OUT}$ measured when the output voltage has dropped 100 mV from the nominal value for $V_{OUT} > 2.0$ V.
9. Guaranteed by design, not production tested.
10. Regulated and stable output over full load range down to 0 mA load.
11. V_{IN} is set at V_{IN} = ((V_{OUT} + 0.5 V) + 5.5 V) / 2 or V_{IN} = ((2.1 V) + 5.5 V) / 2, whichever is greater.
12. Applicable for $V_{OUT} > 1.2$ V.
13. For all output voltages and −40°C to 85°C overall voltage accuracy is 2.9%.
14. Typical disable current is in the nA.

ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le 85°C$ (Note 5); $V_{IN} = V_{OUT}$ +0.5 V or 2.1 V, whichever is greater (Note 6). $V_{EN1,2}$ = 0.95 V, $C_{IN} = C_{OUT1,2}$ = 1.0 μF, unless noted otherwise

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Regulators							
Ground Current; $I_{GND} = I_{IN} - I_{OUT}$		I_{GND}	V_{EN1} = 0.95 V, I_{OUT1} = 200 mA; V_{EN2} = 0.4 V, I_{OUT2} = 0 mA OR V_{EN2} = 0.95 V, I_{OUT2} = 200 mA; V_{EN1} = 0.4 V, I_{OUT1} = 0 mA One Regulator ON; One Regulator OFF	–	105	150	μA
Ground Current; $I_{GND} = I_{IN} - I_{OUT}$		I_{GND}	$I_{OUT1} = I_{OUT2}$ = 200 mA Both Regulators ON	–	175	250	μA
Disable Current; $I_{DIS} = I_{IN} - I_{OUT}$		I_{DIS}	$I_{OUT1,2}$ = 0 mA, $V_{EN1,2}$ = 0.4 V Both Regulators OFF	0	(Note 14)	1	μA
I_{Load}	Load Current (Note 10)	I_{OUT}		0	–	–	mA
	Maximum Output Current	I_{OUT}		300	–	–	mA
Current Limit, per Regulator (Note 9)		I_{SC}	V_{OUT} = 0 V	–	750	–	mA
Output Noise Voltage (Note 9)		e_n	BW = 10 Hz to 100 kHz V_{OUT} = 0.8 V V_{OUT} = 2.8 V	– –	20 30	– –	μV_{RMS}
Thermal Shutdown (Note 9)		T_{jSD}	Junction Temperature	–	155	–	°C
			Hysteresis	–	15	–	
Input under voltage lock out		UVLO		–	1.9	2.1	V
UVLO hysteresis		$UVLO_{hys}$		–	0.1	–	V
Power Supply Rejection Ratio (Note 9)		PSRR	I_{OUT} = 200 mA 120 Hz 0.8 V output 120 Hz 1.8 V output 120 Hz 2.8 V output	 – – –	 60 55 50	 – – –	dB
Power Supply Rejection Ratio (Note 9)		PSRR	I_{OUT} = 200 mA 1 KHz 2.8 V output	–	40	–	dB
Enable Control Characteristics							
Maximum Input Current at EN Input		I_{EN}	V_{EN} = 0.0 V	–	0.01	–	μA
			$V_{EN} = V_{IN}$	–	0.01	–	
Low Input Threshold		V_{IL}		–	–	0.4	V
High Input Threshold		V_{IH}		0.95	–	–	V
Timing Characteristics							
Turn On Time Delay, Both outputs turned on with ENABLE		T_{ON}	To 95% ΔV_O $V_{IN(MIN)}$ to 5.5 V	–	375	700	μs
Turn Off Time Delay, Both outputs turned off with ENABLE (Note 9)		T_{OFF}	V_{IN} = 5.5 V V_{OUT} = 5 V, to V_{OUT} = 250 mV V_{OUT} = 0.8 V, to V_{OUT} = 40 mV	 – –	 215 155	 – –	 μs μs
Recommended Output Capacitor Specifications							
Output Capacitance (Note 9)		C_{OUT}	Capacitance over full temperature range of application. Any ESR	0.7	1.0	4.7	μF

5. Performance guaranteed over specified operating range by design, guard banded test limits, and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
6. V_{OUT} based on the greater of the two outputs.
7. Overall accuracy specified over specified operating conditions of line, load, and temperature.
8. Drop out voltage $V_{DO} = V_{IN} - V_{OUT}$ measured when the output voltage has dropped 100 mV from the nominal value for $V_{OUT} > 2.0$ V.
9. Guaranteed by design, not production tested.
10. Regulated and stable output over full load range down to 0 mA load.
11. V_{IN} is set at $V_{IN} = ((V_{OUT} + 0.5\ V) + 5.5\ V) / 2$ or $V_{IN} = ((2.1\ V) + 5.5\ V) / 2$, whichever is greater.
12. Applicable for $V_{OUT} > 1.2$ V.
13. For all output voltages and −40°C to 85°C overall voltage accuracy is 2.9%.
14. Typical disable current is in the nA.

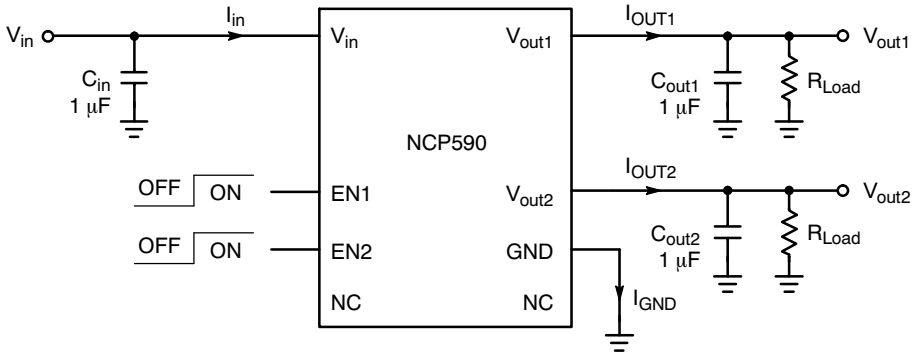


Figure 3. Measuring Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

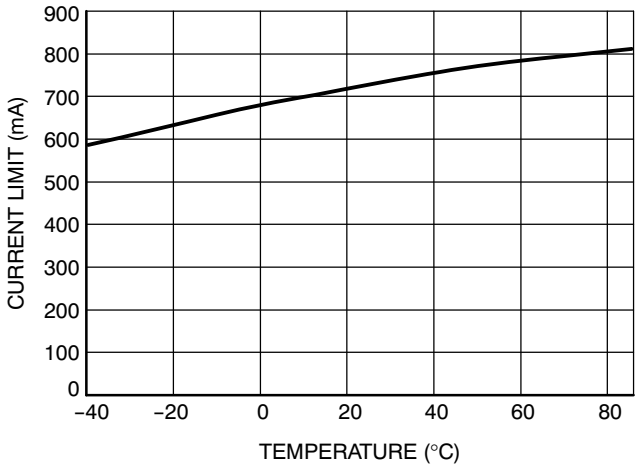


Figure 4. Current Limit vs. Temperature

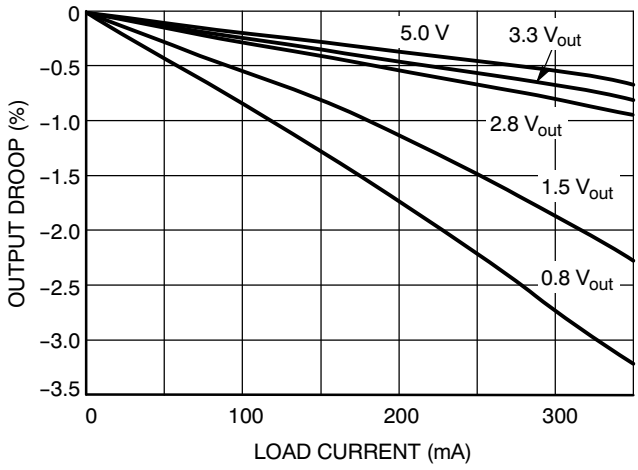


Figure 5. Typical Output Voltage Variation vs. Load Current

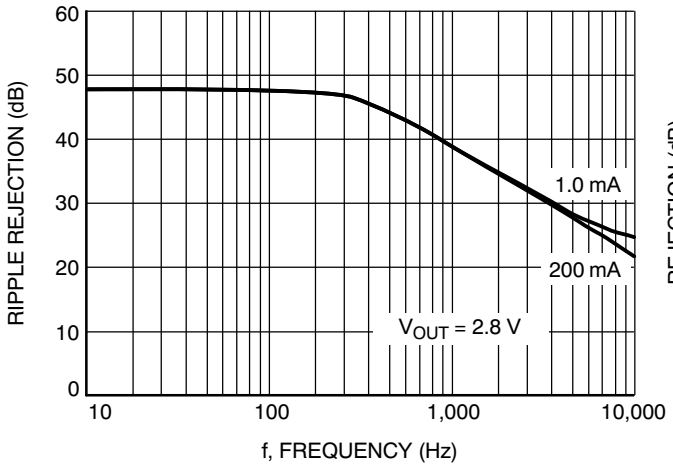


Figure 6. Power Supply Rejection Ratio

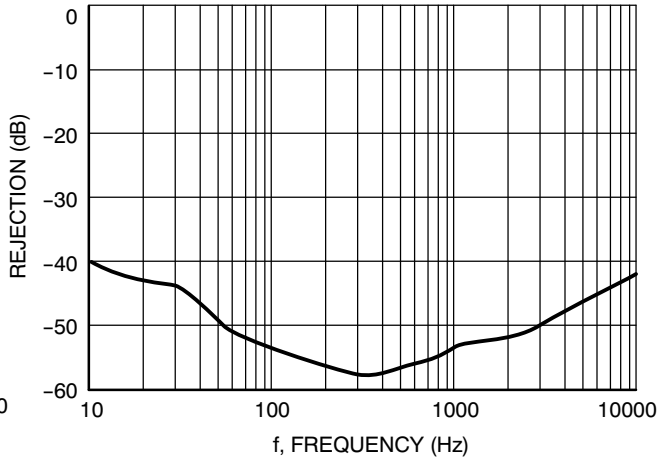


Figure 7. Cross Channel Rejection vs. Frequency

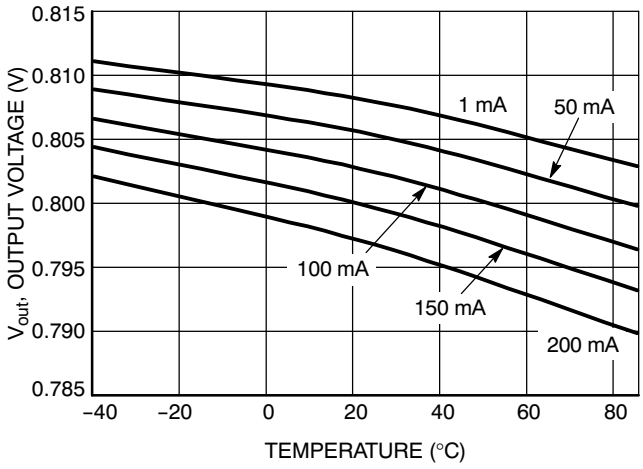


Figure 8. Output Voltage Change vs. Temperature for 0.8 V_{out}

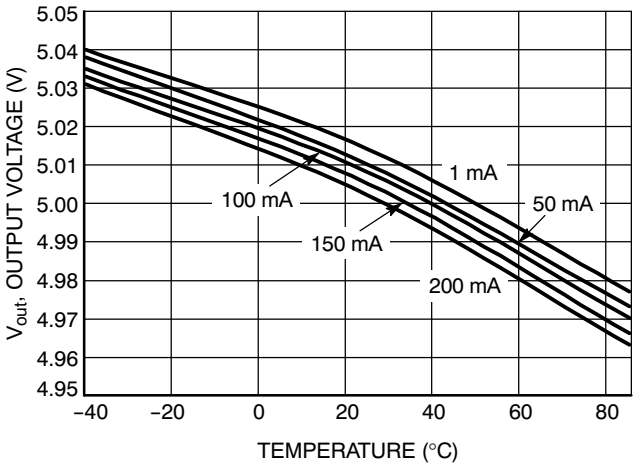


Figure 9. Output Voltage Change vs. Temperature for 5.0 V_{out}

TYPICAL PERFORMANCE CHARACTERISTICS

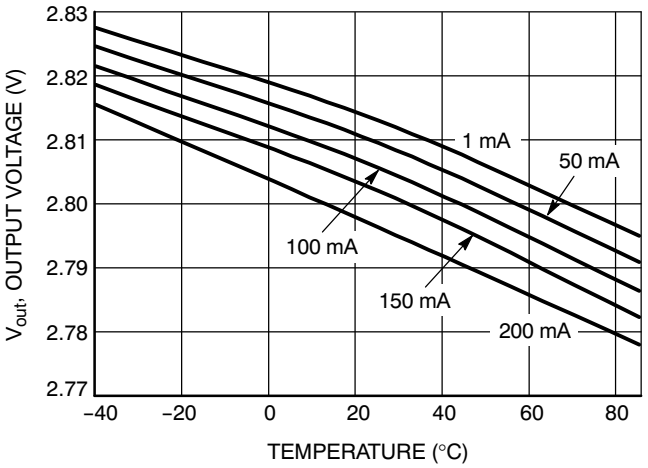


Figure 10. Output Voltage Change vs. Temperature for 2.8 V_{out}

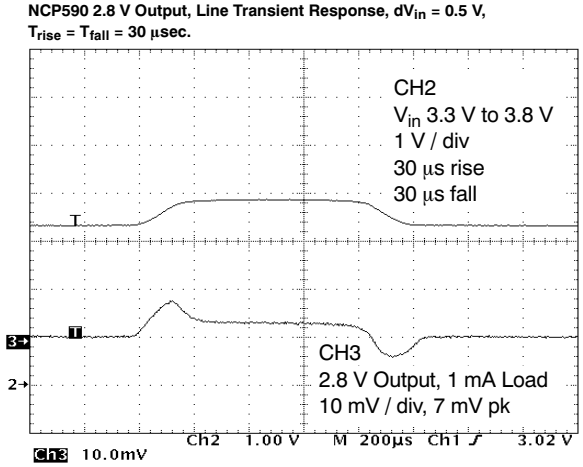


Figure 11. 2.8 V_{out} vs. Line Transient

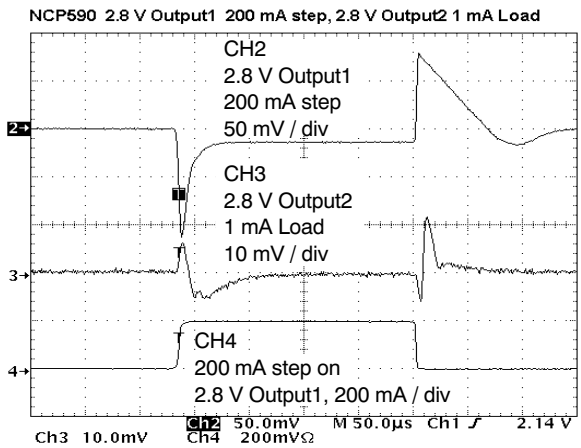


Figure 12. Load Transient on 2.8 V_{out} and Effect on 2.8 V_{out} for 200 mA Step

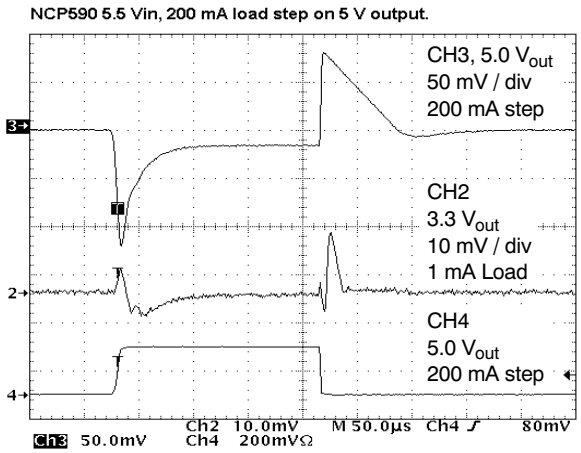


Figure 13. Load Transient on 5.0 V_{out} and Effect on 3.3 V_{out} for 200 mA Step

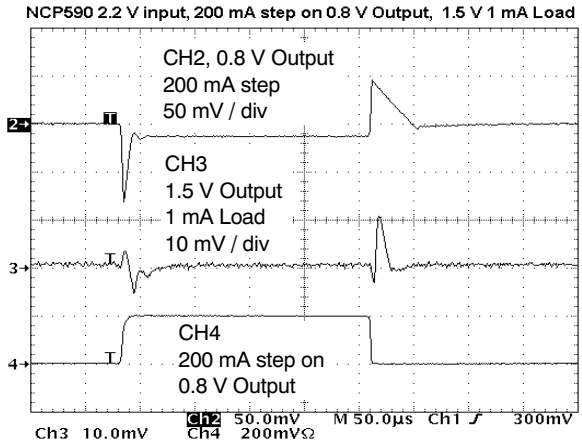


Figure 14. Load Transient on 0.8 V_{out} and Effect on 1.5 V_{out} for 200 mA Step

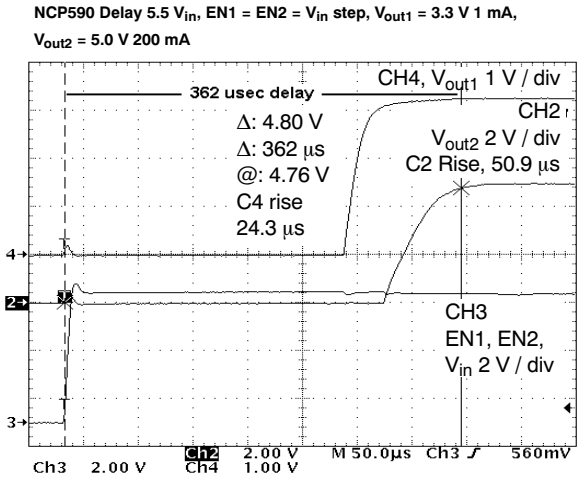


Figure 15. Typical Turn−on Delay for 3.3 V_{out} 1 mA, 5.0 V_{out} 200 mA Output with Simultaneous V_{in} and Enable

APPLICATION INFORMATION

Output Regulator

The output is controlled by a precision trimmed reference and error amplifier. The output has saturation control for regulation while the input voltage is low, preventing over saturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

Standard linear regulator design circuitry consists of only an active output driver providing current at the regulated voltage with resistors from the regulated output to ground (used in the feedback loop). This provides good turn−on characteristics from the active PFET output driver, but turn−off characteristics are determined by the output capacitor values and impedance of the load in parallel with the internal resistors in the feedback loop. The turn−off time in the situation with high impedance loads will be slow. The NCP590 has active pull−down transistors which turn on during device turn−off creating efficient fast turn−offs independent of loading.

Stability Considerations

The input capacitor C_{in} in Figure 3 is necessary to provide low impedance to the input of the regulator.

The output or compensation capacitor C_{outx} helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

Stability is guaranteed at values C_{OUT} = 0.7 μF to 4.7 μF and any ESR within the operating temperature range.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure x) is:

$$P_D = (V_{IN} - V_{OUT1}) \times I_{OUT1} + (V_{IN} - V_{OUT2}) \times I_{OUT2} + V_{IN} \times I_{GND} \quad (1)$$

where:

V_{IN} is the maximum input voltage,

V_{OUT} is the output voltage for each output,

I_{OUT} is the output current for each output in the application, and

I_{GND} is the quiescent or ground current the regulator consumes at I_{OUT}.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = (125°C - T_A) / P_D \quad \text{(eq. 1)}$$

The value of $R_{\theta JA}$ can then be compared with those in the thermal resistance section of the data sheet. Those board areas with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 125°C. In some cases, none of the circuit board areas will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required. The current flow and voltages are shown in the Measurement Circuit Diagram. A chart showing thermal resistance vs. pcb heat spreader area is shown below.

Enable

Enabling the two outputs is controlled by two independent pins, EN1 and EN2. A high (above the high input threshold) on these logic level input pins causes the outputs to turn on.

Normal operation allows for input voltages to these pins to 0.3 V above V_{IN}. It is sometimes necessary to interface logic outputs from different operating voltages into these pins. This happens when standard operating system voltages must interface together (i.e., 5 V to 3.3 V systems).

For example, a 5 V control voltage is needed to control the NCP590 operating with V_{IN} = 3.6 V. The input current into the ENx pin can be kept to safe levels by adding a 100 k resistor in series with the 5 V control drive voltage. This will keep the input voltage in compliance with the maximum ratings and will allow control of the output. Use of this setup will affect turn−on time and will increase the enable current higher than the input current specified in the electrical parameter tables.

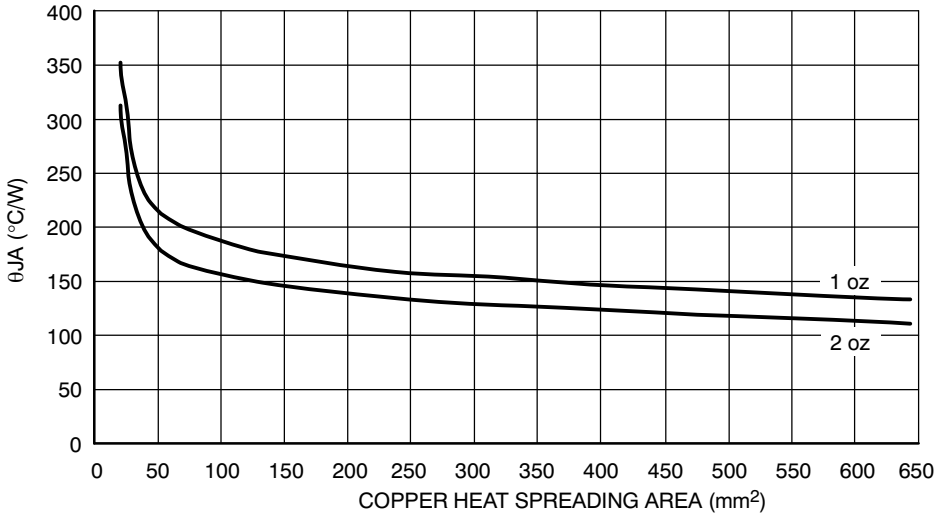


Figure 16. Thermal Performance on PCB Heat Spreader

Thermal impedance of the NCP590 DFN8 mounted to a single sided copper plated circuit board.

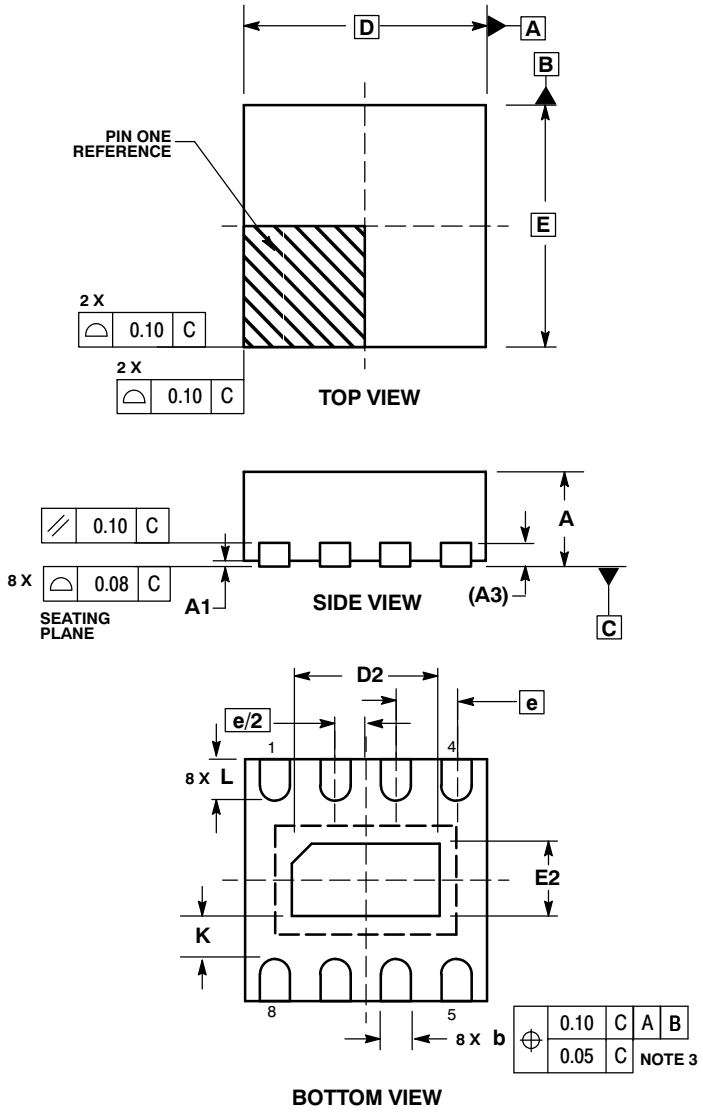
ORDERING INFORMATION*

Device	Output Voltage				
Orderable Part Number	Marking Code	V_{OUT1}	V_{OUT2}	Package	Shipping
NCP590MNVVTAG	VV	3.3	3.3	DFN8 2x2	10,000 / Tape & Reel
NCP590MNPPTAG	PP	2.8	2.8	DFN8 2x2	10,000 / Tape & Reel
NCP590MNDPTAG	DP	1.8	2.8	DFN8 2x2	10,000 / Tape & Reel
NCP590MNOATAG	OA	1.5	2.4	DFN8 2x2	10,000 / Tape & Reel
NCP590MN5DTAG	5D	1.2	1.8	DFN8 2x2	10,000 / Tape & Reel
NCP590MN5ATAG	5A	1.2	1.5	DFN8 2x2	10,000 / Tape & Reel

*Contact factory for additional voltage combinations.

PACKAGE DIMENSIONS

DFN8, 2x2
CASE 506AA−01
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.20	---
L	0.25	0.35

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