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FAIRCHILD SEMICONDUCTOR®

February 2008

FDG901D
Slew Rate Control IC for P-Channel MOSFETs

Features

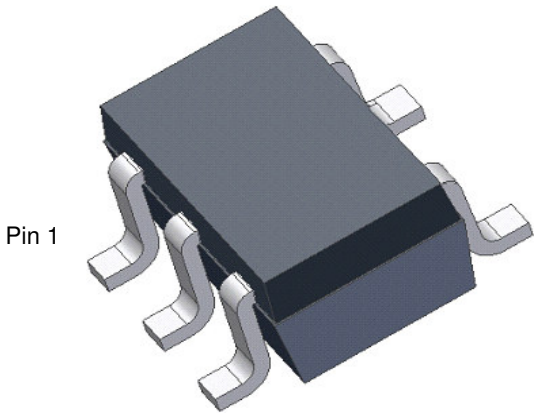
- Three Programmable Slew Rates
- Reduces Inrush Current
- Minimizes EMI
- Normal Turn-Off Speed
- Low-Power CMOS Operates Over Wide Voltage Range
- Compact Industry Standard SC70-5 Surface Mount Package
- RoHS Compliant

Applications

- Battery Load switch
- Power management

General Description

The FDG901D is specifically designed to control the turn on of a P-Channel MOSFET in order to limit the inrush current in battery switching applications with high capacitance loads. During turn-on, the FDG901D drives the MOSFET's gate low with a regulated current source, thereby controlling the MOSFET's turn on. For turn-off, the IC pulls the MOSFET gate up quickly for efficient turn off.

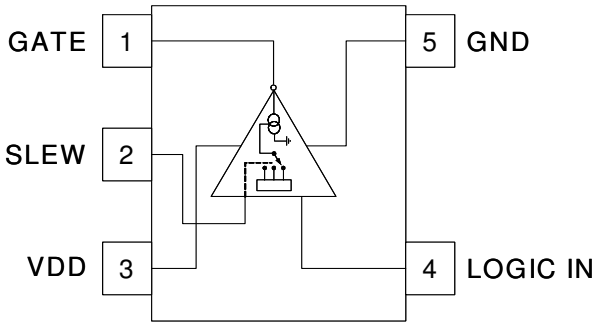


SC70-5

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
91	FDG901D	7”	8mm	3000 units

Pin Configuration



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltage	-0.5	10	V
DC Input Voltage (Logic Inputs)	-0.7	9	V
Power Dissipation for Single Operation @ 85°C		150	mW
Operating and Storage Junction Temperature	-65	150	°C
Thermal Resistance, Junction to Ambient (note 1)		425	°C/W

Recommended Operating Range

Parameter	Min.	Max.	Unit
Supply Voltage	2.7	6	V
Operating Junction Temperature	-40	150	°C

Electrical Characteristics

T_A = 25°C unless otherwise noted

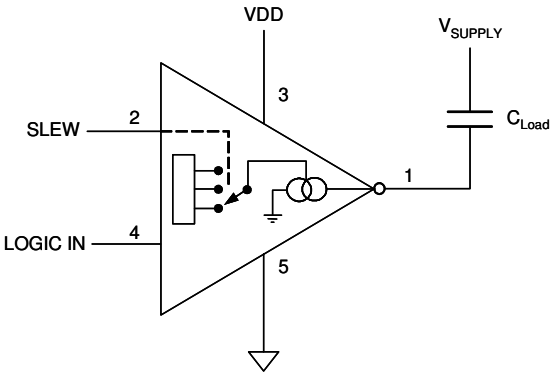
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Logic Levels							
Logic High Input Voltage	V_{IH}	V_{DD} = 2.7V to 6.0V		2.55			V
Logic Low Input Voltage	V_{IL}	V_{DD} = 2.7V to 6.0V				2.0	V
Off Characteristics - Slew Rate Control Driver							
Supply Input Breakdown Voltage	BV_{DG}	I_{DG} = 10µA, V_{IN} = 0V, V_{SLEW} = 0V		9			V
Slew Input Breakdown Voltage	BV_{SLEW}	I_{SLEW} = 10µA, V_{IN} = 0V		9			V
Logic Input Breakdown Voltage	BV_{IN}	I_{IN} = 10µA, V_{SLEW} = 0V		9			V
Supply Input Leakage Current	IR_{DG}	V_{DG} = 8V, V_{IN} = 0V, V_{SLEW} = 0V				100	nA
Slew Input Leakage Current	IR_{SLEW}	V_{SLEW} = 8V, V_{IN} = 0V				100	nA
Logic Input Leakage Current	IR_{IN}	V_{IN} = 8V, V_{SLEW} = 0V				100	nA
On Characteristics - Slew Rate Control Driver							
Gate Current	I_G	V_{IN} = 6V, V_{GATE} = 2V	Slew Pin = Open		90	120	µA
			Slew Pin = GND		1	10	µA
			Slew Pin = V_{DD}		10	50	nA

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

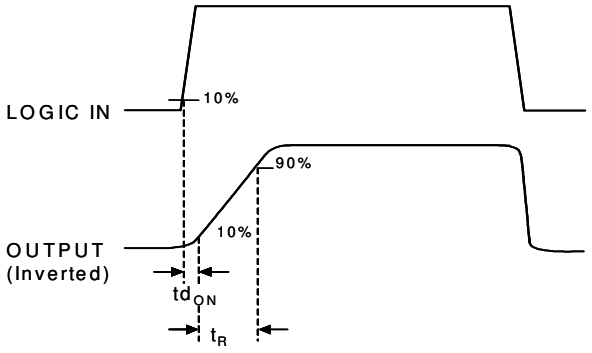
Electrical Characteristics Cont.

T_A = 25°C unless otherwise noted

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
P-Channel Switching Times (V_{SUPPLY} = 5.5V, V_{DD} = 5.5V, Logic IN = 5.5V, C_{LOAD} = 510pF, Test Circuit)							
Delay On Time	td_{ON}	Slew Pin	= Open		8.3		µs
			= GND		0.6		ms
			= V_{DD}		2.2		ms
V_{OUT} Rise Time	t_R	Slew Pin	= Open		28		µs
			= GND		1.8		ms
			= V_{DD}		11		ms
Output Slew Rate	dv/dt	Slew Pin	= Open		162		V/ms
			= GND		26		V/ms
			= V_{DD}		0.3		V/ms



Test Circuit



Switching Waveform

Typical Characteristics

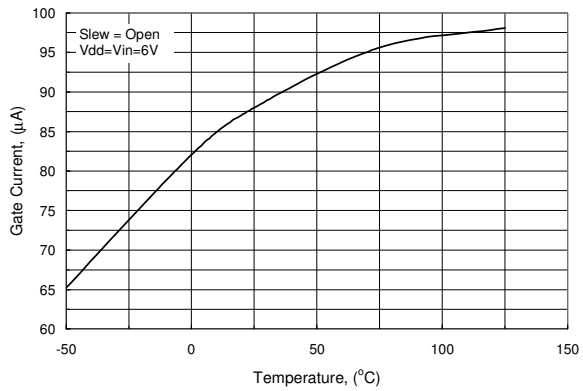


Figure 1. Gate Output Current vs. Temperature
(SLEW = OPEN)

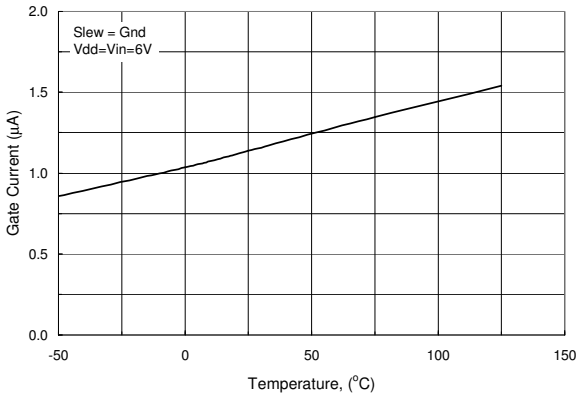


Figure 2. Gate Output Current vs. Temperature
(SLEW = GROUND)

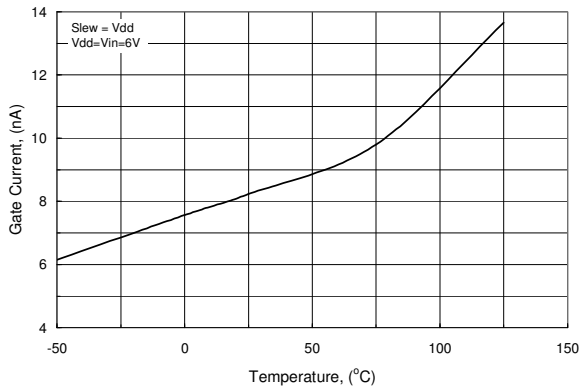


Figure 3. Gate Output Current vs. Temperature
(SLEW = V_{DD})

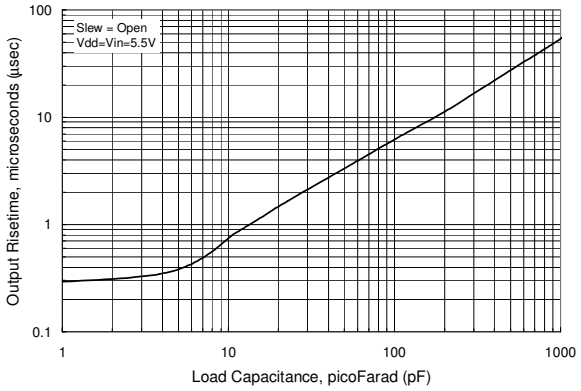


Figure 4. t_{RISE} vs. Load Capacitance
(SLEW = OPEN)

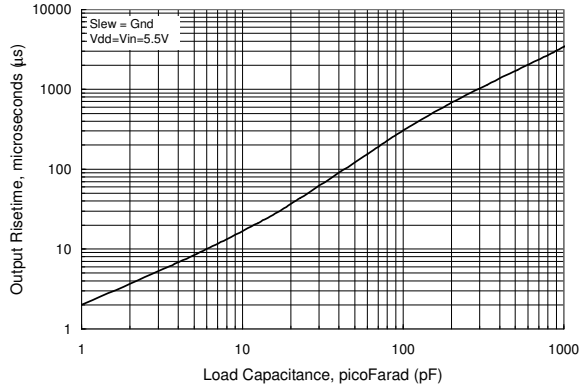


Figure 5. t_{RISE} vs. Load Capacitance
(SLEW = GROUND)

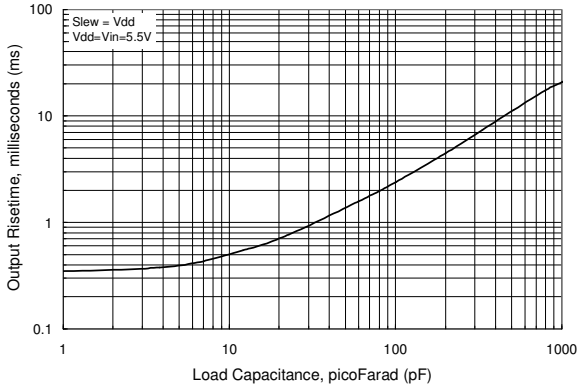


Figure 6. t_{RISE} vs. Load Capacitance
(SLEW = V_{DD})

Typical Characteristics

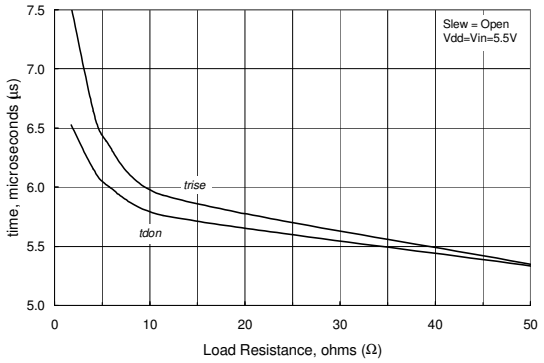


Figure 7. Switching Time vs. Load Resistance
(SLEW = OPEN)

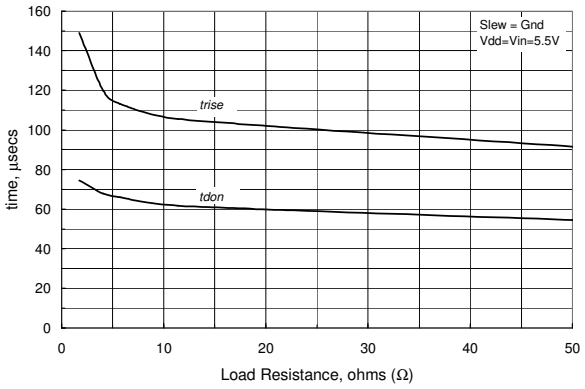


Figure 8. Switching Time vs. Load Resistance
(SLEW = GROUND)

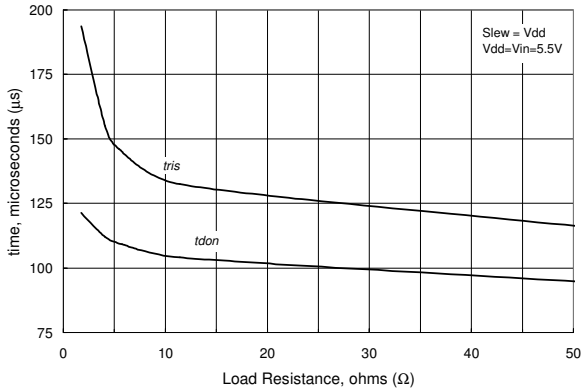


Figure 9. Switching Time vs. Load Resistance
(SLEW = V_{DD})

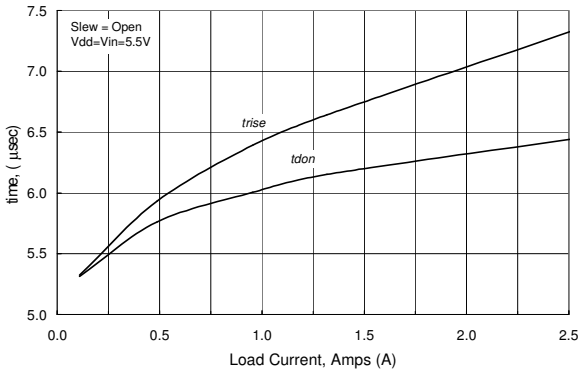


Figure 10. Switching Time vs. Load Current
(SLEW = OPEN)

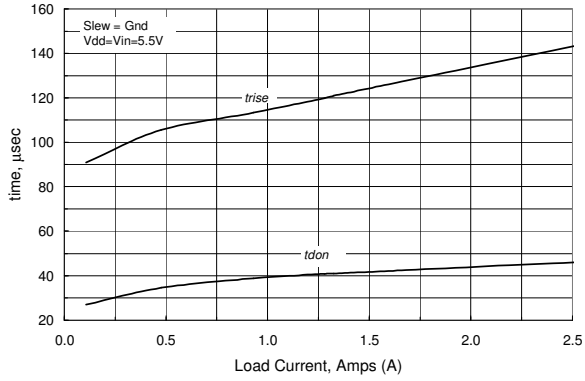


Figure 11. Switching Time vs. Load Current
(SLEW = GROUND)

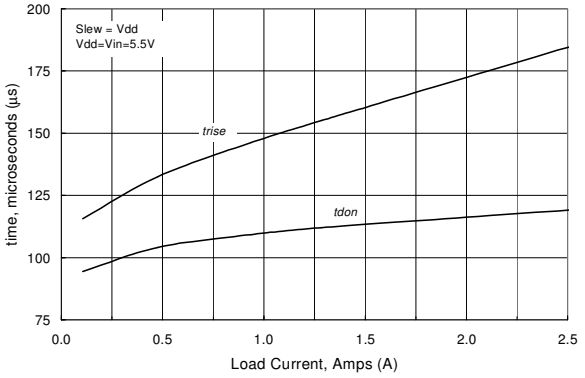
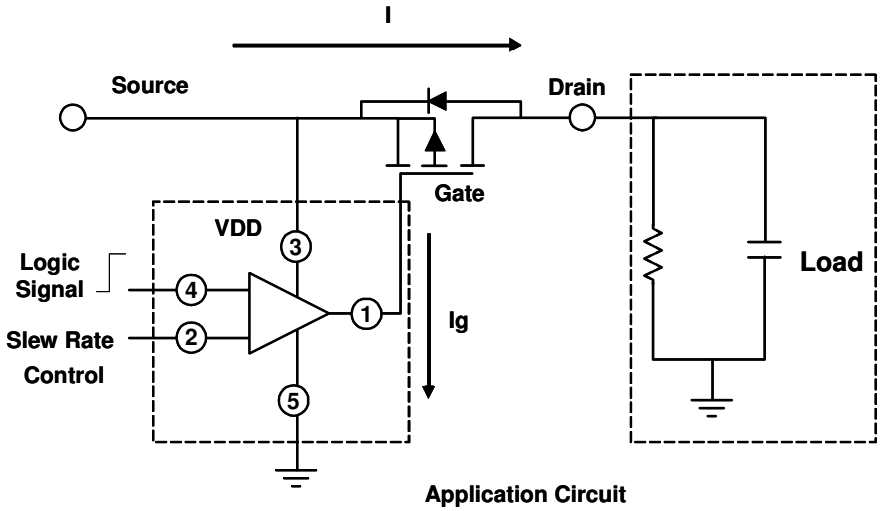


Figure 12. Switching Time vs. Load Current
(SLEW = V_{DD})

Application Information

Typical Application



Application Circuit

Battery powered systems make extensive usage of load switching, turning the power to subsystems off, in order to extend battery life. Power MOSFETs are used to accomplish this task. In PDA's and Cell phones, these MOSFETs are usually low threshold P-Channels. Since the loads typically include bypass capacitor components (high capacitive component), a high inrush current can occur when the load is switched on. This inrush current can cause transients on the main power supply disturbing circuitry supplied by it.

The simplest method of limiting the inrush current is to control the slew rate of the MOSFET switch. This can be done with external R/C circuits, but this approach can occupy significant PCB area, and involves other compromises in performance. The slew rate control driver IC FDG901D is specifically designed to interface low voltage digital circuitry with power MOSFETs and reduce the rapid inrush current in load switch applications. The IC limits inrush current by controlling the current, which drives the gate of the P-Channel MOSFET switch.

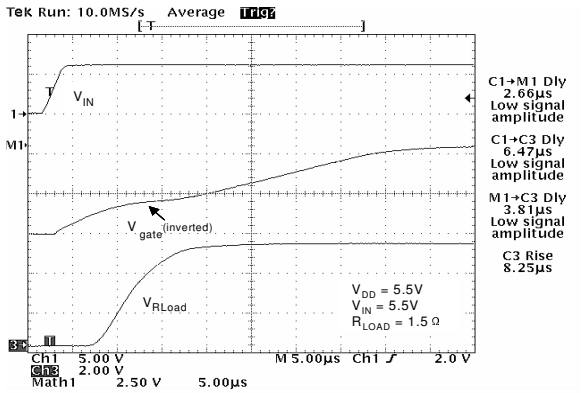
The control input is a CMOS compatible input with a minimum high input voltage of 2.55V with a power rail voltage of 6V. Therefore, it is compatible with any CMOS logic voltages between 2.55V and 5V and under these conditions there is no additional configuration required.

The Slew Rate Control Driver (FDG901D) is designed to give a programmed choice of one of three steady dv/dt states on the output during turn-on. To change the dv/dt value, the user needs to use the Slew Rate Control Pin (Pin 2). To utilize the smallest current setting (10 nA) from the IC, a voltage equal to V_{DD} must be applied to the Slew Rate Control Pin 2. To use the next higher current setting (~1µA) a voltage equal to Ground must be applied to Pin 2. To achieve the highest current setting (~80µA) or obtain a faster switching speed, the Slew Rate Pin2 must be open (floating). A higher value of capacitance will result in a slower switching rate. To determine the switching times of each setting use the simple equation:

$$t = \frac{Q_g}{I_G}$$

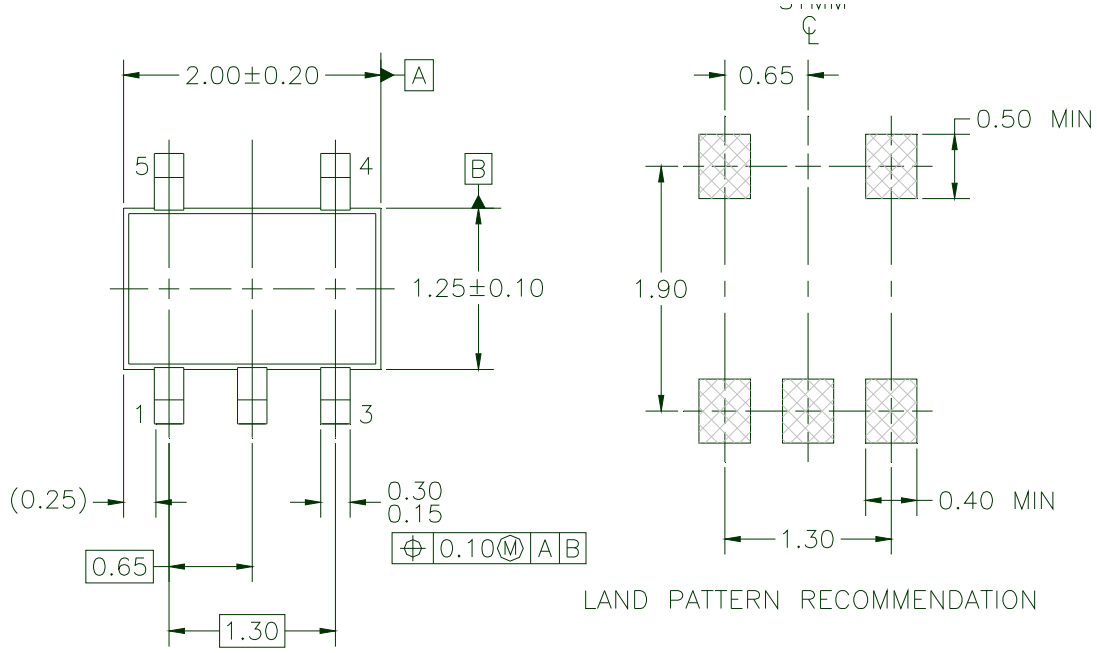
where Qg is the Gate charge in nC for a given MOSFET and IG is the gate current controlled by the slew rate pin.

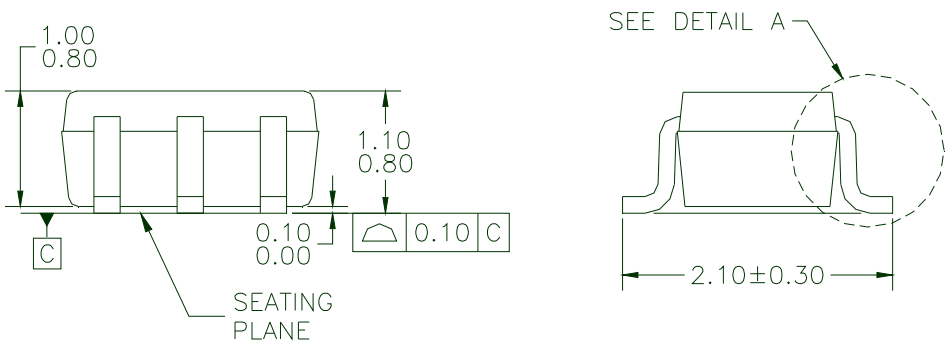
Below is a captured image from an oscilloscope depicting the device response. The FDG901D was connected to control an FDG258P P-Channel DMOS. The Slew Rate control pin was set to open (floating state).

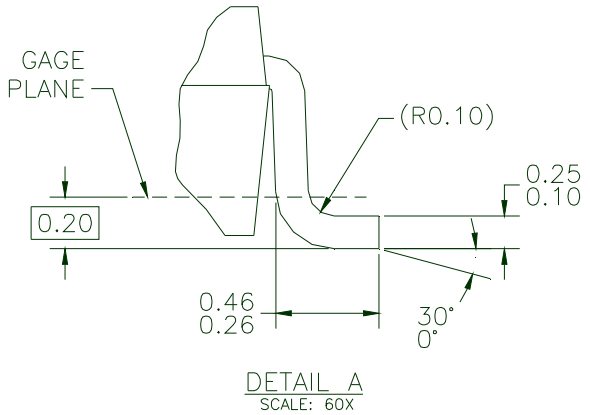


Circuit waveforms for an FDG901D controlling a P-Channel FDG258P MOFET

Dimensional Outline and Pad Layout







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